High-field-induced electron detrapping in an AlGaN/GaN high electron mobility transistor

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A step stress test is carried out to study the reliability characteristics of an AlGaN/GaN high electron mobility transistor (HEMT). An anomalous critical drain-to-gate voltage with a negative temperature coefficient is observed in the stress sequence, beyond which the HEMT device starts to recover from degradation induced by early lower voltage stress. While the performance degradation featuring the drain current slump stems from electron trapping in the surface or bulk states during low-to-medium bias stress, the recovery is attributed to high field induced electron detrapping. The carrier detrapping mechanism could be helpful for lessening the trapping-related performance degradation of a GaN-based HEMT.

Keywords: AlGaN/GaN HEMT, step stress test, high electric field, electron detrapping

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1. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are the most promising candidates for high-frequency and high-power microwave applications due to the intrinsic material advantages of GaN-based semiconductors.[1,2] Recently although impressive improvement in device performance has been reported, there remain challenges to realibility hindering the extensive commercial applications of GaN-based HEMTs.[3−6] In particular, imperfect material quality, a strong polarization effect, variation in processing technologies and testing methods make the investigation of their reliability very complicated. For example, both reversible and irreversible degradation behaviours have been reported in stress-accelerated-degradation tests.[7−14] The former, typically the so-called current slump, is usually induced by carrier trapping either on the device surface or within the bulk semiconductor, and the HEMTs would instantly or gradually return to their original state after removing the stress bias.[7] However, the detailed trapping process is not fully understood yet and is likely to vary from device to device made in different laboratories.[8−10] The latter often involves a new defect generation. A typical case is the recently suggested high-voltage-driven inverse piezoelectric effect, which could introduce mechanical stress in the AlGaN barrier and eventually produce structural defects.[11] Although this undesirable effect has been supported by several experimental studies, the reported critical voltage varies considerably from device to device.[13] With the help of barrier layer engineering or a special metalization scheme, some devices could even withstand a very high drain voltage without permanent degradation.[14,15]

In the present work, we select a step stress test to investigate the reliability characteristics of AlGaN/GaN HEMT. In a low-to-medium stress voltage range, the device suffers from an enhanced carrier-trapping-induced current slump. However, a critical voltage is observed in the high stress voltage range, beyond which the HEMT device starts to recover from degradation induced by early lower voltage stress. The recovery process is explained by a high electric field induced electron detrapping mechanism.

2. Sample preparation

The AlGaN/GaN hetero-structure was grown by metal–organic chemical vapour deposition on

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a semi-insulating 4H–SiC substrate, which consists of i-$Al_{0.25}Ga_{0.75}N$(5 nm)/n-$Al_{0.25}Ga_{0.75}N$ (10 nm)/i-$Al_{0.25}Ga_{0.75}N$(6 nm)/AlN(1 nm)/i-GaN(2 μm). The sheet carrier density and electron mobility of the epi-structure are 1×10^{13} cm^{-2} and 1600 $cm^2/V\cdot s$ respectively. Standard processing steps were employed to fabricate the HEMT devices. Optical lithography was used to define the source/drain Ohmic contacts, in which Ti/Al/Ni/Au metal stacks were deposited by e-beam evaporation followed by annealing in ambient N_2 for 30 s. E-beam lithography was used to fabricate the 0.75-μm long and 10×100-μm wide Ni/Au Schottky barrier gates each with an 8-nm dry-etched gate recess. The source-to-drain and source-to-gate distance are 4.5 μm and 1.5 μm respectively. Finally, the devices were passivated by a 100-nm thick SiN_x film deposited by plasma-enhanced chemical vapour deposition.

3. Experiments and discussion

Firstly, a drain–voltage step stress test is conducted by gradually increasing the drain-to-source voltage (V_{DS}) from 0 V to 78 V in steps of 2 V when the device is biased in pinch-off state (V_{GS} (gate-to-source voltage)=−5 V). This set-up (the inset of Fig. 1(a)) has been chosen to simulate the real bias conditions of a working HEMT device. At each voltage step the device is continuously stressed for 1 min, during which the $I_{G(stress)}$ (gate leakage current at each stress voltage) is sampled to monitor the stress process. After each stress step, $I_{D(on)}$ (a partially "on" drain current at V_{DS} = 4 V and V_{GS} = −0.5 V) and $I_{G(off)}$ (reverse gate current at V_{DS} = 4 V and V_{GS} = −2 V) are quickly measured to evaluate the resulting device performance. The corresponding measurement time is less than 3 s and then a new stress cycle is applied.

As shown in Fig. 1(a), with stress voltage increasing, $I_{D(on)}$ and $I_{G(off)}$ first continually decrease while $I_{G(stress)}$ maintains at a relatively stable level. Interestingly, as the stress voltage further increases, at ∼ 55 V $I_{D(on)}$ and $I_{G(off)}$ start to increase, which is also coupled with an increase in $I_{G(stress)}$. After the last stress cycle with V_{DG-max} = 83 V, above which the device is prone to an off-state breakdown, $I_{D(on)}$ and $I_{G(off)}$ are even larger than their original values. That is, a well-defined critical stress voltage is observed here, beyond which the device begins to recover from a current slump induced by an early lower voltage stress.

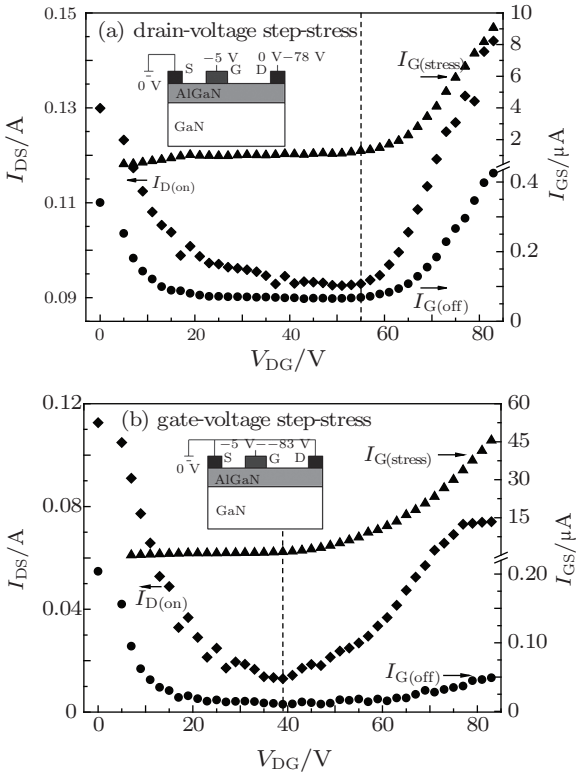


Fig. 1. Evolutions of $I_{G(stress)}$, $I_{D(on)}$ (V_{DS} = 4 V, V_{GS} = −0.5 V), and $I_{G(off)}$ (V_{DS} = 4 V , V_{GS} = −2 V) each as a function of the stress voltage V_{GD} in the drain–voltage step stress test (a) and in the gate–voltage step stress test (b). The insets show the measurement setup.

To further confirm the observed phenomenon, a gate-voltage step stress test at V_{DS} = 0 V is also conducted, during which the stress voltage (V_{GS}) steadily increases from −5 V to −83 V. As shown in Fig. 1(b), a similar performance recovery process occurs at a relatively low stress voltage of about 40 V. Meanwhile, the device exhibits a more serious current slump but a smaller degree of current recovery than those observed in the drain–voltage step stress test. These differences are strong evidence that the recovery process is field-dependent, considering the smaller gate-to-source distance relative to the gate-to-drain distance. In addition, when the maximum field strength at the source side of the device is high enough for the recovery mechanism, the drain side is still in a degradation state, leading to an overall smaller degree of current recovery. The above analysis is supported by the distribution of leakage current among the three terminals of the device during stress. Due to the good pinch-off property of our device, buffer leakage is found to be negligible and I_G is approximately the sum of I_S and I_D during stress. Thus, the relative magnitude of I_D to I_G at each stress voltage can be qualitatively used to compare the electric field strengths between the drain

and source sides of the gate. As shown in Fig. 2, in a high stress voltage range $I_{\mathrm{D(stress)}}/I_{\mathrm{G(stress)}}$ quickly reduces from more than 0.4 to $\sim$ 0.1 for the gate–voltage step stress, while $I_{\mathrm{D(stress)}}/I_{\mathrm{G(stress)}}$ is more than 0.8 for the drain–voltage step stress.

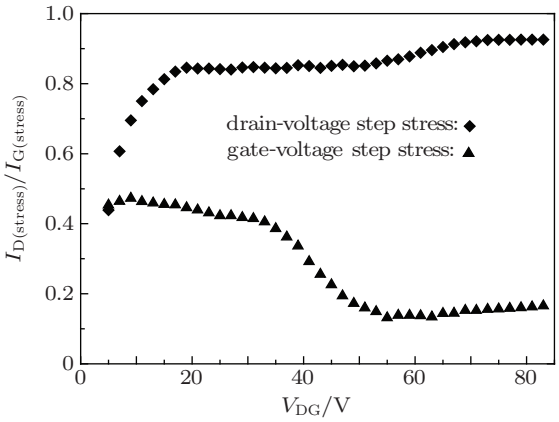


Fig. 2. Evolutions of $I_{\mathrm{D(stress)}}/I_{\mathrm{G(stress)}}$ each as a function of V_{DG} in drain–voltage and gate–voltage step stress tests.

Based on conventional wisdom, the HEMT degradation in the low-to-medium stress voltage range should be caused by the carrier trapping related effect.[16] That is, with stress voltage increasing, the enhanced electrical field would change the relative energy positions of some surface or bulk states, and these trap states could then capture leaked electrons. The trapped electrons could in turn modify the barrier shape and cause additional depletion of the two-dimensional electron gas (2DEG). Thus, after stress $I_{\mathrm{D(on)}}$ would show a current slump. Actually, a similar mechanism could also cause the frequently observed "kink" effect in the output characteristics of a GaN-based HEMT.[10] In particular, some trapped electrons are expected to stay within the AlGaN barrier of our device, as a simultaneous reduction of the field-dependent gate leakage current $I_{\mathrm{G(off)}}$ is observed. Unlike $I_{\mathrm{G(off)}}$ and $I_{\mathrm{D(on)}}$, during stress $I_{\mathrm{G(stress)}}$ would maintain a stable level, owing to the ever increased stress voltage.

A major observation of this work is the high-voltage-stress-induced current recovery, which acts contrary to the common trend of a more serious degradation after higher voltage stress. If the current slump is caused by carrier trapping, the current recovery process should then be caused by carrier detrapping, as the device exhibits highly reproducible behaviours in repeated stress sequence. To further understand the detrapping mechanism, a drain–voltage step stress test is carried out at elevated temperatures. Here again a partially "on" current I_{DS} at $V_{\mathrm{DS}} = 4$ V and $V_{\mathrm{GS}} = -0.5$ V is recorded after each step to minimize the self-heating effect. As shown in Fig. 3, the critical voltage for current recovery shows a clear negative temperature coefficient, which can be explained by thermally-assisted detrapping. Since enhanced thermal energy also reduces carrier trapping, the observation that the overall drain current I_{DS} at high temperature (360 K) is ever higher than that at room temperature (300 K) can also be understood.[17] In addition, this result further suggests that the impact ionization related effect is not a major mechanism for the detrapping process as phonon scattering would be strengthened at high temperatures.[18]

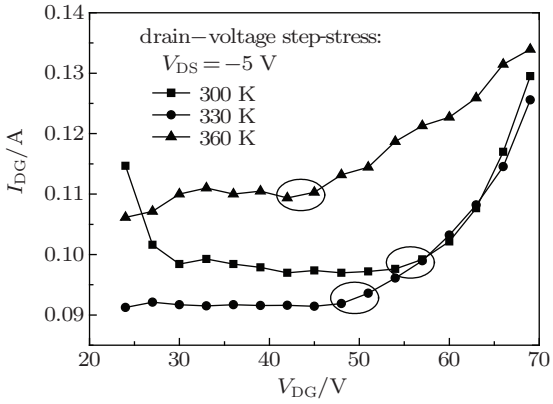


Fig. 3. Evolutions of I_{DS} ($V_{\mathrm{DS}} = 4$ V, $V_{\mathrm{GS}} = -0.5$ V) each as a function of V_{GD} in drain–voltage step stress tests at different temperatures.

Since the observed carrier detrapping process requires a well-defined critical voltage, a high field induced effect which can lower the energy barrier for electron runaway should be the primary mechanism, such as field-dependent electron tunneling or Frenkel–Poole emission or related effects.[19] The evolution of device behaviour throughout the whole stress sequence further suggests that the carrier trapping and detrapping mechanisms should co-exist in the HEMT device, and each of them is a strong function of electrical field strength. Nevertheless, the two mechanisms have different characteristic energies, which can explain why the trapping process dominates in the low-to-medium stress voltage range but is surpassed by the detrapping process in the high stress voltage range.

If the above physical picture is true, a high voltage operation is expected to be helpful for alleviating trap-related adverse effects for a GaN-based HEMT, as long as the device operates in a safe bias range. To prove the possibility, long time off-state stress at medium and high drain voltages are carried out respectively.

The transfer characteristics of the stressed devices are measured directly after having been stressed and are compared with those of the fresh device. As shown in Fig. 4, apparent device degradation in terms of drain current and transconductance is observed after a 1-h stress at bias of $V_{GS} = -5$ V and $V_{DS} = 35$ V (smaller than the critical voltage). On the contrary, after the same long time stress at bias of $V_{GS} = -5$ V and $V_{DS} = 70$ V (larger than the critical voltage), the device shows no degradation but an even larger drain current and a roughly similar transconductance. The increased drain current and the negative shift of threshold voltage after high voltage stress, compared with those of unstressed devices, are caused by the de-trapping of trapped electrons originally existing within the fresh device. This observation is consistent with the results shown in Fig. 1(a), in which the final $I_{D(on)}$ in the step-stress test is even larger than its original value before being stressed. Here it should be noted that no permanent degradation is found in our devices after the long time stress and the device behaviours are fully reversible. It means that at least the high stress voltage applied ($V_{DG} \leq 83$ V) is not enough to trigger structural defect generation induced by the inverse piezoelectric effect, which is suggested to require a threshold electrical field and depend little on the total stress time.

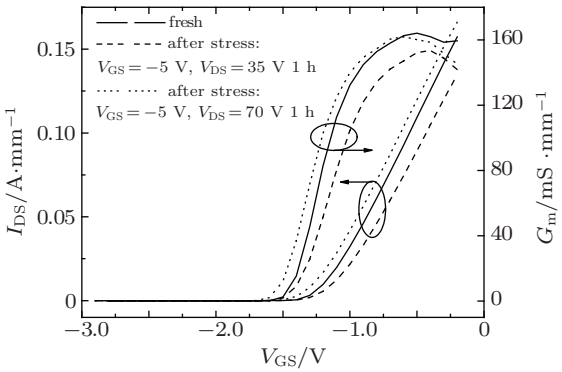


Fig. 4. DC transfer characteristics and transconductance curves ($V_{DS} = 4$ V) before stress (dash–dot lines), after a 1-h stress at $V_{GS} = -5$ V and $V_{DS} = 35$ V (dot lines), after a 1-h stress at $V_{GS} = -5$ V and $V_{DS} = 70$ V (dash lines).

4. Summary

In this paper, a critical stress voltage is observed in the step stress tests, beyond which the AlGaN/GaN HEMT starts to recover from the drain current slump induced by the lower voltage stress. The recovery process is explained by a high field-induced carrier detrapping mechanism, while the device degradation in the low-to-medium stress voltage range is caused by carrier trapping in surface or bulk states. The suggested carrier detrapping mechanism could be helpful for lessening trapping-related performance degradation of GaN-based HEMT. Meanwhile, a reliability study based on pulsed I–V measurement is under way for further confirming the trapping/detrapping mechanisms.[20]

References

[1] Wu Y F, Kapolnek D, Ibbetson J P, Parikh P, Keller B P and Mishra U K 2001 *IEEE Trans. Electron Dev.* **48** 586

[2] Eastman L F, Tilak V, Smart J, Green B M, Chumbes E M, Dimitrov R, Kim H, Ambacher O S, Weimann N, Prunty T, Murphy M, Schaff W J and Shealy J R 2001 *IEEE Trans. Electron Dev.* **48** 479

[3] Bi Z W, Hu Z H, Mao W, Hao Y, Feng Q, Cao Y R, Gao Z Y, Zhang J C, Ma X H, Chang Y M, Li Z M and Mei N 2011 *Chin. Phys.* B **20** 087307

[4] Fan L, Hao Y, Zhao Y F, Zhang J C, Gao Z Y and Li P X 2009 *Chin. Phys.* B **18** 2912

[5] del Alamo J A and Joh J 2009 *Microelectron. Reliab.* **49** 1200

[6] Meneghesso G, Verzellesi G, Danesin F, Rampazzo F, Zanon F, Tazzoli A, Meneghini M and Zanoni E 2008 *IEEE Trans. Dev. Mater. Reliab.* **8** 332

[7] Vetury R Q, Zhang N, Keller S K and Mishra U 2001 *IEEE Electron Dev. Lett.* **48** 560

[8] Meneghesso G, Zanon F, Uren M J and Zanoni E 2009 *IEEE Electron Dev. Lett.* **30** 100

[9] Wang M J and Chen K J 2011 *IEEE Electron Dev. Lett.* **32** 482

[10] Fu L H, Lu H, Chen D J, Zhang R, Zheng Y D, Chen T S, Wei K and Liu X Y 2011 *Appl. Phys. Lett.* **98** 173058

[11] Joh J and del Alamo J A 2008 *IEEE Electron Dev. Lett.* **29** 287

[12] Ma X H, Jiao Y, Ma P, He Q, Ma J G, Zhang K, Zhang H L, Zhang J C and Hao Y 2011 *Chin. Phys.* B **20** 127305

[13] Casa M, Dammann M, Polyako V, Waltereit P, Quay R, Mikulla M and Ambache O 2011 *Microelectron. Reliab.* **51** 224

[14] Ivo P, Glowacki A, Bahat-Treidel E, Lossy R, Würfl J, Boit C and Trakle G 2011 *Microelectron. Reliab.* **51** 217

[15] Lo C F, Liu L, Kang T S, Davies R, Gila B P, Pearton S J, Kravchenko II, Laboutin O, Cao Y, Johnson W J and Ren F 2011 *Electrochem. Solid State Lett.* **14** 264

[16] Joh J and del Alamo J A 2011 *IEEE Trans. Electron Dev.* **58** 132

[17] Meneghesso G, Verzellesi G, Pierobon R, Rampazzo F, Chini A K, Mishra U, Canali C, Member A and Zanoni E 2004 *IEEE Trans. Electron Dev.* **51** 1554

[18] Dyakonova N, Dickens A, Shura M S, Gaska R and Yang J W 1998 *Appl. Phys. Lett.* **72** 2562

[19] Mitrofanov O and Manfra M 2004 *J. Appl. Phys.* **95** 6414

[20] Zanoni E, Danesin F, Meneghini M, Cetronio A, Lanzieri C, Peroni M and Meneghesso G 2009 *IEEE Electron Dev. Lett.* **30** 427