Breakdown voltage model and structure realization of a thin silicon layer with linear variable doping on a silicon on insulator high voltage device with multiple step field plates*

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Based on the theoretical and experimental investigation of a thin silicon layer (TSL) with linear variable doping (LVD) and further research on the TSL LVD with a multiple step field plate (MSFP), a breakdown voltage (BV) model is proposed and experimentally verified in this paper. With the two-dimensional Poisson equation of the silicon on insulator (SOI) device, the lateral electric field in drift region of the thin silicon layer is assumed to be constant. For the SOI device with LVD in the thin silicon layer, the dependence of the BV on impurity concentration under the drain is investigated by an enhanced dielectric layer field (ENDIF), from which the reduced surface field (RESURF) condition is deduced. The drain in the centre of the device has a good self-isolation effect, but the problem of the high voltage interconnection (HVI) line will become serious. The two step field plates including the source field plate and gate field plate can be adopted to shield the HVI adverse effect on the device. Based on this model, the TSL LVD SOI n-channel lateral double-diffused MOSFET (nLDMOS) with MSFP is realized. The experimental breakdown voltage (BV) and specific on-resistance ($R_{\rm on,sp}$) of the TSL LVD SOI device are 694 V and 21.3 Ω·mm^2 with a drift region length of 60 μm, buried oxide layer of 3 μm, and silicon layer of 0.15 μm, respectively.

Keywords: breakdown voltage model, enhanced dielectric layer field, thin silicon layer, linear variable doping, multiple step field plates

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1. Introduction

Compared with the thick layer silicon on insulator (SOI), the thin layer SOI has an improved latch-up effect, reduced parasitic capacitance, better process compatibility, etc. Therefore, the thin layer (SOI) has become a mainstream SOI technology.[1−3] The conventional SOI high voltage device has low vertical breakdown voltages ($V_{\rm B,V}$), especially for the thin layer SOI device, and some studies have been carried out.[4−7] Enhancing the electric field of the buried dielectric layer is a feasible way to increase the $V_{\rm B,V}$ by enhancing the dielectric layer field (ENDIF) and several novel structures have been proposed.[8−11] Based on the theoretical and experimental investigation of TSL with LVD,[12] a TSL LVD SOI n-channel lateral double-diffused MOSFET (nLDMOS) with MSFP and its breakdown voltage model are proposed in this paper. The influences of structure parameters on BV and $R_{\rm on,sp}$ are analysed by MEDICI and TSUPREM4,[13] and the relevant experiments are realized.

2. Structure and mechanism

The TSL SOI nLDMOS with MSFP and its physical mechanism are shown in Fig. 1. The thickness of the silicon layer is thinned and the LVD drift region can improve the critical electric field of the silicon layer ($E_{\rm S,C}$) and enhance the dielectric buried layer electric field ($E_{\rm I}$), thus the BV can be increased. The LVD technology can optimize the surface electric field distribution of the device for realizing high BV and low $R_{\rm on,sp}$. The MSFP can eliminate the adverse effects of HVI to make the device have a high reliability. $t_{\rm f}$,

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$t_{\rm I}$, $t_{\rm S}$, and $t_{\rm soi}$ are the thicknesses of the thin field oxide layer, the buried oxide layer, the thin silicon layer, and the SOI layer, respectively. $L_{\rm g}$, $L_{\rm f1}$, $L_{\rm f2}$, $L_{\rm f3}$, $L_{\rm f4}$, and $L_{\rm d}$ are the lengths of the channel, the distance between the P-well region and the thin field oxide region, the distance between the P-well region and the thick field oxide region, the length of gate poly field plate, the length of the source metal field plate, and the length of the drift region, respectively. $N(x)$ is the doping concentration of the drift region.

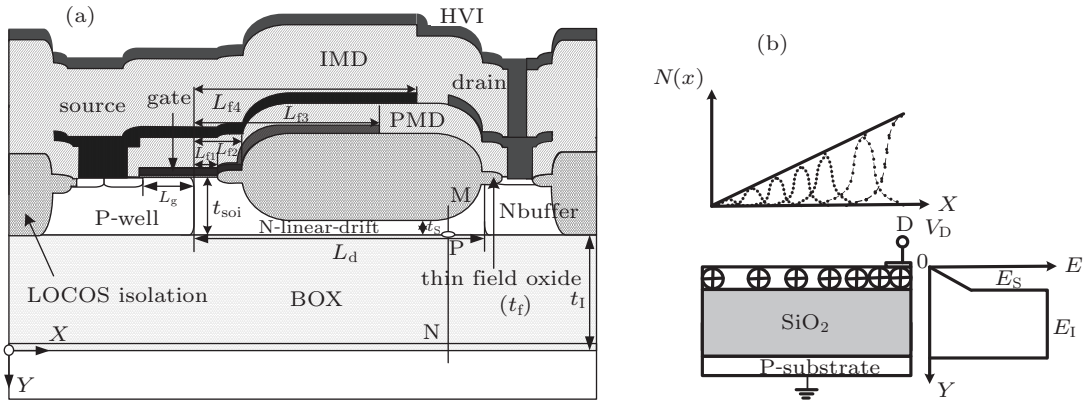


Fig. 1. Structure and mechanism of the TSL LVD SOI nLDMOS with MSFP. (a) Device structure and (b) working mechanism.

For a lateral SOI high voltage nLDMOS device which is optimized by junction termination technology, its BV lies on the vertical BV ($V_{\rm B,V}$), while the source and substrate are grounded. The two-dimensional (2D) potential $\phi(x,y)$ in the drift region can be written as

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=-\frac{qN(x)}{\varepsilon_{\rm S}},$$
$$0\le x\le L_{\rm d},\ 0\le y\le t_{\rm S}. \tag{1}$$

For a full depleted drift region, the vertical electric field of the top silicon layer can be shown as

$$E_y(x,y)=-\frac{\partial\phi(x,y)}{\partial y}=\psi_1(x)+\psi_2(x)y,$$
$$0\le x\le L_{\rm d},\ 0\le y\le t_{\rm S}. \tag{2}$$

In most of the drift region area, the length of the field plate is much greater than the thicknesses of the field oxide layer and the depletion layer. Therefore, the field plate can be taken as an infinite field plate. The boundary conditions of the surface and interface of the drift region satisfy

$$\left.\frac{\partial\phi(x,y)}{\partial y}\right|_{y=0}=\frac{\varepsilon_{\rm I}\phi(x,0)}{\varepsilon_{\rm s}t_{\rm f}}, \tag{3a}$$
$$\phi(0,0)=0,\quad \phi(L_{\rm d},0)=V_{\rm d}, \tag{3b}$$
$$\frac{\varepsilon_{\rm I}\phi(x,t_{\rm S})}{t_{\rm I}}=-\left.\frac{\partial\phi(x,y)}{\partial y}\varepsilon_{\rm S}\right|_{y=t_{\rm S}}. \tag{3c}$$

Solving Eq. (2) with the boundary conditions yields

$$\left.\frac{\partial^2\phi(x,y)}{\partial y^2}\right|_{y=0}=-\frac{\phi(x,0)}{t^2}, \tag{4}$$

where

$$t=\left(\frac{\left(t_{\rm S}t_{\rm I}\varepsilon_{\rm s}+\frac{1}{2}\varepsilon_{\rm I}t_{\rm S}^2\right)\varepsilon_{\rm s}t_{\rm f}}{\varepsilon_{\rm s}\varepsilon_{\rm I}t_{\rm I}+\varepsilon_{\rm I}^2t_{\rm S}+\varepsilon_{\rm s}\varepsilon_{\rm I}t_{\rm f}}\right)^{1/2}$$

is the characteristic thickness of the SOI device.

When $t_{\rm f}$ approaches infinity, the above characteristic thickness becomes the characteristic thickness of conventional device, that is,

$$t=\sqrt{\frac{1}{2}t_{\rm S}^2+\frac{\varepsilon_{\rm S}}{\varepsilon_{\rm I}}t_{\rm S}t_{\rm I}}.$$

From Eq. (4), we have

$$\phi(x,y)=\left(1-\frac{\varepsilon_{\rm I}}{\varepsilon_{\rm s}t_{\rm f}}y-\frac{y^2}{2t^2}\right)\phi(x,0). \tag{5}$$

Solving Eq. (5), the electric potential $\phi(x,y)$ under the drain is derived as

$$\phi(L_{\rm d},y)=\left(1-\frac{\varepsilon_{\rm I}}{\varepsilon_{\rm s}t_{\rm f}}y-\frac{y^2}{2t^2}\right)\phi(L_{\rm d},0). \tag{6}$$

Solving Eq. (6), the vertical electric field under the drain is obtained as

$$E_y(L_{\rm d},y)=\left(\frac{\varepsilon_{\rm I}}{\varepsilon_{\rm s}t_{\rm f}}+\frac{y}{t^2}\right)\phi(L_{\rm d},0). \tag{7}$$

In the following, the drift region doping concentration function is deduced. When the thickness of

the silicon layer is thin (0.1 μm in magnitude), on the assumption that the silicon layer lateral electric field component is constant, that is $\partial E_x(x,y)/\partial x = 0$, the Poisson equation can be simplified into

$$\frac{\partial^2 \phi(x,y)}{\partial y^2} = -\frac{qN(x)}{\varepsilon_{\rm S}}, \quad 0 \le x \le L_{\rm d},\ 0 \le y \le t_{\rm S}. \tag{8}$$

Solving Eq. (5) with the same boundary conditions, we have

$$\phi(x,y) = -\frac{1}{2}\frac{qN(x)}{\varepsilon_{\rm S}}y^2 + \frac{\varepsilon_{\rm I}}{\varepsilon_{\rm S}t_{\rm f}}\frac{qN(x)}{\varepsilon_{\rm S}}t^2 y + \frac{qN(x)}{\varepsilon_{\rm S}}t^2. \tag{9}$$

Let $y = 0$ in Eq. (9), then the surface electric potential and electric field will be as follows:

$$\phi(x,0) = \frac{qN(x)}{\varepsilon_{\rm S}}t^2, \tag{10}$$

$$E_x(x,0) = -\frac{{\rm d}\phi(x,0)}{{\rm d}x} = -\frac{qt^2}{\varepsilon_{\rm S}}\frac{{\rm d}N(x)}{{\rm d}x}. \tag{11}$$

Equation (11) shows that the surface electric field of a TSL LVD device with MSFP is proportional to the slope of the doping concentration. This is the reason why the TSL structure is doped with LVD.

$$E_y(x,y) = -\frac{\partial \phi(x,y)}{\partial y} = \frac{qN(x)}{\varepsilon_{\rm S}}y - \frac{\varepsilon_{\rm I}}{\varepsilon_{\rm S}t_{\rm f}}\frac{qN(x)}{\varepsilon_{\rm S}}t^2, \tag{12}$$

$$E_y(L_{\rm d},t_{\rm S}) = -\left.\frac{\partial \phi(x,y)}{\partial y}\right|_{x=L_{\rm d},y=t_{\rm S}} = \frac{qN(L_{\rm d})}{\varepsilon_{\rm S}}t_{\rm S} - \frac{\varepsilon_{\rm I}}{\varepsilon_{\rm S}t_{\rm f}}\frac{qN(L_{\rm d})}{\varepsilon_{\rm S}}t^2. \tag{13}$$

When the RESURF condition is satisfied, the device breakdown point is located on the top interface of the buried layer at the drain end. At breakdown, the electric field of the silicon layer (at P point) is the critical breakdown electric field ($E_{\rm S} = E_{\rm S,C}$), so the interface electric field layer of the silicon layer is expressed as

$$E_{\rm S,C} = \frac{qN(L_{\rm d})}{\varepsilon_{\rm S}}t_{\rm S} - \frac{\varepsilon_{\rm I}}{\varepsilon_{\rm S}t_{\rm f}}\frac{qN(L_{\rm d})}{\varepsilon_{\rm S}}t^2. \tag{14}$$

Based on Eq. (13), the electric field of the top silicon layer ($E_{\rm S}$) is linearly distributed from the surface ($y = 0$) to the interface ($y = t_{\rm S}$). The vertical voltage $V_{\rm B,V}$ is obtained as

$$V_{\rm B,V} = \frac{1}{2}t_{\rm S}E_{\rm S,C} + t_{\rm I}E_{\rm I}. \tag{15}$$

For the device without field plates, along the MN direction, a one-dimensional approximation about $E_{\rm S} = yE_{\rm S,C}/t_{\rm S}$ and $E_{\rm I} = \varepsilon_{\rm S}E_{\rm S,C}/\varepsilon_{\rm I}$ is obtained. Using the effective threshold energy of ionization rate formula $\alpha_{\rm eff}(E) = 70.3\exp(-146.8/E)$, the threshold energy $\varepsilon_{\rm T}$[14] is attained by electron multiplying. Based on the classic avalanche breakdown threshold energy conditions

$$\int_0^{t_{\rm S}} 70.3\exp\left(-\frac{146.8}{E(y)}\right){\rm d}y = 1,$$

the following equation can be introduced

$$70.3\gamma t_{\rm S}\left(\frac{{\rm e}^{-\gamma}}{\gamma} - \int_1^{\infty}\frac{{\rm e}^{-u\gamma}}{u}{\rm d}u\right) = 1, \tag{16}$$

where $\gamma = 146.8/E_{\rm S,C}$, equation (14) is the relationship between $E_{\rm S,C}$ and $t_{\rm S}$. To meet the RESURF condition of $N_{\rm d}t_{\rm S} = \varepsilon_{\rm S}E_{\rm S,C}/q$, the relationship between $E_{\rm S,C}$ and $N_{\rm d}$ is obtained as

$$N(L_{\rm d}) = \frac{\varepsilon_{\rm S}}{q}\frac{10320.04}{\gamma}\left({\rm e}^{-\gamma} - \gamma\int_1^{\infty}\frac{{\rm e}^{-u\gamma}}{u}{\rm d}u\right). \tag{17}$$

Through the nonlinear curve fitting equation (17), $E_{\rm S,C}(\times 10^5$ V/cm) is obtained as

$$E_{\rm S,C} = 2.19 + 7.1\times 10^{-8}N(L_{\rm d})^{0.46}. \tag{18}$$

When the device has field plates, the breakdown point may be located in the surface of the silicon layer under the drain or the interface of the buried layer. The surface electric field and interface electric field are smaller than the critical electric field of the silicon layer, so based on Eq. (12), the relationship of the interface electric field with the critical electric field of silicon layer breakdown is obtained as

$$\frac{qN(L_{\rm d})t_{\rm S}}{\varepsilon_{\rm S}}\left(1 - \frac{t^2}{3t_{\rm f}t_{\rm S}}\right) \le E_{\rm S,C}. \tag{19}$$

At the same time, the relationship of the surface electric field with the critical electric field of the silicon layer breakdown is obtained as

$$-\frac{t^2}{3t_{\rm f}}\frac{qN(L_{\rm d})}{\varepsilon_{\rm S}} \le E_{\rm S,C}. \tag{20}$$

Based on Eqs. (19) and (20), the RESURF condition of the TSL LVD device with MSFP can be expressed as

$$-\frac{\varepsilon_{\rm S}E_{\rm S,C}}{q\left(\dfrac{t^2}{3t_{\rm f}t_{\rm S}}\right)} \le N(L_{\rm d})t_{\rm S} \le \frac{\varepsilon_{\rm S}E_{\rm S,C}}{q\left(1 - \dfrac{t^2}{3t_{\rm f}t_{\rm S}}\right)}. \tag{21}$$

When the device has no field plate, the relationship becomes $E_{\rm S,C}(\times 10^5$ V/cm) and $N_{\rm d}({\rm cm}^{-3})E_{\rm S,C}$ becomes

$$N(L_{\rm d})t_{\rm S} = \frac{\varepsilon_{\rm S}(2.19 + 7.1\times 10^{-8}N_{\rm d}^{0.46})}{q}. \tag{22}$$

$E_{S,C}$ as a function of N_d and t_S in the analytic model, the conventional equation[15] and the experimental curves[16] are all shown in Fig. 2. The $E_{S,C}$ increases as N_d increases. When the N_d is quite low ($N_d < 1\times10^{17}$ cm^{-3}), these curves fit well; when $N_d \geq 1\times10^{17}$ cm^{-3}, from Eq. (18), $E_{S,C}$ of Grove's experimental data[16] and traditional results[15] are different. The values of N_d of TSL LVD are 1×10^{17} cm^{-3} and 1×10^{18} cm^{-3}, and the values of $E_{S,C}$ are 68.8 V/μm and 157.2 V/μm, respectively, which are greater than that of the traditional structure (about 30 V/μm). The experimental result of Grove[16] is consistent with that obtained from the analytical model. The dependences of N_d on $E_{S,C}$ in Eqs. (19) and (20) are suitable for the analysis of the thin silicon layer and the high doping drift region concentration under the drain.

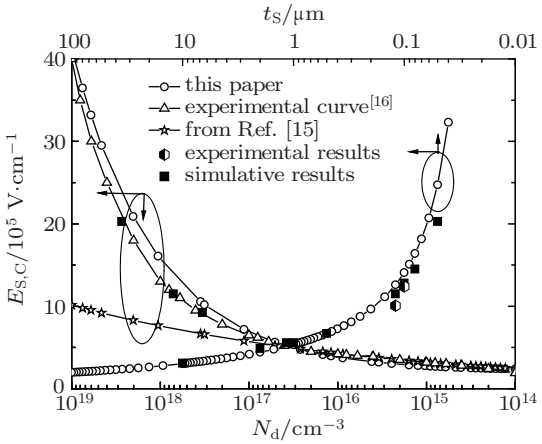


Fig. 2. Variations of $E_{S,C}$ with N_d and t_S.

Based on Eqs. (15) and (19), the $V_{B,V}$ of the thin silicon layer SOI device at the interface breakdown can be obtained as

$$V_{B,V} = \frac{1}{2}\left(\frac{qN(L_d)}{\varepsilon_S}t_S - \frac{\varepsilon_I}{\varepsilon_S t_f}\frac{qN(L_d)}{\varepsilon_S}t^2\right)t_S + 3t_I\left(\frac{qN(L_d)}{\varepsilon_S}t_S - \frac{\varepsilon_I}{\varepsilon_S t_f}\frac{qN(L_d)}{\varepsilon_S}t^2\right). \quad (23)$$

When the silicon layer becomes thinner, the value of $E_{S,C}$ increases, which enhances the buried oxide electric field and the BV. The doping concentration of the drift region cannot be too high to be depleted. The breakdown voltage is more sensitive to $N(x)$, therefore, the appropriate thin silicon layer thickness and the maximum drift region concentration are keys to the design of the device.

3. Results and discussion

The window size and spacing of impurity implantation are shown in Fig. 3(a). The widths of an injected cell of X_i plus Y_i are the same for different values of i, which is used in the design of the LVD (X is the window size of the impurity implantation, Y is the length of the masking photoresist). The window size of impurity implantation increases from the source to the drain and the length of the masking photoresist decreases from the source to the drain gradually.

The device profile structure after 10 hour thermal oxidation by the process simulation software TSUPREM4 is shown in Fig. 3(b). The top silicon layer thickness is thinned from 1.5 μm to 0.26 μm.

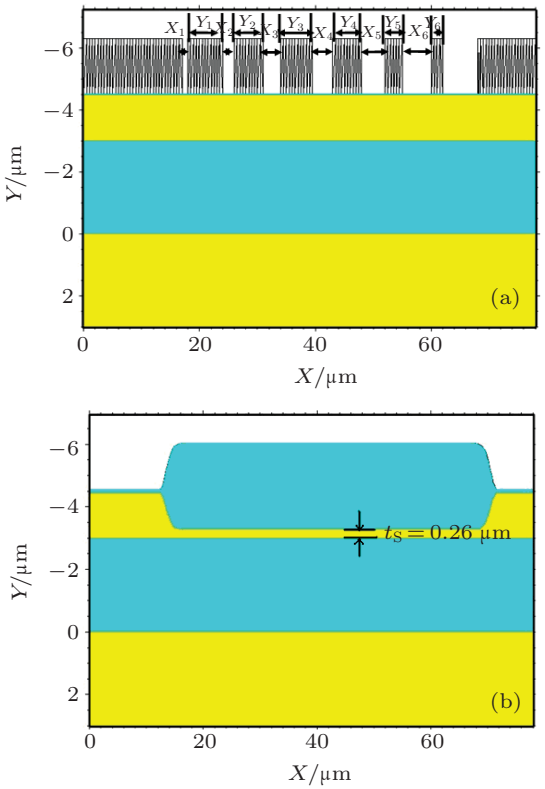


Fig. 3. (colour online) The implantation window and the thickness of the silicon layer after 10 hour thermal oxidation. Panel (a) shows the implantation window for linear variable doping, and panel (b) exhibits the device profile structure after 10 hour thermal oxidation.

Figure 4(a) shows the impurity concentration distribution in the drift region with different high temperature oxidation and drive-in time. When the dose of phosphorus implantation is 2×10^{13} cm^{-2} in the drift region, the average impurity concentration increases as oxidation time increases. After the 28 hour high temperature oxidation and drive-in, the distribution of the drift region is nearly linear. Figure 4(b) shows the thickness of the silicon layer varying with

high temperature oxidation time.

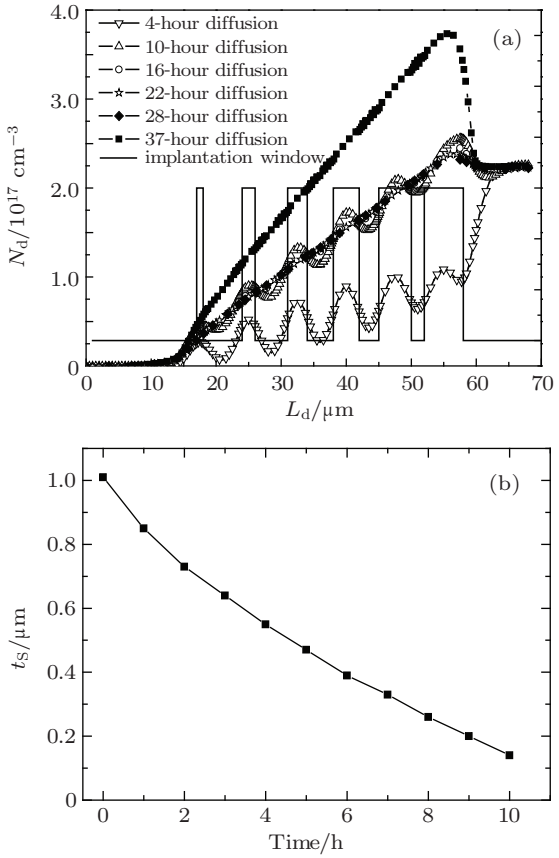


Fig. 4. (a) Impurity concentration distributions in the drift region for different high temperature oxidation and drive-in times, and (b) the thickness of the top silicon layer varying with high temperature oxidation time.

Figure 5(a) shows the critical electric field of the silicon layer and breakdown voltage each as a function of the thickness of the thin silicon layer. The thickness of the silicon layer is reduced to make the BV and the $E_{S,C}$ increase. The simulations of $E_{S,C}$ and the experimental results from Ref. [8] of $E_{S,C}$ are in good agreement. The silicon critical electric field reaches 99.6 V/μm when the thickness of the silicon layer is 0.14 μm.

Figure 5(b) shows the vertical electric field distributions under the drain electrode with different values of t_S when t_I is 3 μm. The electric field of the buried layer increases as the thickness of the silicon layer decreases. The improvement of the critical breakdown electric field of the silicon layer increases with the electric field of the buried layer. The LVD technology can optimize the lateral electric field distribution and increase the value of BV, and at the same time the higher concentration of the LVD drift region with field plates can be depleted. When the thickness of the silicon layer is 0.14 μm, the critical electric field of the top silicon layer and the dielectric layer reach 99.6 V/μm and 336 V/μm, respectively.

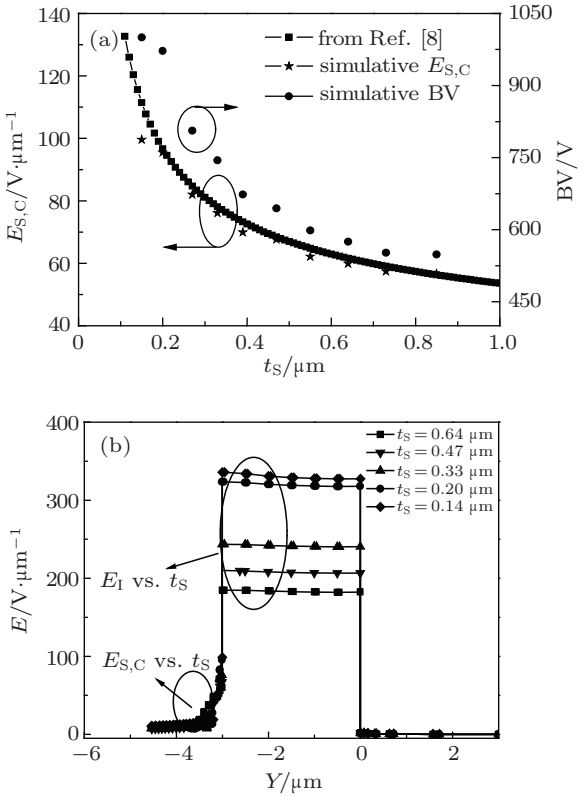


Fig. 5. (a) The critical electric field of the silicon layer and the BV, each as a function of t_S, and (b) the vertical electric field distributions for different values of t_S.

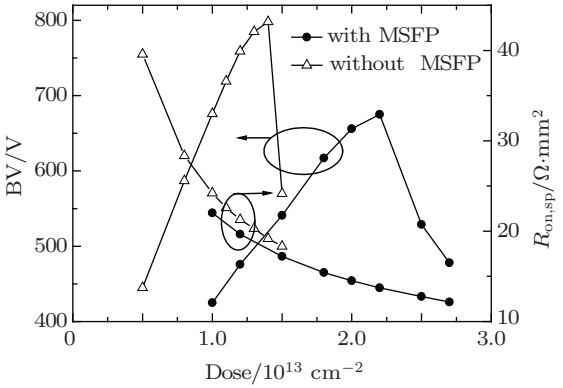


Fig. 6. Values of BV and $R_{on,sp}$ each as a function of the implantation dose of the drift region with MSFP and without MSFP for a drift region length of 50 μm.

Figure 6 shows the values of BV and $R_{on,sp}$ each as a function of the implantation dose of the drift region with and without MSFP for a drift region length of 50 μm. The maximum voltage of the device is 798 V and $R_{on,sp}$ is 19.0 Ω·mm^2 without MSFP and HVI. The MSFP which includes the source field plate and the gate field plate is designed, and the maximum voltage is reduced to 675 V and $R_{on,sp}$ is dropped to

13.7 Ω·mm^2. The $R_{on,sp}$ is reduced because the gate poly field plate and the source metal field plate assist the depletion of the drift region, so the doping concentration of the drift region can be increased. The trade-off between BV and $R_{on,sp}$ can be improved.

HVI will disturb the uniform surface potential distribution of the device and the BV is reduced. MSFP is introduced to relax the high electric field at the source side caused by HVI. Figure 7(a) gives the equipotential line distribution without MSFP and HVI. The equipotential line distribution is uniform and BV is 798 V due to the lack of HVI. Figure 7(b) gives an equipotential line distribution with MSFP and HVI. The equipotential lines are locally focused at the source end by the influence of HVI. The device has a premature avalanche breakdown when the drift region is not fully depleted. The breakdown voltage of the device is reduced to 343 V. The breakdown voltage is reduced by 57% compared with that of the device without HVI. Figures 7(c) and 7(d) show the equipotential line distribution with MSFP and with or without HVI, respectively. The equipotential lines focus at the end of the source metal field plate and the BV is 675 V without HVI. When HVI crosses over the surface of nLDMOS, the equipotential lines remain focused on the source metal field plate end and the BV is 673 V. Therefore, the MSFP is very useful for reducing the influence of HVI on the breakdown characteristics of the TSL LVD device.

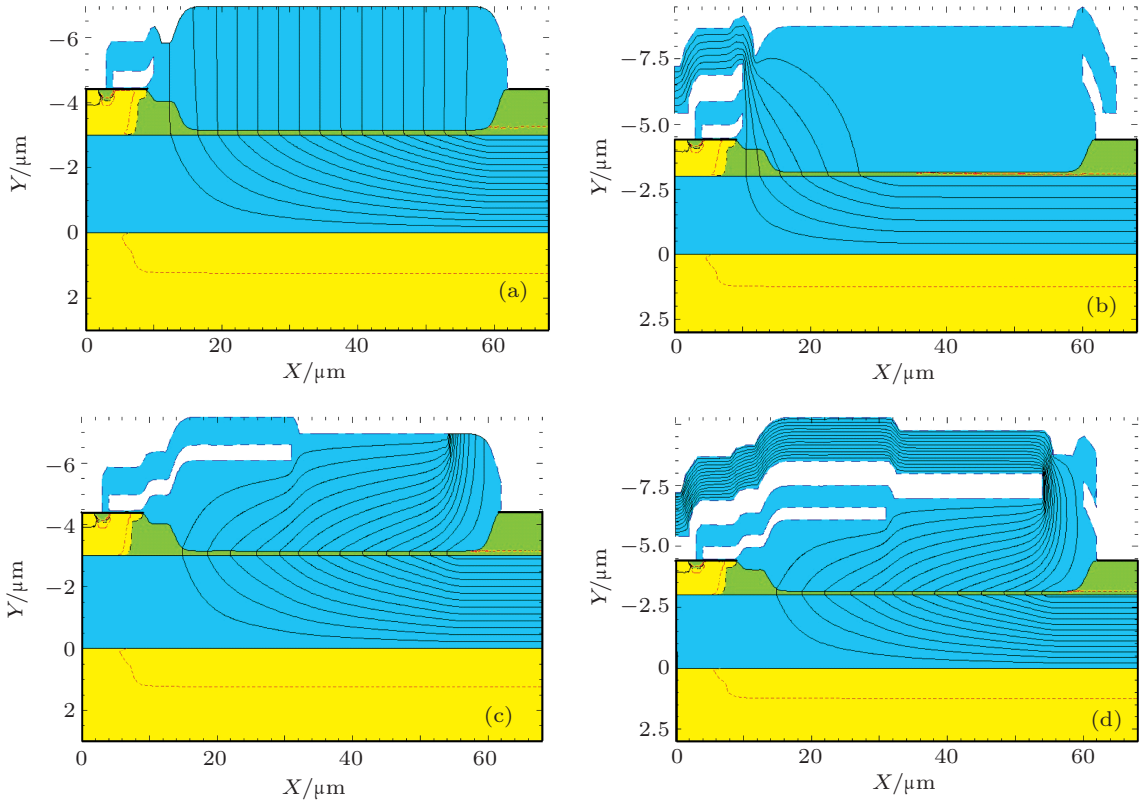


Fig. 7. (colour online) Equipotential line distributions in the following cases: (a) Without HVI and MSFP, (b) with HVI and without MSFP, (c) without HVI and with MSFP, (d) with HVI and MSFP.

Figure 8 shows the values of BV and $R_{on,sp}$ each as a function of the impurity implantation dose of the drift region with different drift region lengths for the LVD nLDMOS with MSFP. When the length of the drift region is 40 μm, due to the smaller drift region length, the drift region is easy to deplete, and the breakdown voltage is 496 V which is limited by the lateral sustain voltage. When the lengths of the drift region are 50 μm and 60 μm, the breakdown voltages are 675 V and 709 V, respectively. At the same time, the $R_{on,sp}$ is reduced as the implantation dose increases. When the drift region length is 60 μm, BV is 709 V and $R_{on,sp}$ is 16.8 Ω·mm^2.

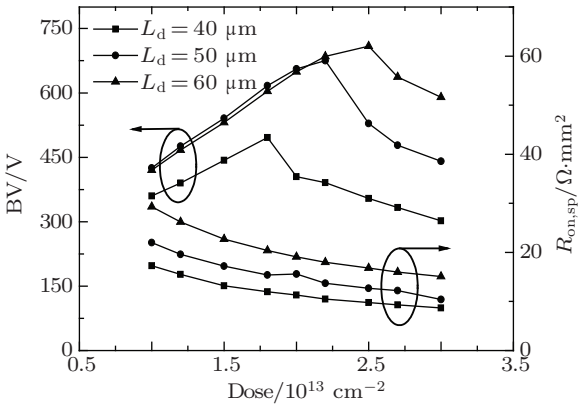


Fig. 8. Values of BV and $R_{on,sp}$ each as a function of the impurity implantation dose of the drift region with different lengths of the drift region for the LVD with MSFP.

Figure 9(a) shows the layout of TSL LVD SOI nLDMOS with HVI. The drain is designed in the centre and the source is in the peripheral of the layout. Figure 9(b) shows the SEM image of the device, and the interdigitated structure, which can increase the width of the device to meet the applied high voltage and large working current, is used. Figure 9(c) shows the cross-sectional SEM image of the device, where t_S is 0.14 μm by design and the experimental thickness is 0.15 μm, t_f is 0.8 μm, and the experimental thickness is 0.797 μm. The experimental results and the simulation results are consistent.

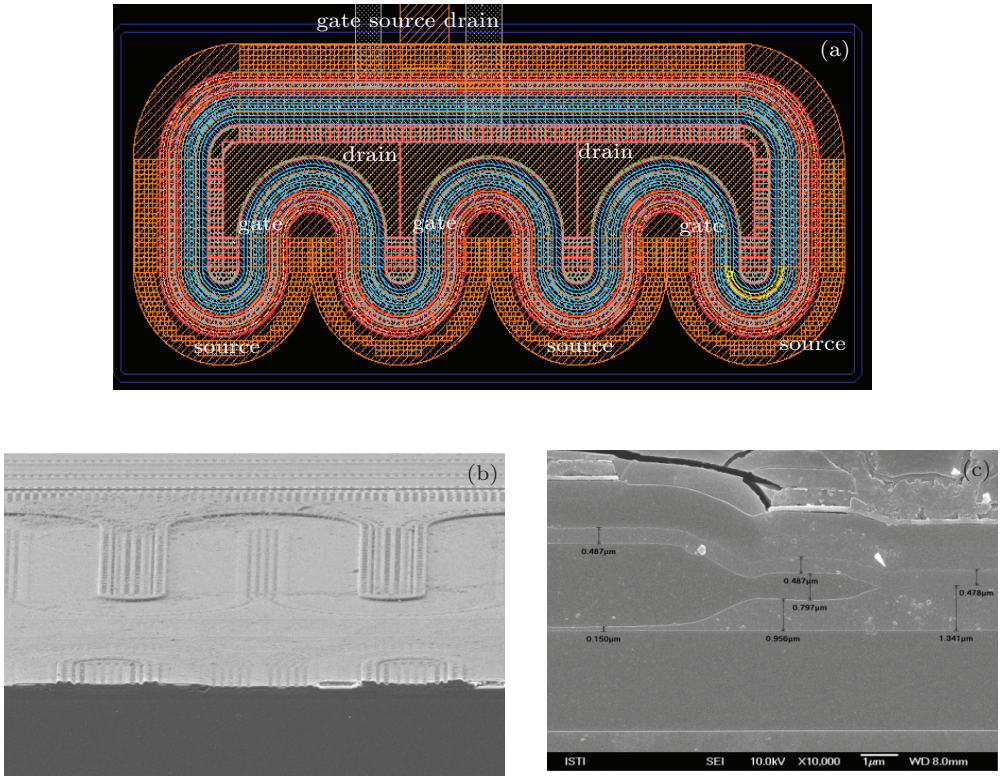


Fig. 9. (colour online) (a) The layout of the TSL LVD nLDMOS, (b) SEM image of the TSL LVD nLDMOS, and (c) cross-sectional SEM image of the TSL LVD nLDMOS.

Figure 10 shows the measured off-state breakdown characteristics, output characteristics, and transfer characteristics of TSL LVD nLDMOS with MSFP at a drift region length of 60 μm. Figure 10(a) shows the off-state breakdown characteristics, where the BV is 694 V with t_I of 3 μm, therefore E_I is over 200 V/μm. Figure 10(b) shows the measured output characteristics of the device. When the gate voltage is 9 V, the $R_{on,sp}$ of the device is 21.3 Ω·mm^2. As the gate voltage increases, the on-state current of the device increases. The saturated current of the device is reduced with the increase of drain voltage due to the self-heating effect (SHE). Figure 10(c) shows the measured transfer characteristics. The drain currents as a function of gate voltage are tested with drain voltages of 0.1 V, 5 V, and 9 V.

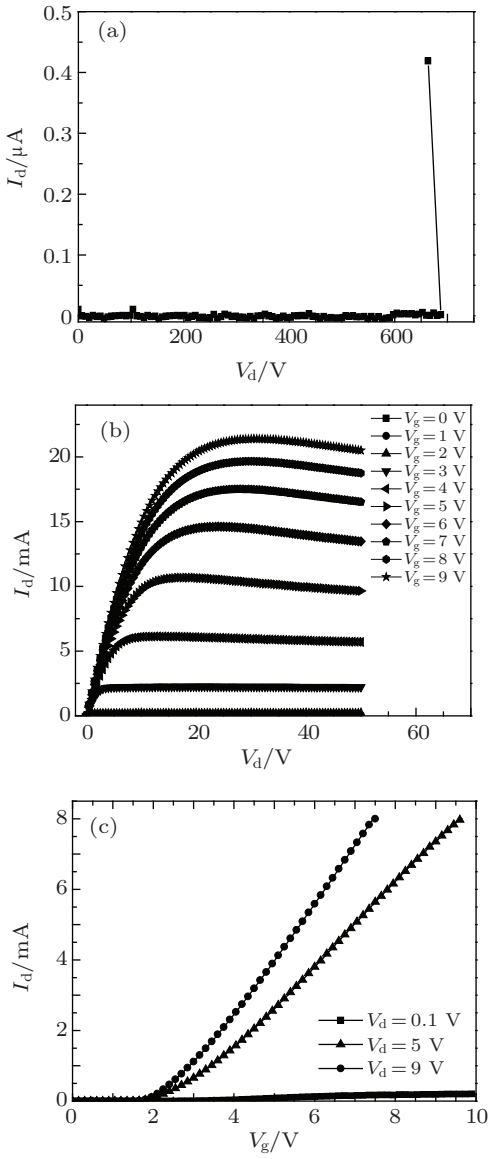


Fig. 10. Measured characteristic curves of the TSL LVD nLDMOS with MSFP, showing (a) the off-state breakdown characteristics, (b) the output characteristics, and (c) the transfer characteristics.

4. Conclusions

Based on the discussion of the TSL LVD high voltage nLDMOS with MSFP, the breakdown voltage model is deducted and the simulation results fit well with the analytical results. The relationship between the critical breakdown electric field of the thin silicon layer and the thickness of the silicon layer for a TSL LVD device with MSFP is studied. It is shown that in experiments with a drift region length of 60 μm, buried oxide layer thickness of 3 μm, and silicon layer thickness of 0.15 μm, the BV is 694 V, $R_{\rm on,sp}$ is 21.3 Ω·mm^2 and $E_{\rm I}$ is over 200 V/μm.

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