The breakdown mechanism of a high-side pLDMOS based on a thin-layer silicon-on-insulator structure*

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A high-side thin-layer silicon-on-insulator (SOI) pLDMOS is proposed, adopting field implant (FI) and multiple field plate (MFP) technologies. The breakdown mechanisms of back gate (BG) turn-on, surface channel punch-through, and vertical and lateral avalanche breakdown are investigated by setting up analytical models, simulating related parameters and verifying experimentally. The device structure is optimized based on the above research. The shallow junction achieved through FI technology attenuates the BG effect, the optimized channel length eliminates the surface channel punch-through, the advised thickness of the buried oxide dispels the vertical avalanche breakdown, and the MFP technology avoids premature lateral avalanche breakdown by modulating the electric field distribution. Finally, for the first time, a 300 V high-side pLDMOS is experimentally realized on a 1.5 μm thick thin-layer SOI.

Keywords: field implant technology, back gate punch-through, surface channel punch-through, avalanche breakdown

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1. Introduction

The silicon-on-insulator (SOI) has attracted tremendous interest in smart power integrated circuits for its super isolation, high speed, low power loss and small isolation area compared with the self-isolation and junction-isolation processes.[1−7] The thin-layer SOI is superior to the thick-layer one due to its better process compatibility and lower parasitic effects, such as kink, latch breakdown, self-heating and the hot-carrier degradation effect.[8−11] However, for a thin-layer SOI pLDMOS at high side operation, the device and handler wafer biasing causes an accumulation in the drift region, leading to a reduced breakdown voltage (BV) compared with that of the nLDMOS based on the double reduced surface field action. Meanwhile, the body region suffers from a depletion, which induces the back gate (BG) punch-through.[12−18] So far, the highest breakdown voltage reported for the high-side thin-layer SOI pLDMOS is 150 V.[19] The thick gate oxide pLDMOS is widely used in various drive circuits to simplify the circuit design and reduce fabrication process steps.[20−21] However, the top silicon thinning caused by the thick gate oxide makes the BG effect more severe for the thin-layer SOI pLDMOS.

In this paper, a novel pLDMOS structure is presented, which adopts multiple field plate (MFP) and field implant (FI) technologies. Both lateral and vertical breakdown mechanisms are investigated by setting up analytical models, simulating and verifying experimentally. The simulation and experimental results show good consistency with the theoretical analysis, and a 300 V high-side thin-layer SOI pLDMOS is made on a 1.5 μm thick thin-layer SOI.

2. Device structure and punch-through mechanism

A high-side thick gate oxide pLDMOS based on the thin-layer SOI is proposed, and is shown in Fig. 1(a). The thick gate oxide is replaced directly with a 500 nm thick field oxide to realize a high level shift between the source and the gate. The MFP enhances the depletion of the p-drift and modulates the surface electric field distribution, avoiding the premature breakdown resulting from the electric field concentration at the source side. The FI technology is used not only to eliminate channel discontinuity in

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the bird's beak, but also to achieve a shallow p-field that prevents premature BG punch-through, as shown in Fig. 1(b).

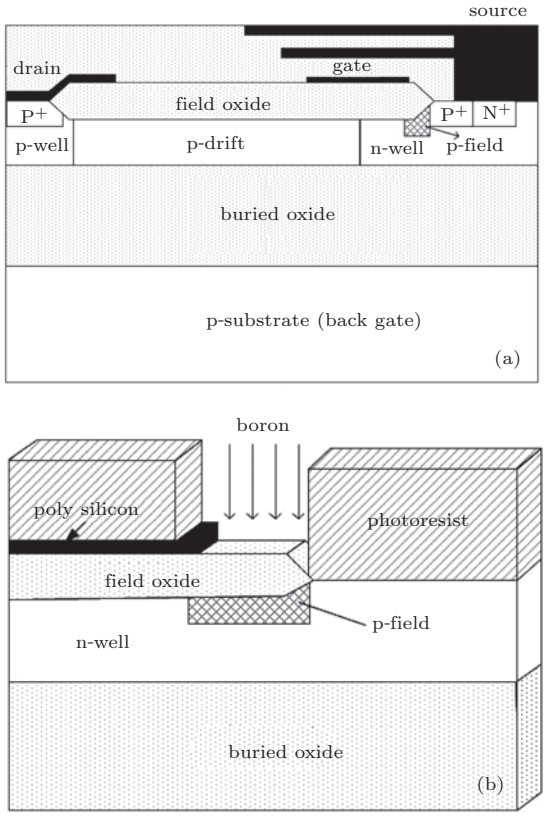


Fig. 1. (a) A schematic cross-sectional view of pLDMOS, and (b) the schematic principle of FI technology.

Figure 2 shows a schematic diagram of the back and surface channel punch-through, with some of the parameters given. When the pLDMOS is in the off state, the n-well is depleted over the buried oxide and beside the p-drift. The positive space charge region creates and forms the back and surface channel. The depletion layer spreads to the p-field vertically and laterally as $V_{\rm s}$ increases. When the depletion layer vertically attacks the built-in barrier of the p-field and n-well junction, BG punch-through occurs; when it attacks laterally, surface channel punch-through occurs. The BG punch-through is described by

$$w_{\rm v} = -\frac{\varepsilon_{\rm s} t_{\rm i}}{\varepsilon_{\rm i}} + \sqrt{\left(\frac{\varepsilon_{\rm s} t_{\rm i}}{\varepsilon_{\rm i}}\right)^2 + \frac{2\varepsilon_{\rm s}}{qN_{\rm n-well}} V_{\rm s}} + \sqrt{\frac{2\varepsilon_{\rm s}}{qN_{\rm n-well}} V_{\rm bi}} \geq t_{\rm s} - t_{\rm p-field}, \quad (1)$$

and the surface channel punch-through is described by

$$w_{\rm l} = \frac{\varepsilon_{\rm s}}{qN_{\rm n-well}} \sqrt{\frac{2qN_{\rm n-well}N_{\rm p-drift}}{\varepsilon_{\rm s}\left(N_{\rm n-well} + N_{\rm p-drift}\right)}\left(V_{\rm bi} + V_{\rm s}\right)} + \sqrt{\frac{2\varepsilon_{\rm s}}{qN_{\rm n-well}} V_{\rm bi}} \geq w_{\rm channel}, \quad (2)$$

where $w_{\rm v}$ represents the vertical depletion length; $w_{\rm l}$ describes the lateral depletion length; $\varepsilon_{\rm s}$ and $\varepsilon_{\rm i}$ are the dielectric constants of silicon and silicon dioxide, respectively; $N_{\rm n-well}$ and $N_{\rm p-drift}$ are the doping concentrations of the n-well and the p-drift, respectively; $V_{\rm bi}$ is the built-in potential of the p-field and n-well junction; and $\sqrt{\frac{2\varepsilon_{\rm s}}{qN_{\rm n-well}} V_{\rm bi}}$ is the depletion region length of the p-field and n-well junction.

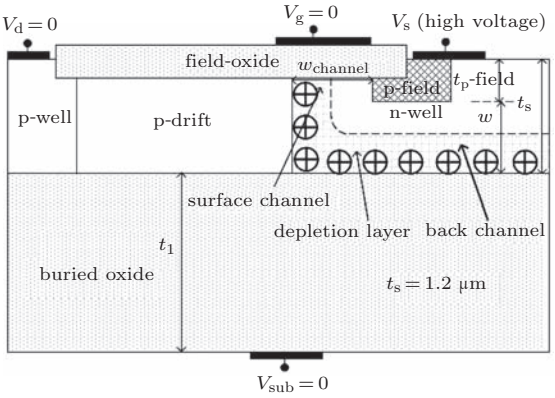


Fig. 2. Schematic diagram of back and surface channel punch-through.

3. Theoretical analysis and discussion

The contribution of $t_{\rm p-field}$ to the breakdown voltage simulated by MEDICI is shown in Fig. 3(a). For the convenience of simulation, $V_{\rm s}$ and $V_{\rm g}$ are set to be 0 V; $V_{\rm s}$ and $V_{\rm sub}$ are applied with negative voltages. In this paper, the dash arrowhead indicates the corresponding coordinate, the solid arrowhead indicates the breakdown mechanism, and the critical value is marked with dashed beelines. The back gate punch-through can be avoided when $t_{\rm p-field} \leq 0.4$ μm. When $t_{\rm p-field} \geq 1.0$ μm, the BV is a constant and equal to the back gate threshold voltage. The $w_{\rm v}$ as an analytic function of $N_{\rm n-well}$ is also shown in Fig. 3(a). When $N_{\rm n-well}$ is 3×10^{16} cm^{-3}, $w_{\rm v}$ is equal to 0.88 μm, so the analytic critical $t_{\rm p-field}$ is equal to 0.32 μm, as calculated from Eq. (1).

FI technology is used to form the shallow p-field in the source side by injecting through the thick field oxide, and the depth of the p-field is controlled by the FI energy, as shown in Fig. 3(b). The boron cannot penetrate through the 500 nm thick field oxide until

the FI energy is larger than 125 keV. Because of the compensation between donors and acceptors, $t_{\mathrm{p-field}}$ decreases with the addition of $N_{\mathrm{n-well}}$ for the same FI energy.

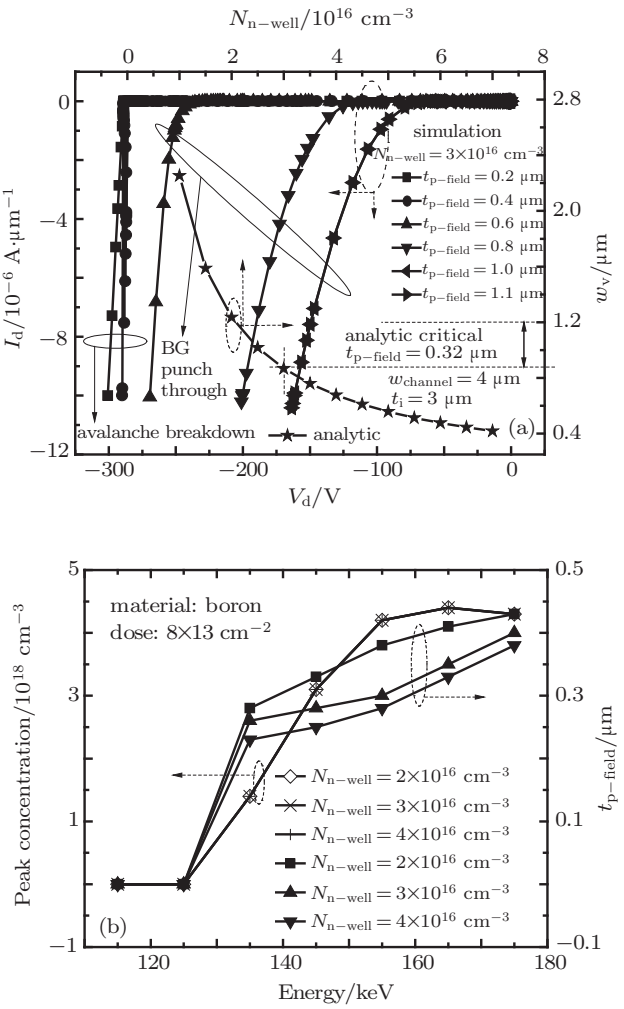


Fig. 3. (a) Simulated drain current to drain voltage characteristics of pLDMOS for different $t_{\mathrm{p-field}}$ ($N_{\mathrm{n-well}} = 3 \times 10^{16}$ cm^{-3}), and w_{v} as an analytical function of $N_{\mathrm{n-well}}$. (b) The peak concentration and depth of the p-field as a function of implanting energy for different $N_{\mathrm{n-well}}$.

Figure 4(a) shows the simulated BV depending on t_{i} for different $t_{\mathrm{p-field}}$ together with w_{v} as an analytic function of t_{i}. With the modulation of the MFP, a lateral avalanche breakdown point appears at the interface of the n-well and p-drift junction, as shown in Fig. 4(b). When $t_{\mathrm{p-field}}$ is above 0.4 μm, the simulated critical t_{i} is 3 μm and 5 μm. The thin buried oxide accelerates the depletion of the n-well, which then undertakes the added vertical voltage and thus induces BG punch-through, as shown in Fig. 4(c). When $t_{\mathrm{p-field}}$ is 0.2 μm, the simulated critical t_{i} is 2.5 μm. The thin buried oxide layer leads to vertical avalanche breakdown and the vertical voltage supported by the buried oxide decreases, as shown in Fig. 4(d).

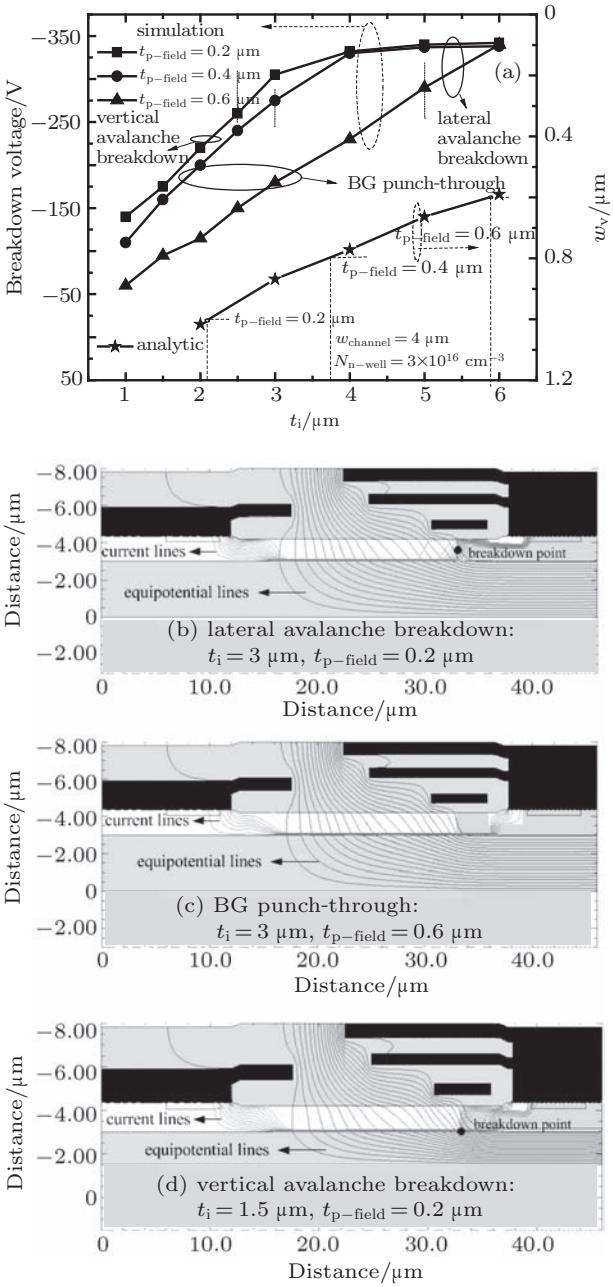


Fig. 4. (a) Simulated breakdown voltage as a function of t_{i} for different $t_{\mathrm{p-field}}$, and w_{v} as an analytical function of t_{i}. (b)–(d) Current lines and potential distributions of pLDMOS; the potential difference between the two lines is equal to 10 V.

Figure 5(a) shows the simulated BV as a function of $N_{\mathrm{n-well}}$ for different $t_{\mathrm{p-field}}$, together with w_{v} as an analytical function of $N_{\mathrm{n-well}}$. The simulated critical $N_{\mathrm{n-well}}$ is 3×10^{16} cm^{-3}, 3.5×10^{16} cm^{-3} and 4×10^{16} cm^{-3} for $t_{\mathrm{p-field}}$ of 0.2, 0.4 and 0.6 μm, respectively. Figure 5(b) shows the simulated BV as a function of $N_{\mathrm{n-well}}$ for different t_{i}, and the analytical critical $N_{\mathrm{n-well}}$ depending on t_{i}. The simulated

critical $N_{\mathrm{n-well}}$ is 3×10^{16} cm^{-3}, 3.5×10^{16} cm^{-3}, and 4×10^{16} cm^{-3} for t_{i} of 2, 3 and 4 μm, respectively. The avalanche breakdown occurs at the interface of the n-well and the p-drift junction when $N_{\mathrm{n-well}}$ is above the critical value and the peak electric field

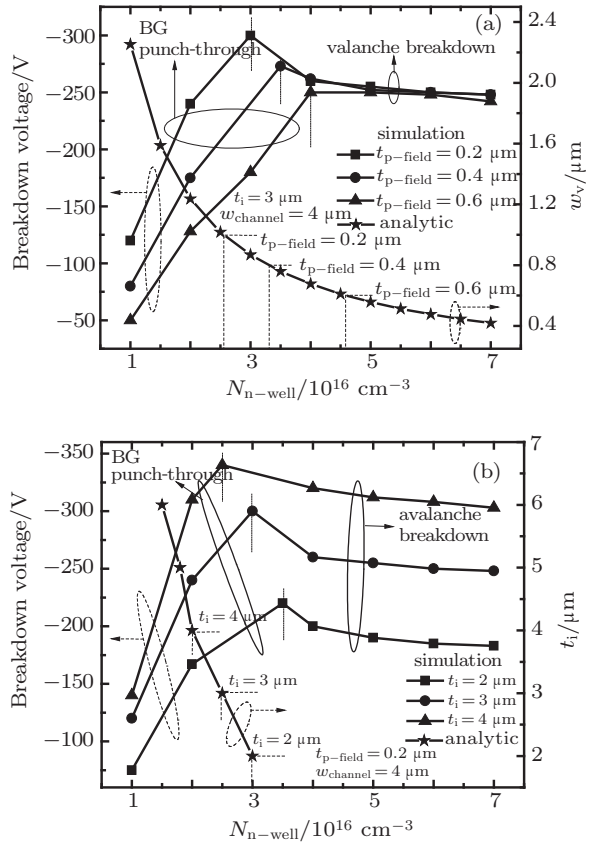


Fig. 5. Breakdown voltage as a function of $N_{\mathrm{n-well}}$, (a) for different $t_{\mathrm{p-field}}$ and w_{v} as an analytical function of $N_{\mathrm{n-well}}$, and (b) for different t_{i} and analytical critical $N_{\mathrm{n-well}}$ depending on t_{i}.

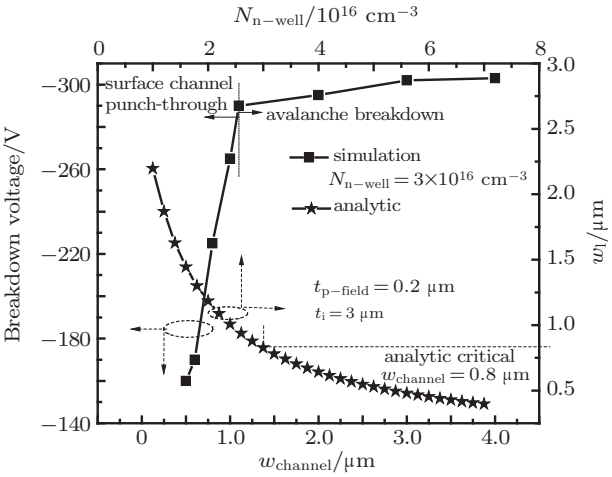


Fig. 6. The simulated breakdown voltage as a function of w_{channel} ($N_{\mathrm{n-well}}=3\times10^{16}$ cm^{-3}) and w_{l} as an analytical function of $N_{\mathrm{n-well}}$.

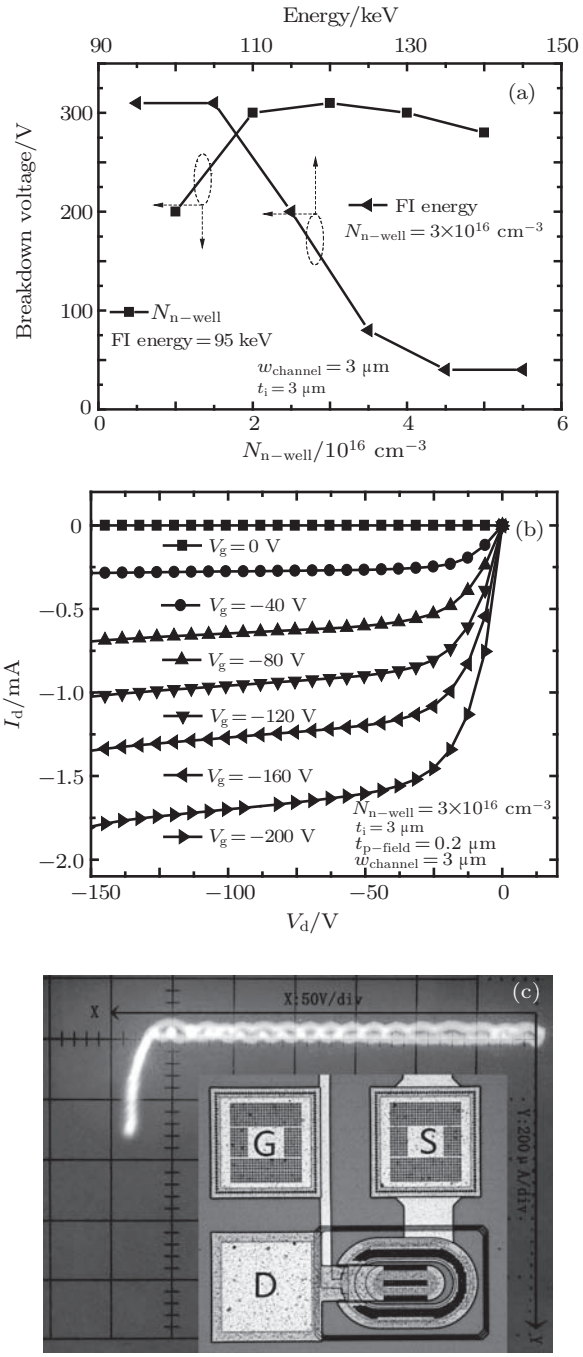


Fig. 7. The experimental pLDMOS results: (a) the breakdown voltage as a function of $N_{\mathrm{n-well}}$ and FI energy; (b) the on-state characteristics; and (c) the off-state characteristics and a microphotograph.

value can be expressed as

$$|E_{\max}|=\left[\frac{2q}{\varepsilon_{\mathrm{s}}}\left(\frac{N_{\mathrm{n-well}}N_{\mathrm{p-drift}}}{N_{\mathrm{n-well}}+N_{\mathrm{p-drift}}}\right)(V_{\mathrm{bi}}+V_{\mathrm{s}})\right]. \quad (3)$$

The BV decreases with the addition of $N_{\mathrm{n-well}}$ that results from the increased peak electric field. The back gate punch-through occurs when $N_{\mathrm{n-well}}$ is below the critical value. The critical $N_{\mathrm{n-well}}$ increases with the increase in $t_{\mathrm{p-field}}$ and the decrease in t_{i}.

A smaller $t_{\rm i}$ accelerates the vertical depletion and a larger $t_{\rm p-field}$ decreases the depletion length.

Figure 6 shows the simulated BV as a function of $w_{\rm channel}$ and $w_{\rm l}$ as an analytical function of $N_{\rm n-well}$. The depletion layer mainly spreads towards the lightly doped p-drift region when $N_{\rm n-well}$ is much larger than $N_{\rm n-drift}$, and the lateral punch-through does not occur until $w_{\rm channel}$ reduces to 1.1 μm in the simulation. The charge shares in the region deplete both laterally and vertically.[22] In other words, the vertical depletion can accelerate the lateral depletion and make the surface channel punch-through occur more easily.

Figure 7(a) shows the experimental BV as a function of $N_{\rm n-well}$ and the FI energy. As the thick gate oxide is out of flatness at the bird's beak, an FI energy of 95 keV is enough to achieve the shallow p-field that avoids BG punch-through. An optimized 300 V pLDMOS is achieved when $N_{\rm nwell}$ is 3×10^{16} cm^{-3}, $t_{\rm i}$ is 3 μm and $t_{\rm p-field}$ is less than 0.4 μm. Its on-state characteristics are shown in Fig. 7(b), and its off-state characteristics and a microphotograph are shown in Fig. 7(c).

4. Conclusion

It is difficult to achieve high BV in a high-side thin-layer SOI pLDMOS for two reasons: the device and handler wafer biasing causes an accumulation in the drift region; and the body region suffers from a depletion, which induces BG punch-through. In this paper, MFP is adopted to enhance the depletion of the p-drift, and FI technology is proposed to attenuate the BG effect. The breakdown mechanisms of the punch-through and the avalanche breakdown are investigated by setting up analytical models. The device off-state characteristics can be improved by optimizing critical parameters such as $t_{\rm p-field}$, $N_{\rm n-well}$, $t_{\rm i}$ and $w_{\rm channel}$. The simulation and experimental results show good consistency with the theoretical analysis. A 300 V high side field pLDMOS is achieved on a 1.5 μm thick SOI layer, which is a 100% improvement compared with the conventional pLDMOS.

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