Effects of gate-buffer combined with a p-type spacer structure on silicon carbide metal–semiconductor field-effect transistors*

Song Kun(宋 坤)†, Chai Chang-Chun(柴常春), Yang Yin-Tang(杨银堂), Chen Bin(陈 斌), Zhang Xian-Jun(张现军), and Ma Zhen-Yang(马振洋)

Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices of Ministry of Education, School of Microelectronics, Xidian University, Xi'an 710071, *China*

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An improved structure of silicon carbide metal–semiconductor field-effect transistors (MESFET) is proposed for high power microwave applications. Numerical models for the physical and electrical mechanisms of the device are presented, and the static and dynamic electrical performances are analysed. By comparison with the conventional structure, the proposed structure exhibits a superior frequency response while possessing better DC characteristics. A p-type spacer layer, inserted between the oxide and the channel, is shown to suppress the surface trap effect and improve the distribution of the electric field at the gate edge. Meanwhile, a lightly doped n-type buffer layer under the gate reduces depletion in the channel, resulting in an increase in the output current and a reduction in the gate-capacitance. The structural parameter dependences of the device performance are discussed, and an optimized design is obtained. The results show that the maximum saturation current density of 325 mA/mm is yielded, compared with 182 mA/mm for conventional MESFETs under the condition that the breakdown voltage of the proposed MESFET is larger than that of the conventional MESFET, leading to an increase of 79% in the output power density. In addition, improvements of 27% cut-off frequency and 28% maximum oscillation frequency are achieved compared with a conventional MESFET, respectively.

Keywords: silicon carbide, metal–semiconductor field-effect transistor, p-type spacer, gate-buffer

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1. Introduction

Silicon carbide (SiC) has been widely investigated for its excellent properties such as a wide bandgap, high electron saturation drift velocity, high critical electric field and high thermal conductivity.[1] As wireless communication develops rapidly, there are increasing demands for high power and high frequency applications. Metal–semiconductor field-effect transistors (MESFETs) based on SiC have received increasing attention as a promising candidate for these applications.[2] In recent years, how to realize a high output power density in high frequency operation has become a hot research topic. Like MESFETs based on gallium arsenide (GaAs), SiC MESFETs suffer from a severe surface trapping problem, which causes degradation of device performance.[3−5] Studies on this issue have been carried out from various aspects.[6−17]

Besides theoretical studies, a number of experimental investigations have been performed to develop SiC MESFETs with superior performance. Different types of oxide materials have been grown to improve surface properties.[18] The density of interface states cannot be reduced fundamentally. A buried gate is a proven solution to result in less trapping, leading to less frequency dispersion and a reduction in current instability.[19] In S-band operation, a buried channel approach has been proved to give a favourable gate-lag ratio under a small working bias.[20] However, the lightly doped spacer layer turns out to be of n-type, which leads to an unwanted parasitic effect. A field plate (FP) applied to a SiC MESFET suppresses surface trap effects.[21] Unfortunately, the FP increases the effective gate length, which results in extra depletion in the conductive channel.[22] A source-connected FP eliminates the extra capacitance induced by the gate-FP at the cost of adding to layout complexity.[23] A p-buffer layer with a stepped shape has been proposed, and the simulated results show that the prop-

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†Corresponding author. E-mail: sk88205853@sina.com

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erties are improved.[24] However, during the fabrication of a SiC MESFET, each process starts from the top of the multi-epitaxial layers which have already been grown with specific conductive types and parameters, thus the shape of p-buffer layer can hardly be achieved.

In this work, an improved structure is proposed based on the theories of the device and process. To totally isolate the channel from the interface states, a p-type spacer layer is inserted between the oxide and the channel, which leads to an increase in the gate-lag ratio in high frequency operation. On the other hand, an n-type buffer layer is introduced under the gate electrode to reduce depletion in the channel, which results in a larger drain–source current $I_{\rm ds}$. Furthermore, due to the existence of the n-type gate-buffer layer, the total depletion thickness under the gate is increased. Therefore, the gate capacitance $C_{\rm g}$ is reduced and a better frequency response is obtained. In order to make this work possess practical meaning, the physical models for SiC material properties and numerical models for MESFET mechanisms are integrated in our simulation. Direct current (DC), breakdown and alternating current (AC) characteristics have been investigated and the results show that the performance of the proposed MESFET is totally enhanced compared with that of a conventional MESFET.

2. Methodology

2.1. Device structure and parameters

Figure 1 shows the schematic cross-section of a SiC MESFET with the proposed structure. A p-type layer is inserted between the n-type conductive channel layer and the oxide to isolate the channel from surface traps. In addition, an n-type buffer layer is introduced under the gate to reduce depletion in the channel below. To meet the demand for high frequency (up to X band) applications, the gate length of the device is designed to be 0.5 μm.

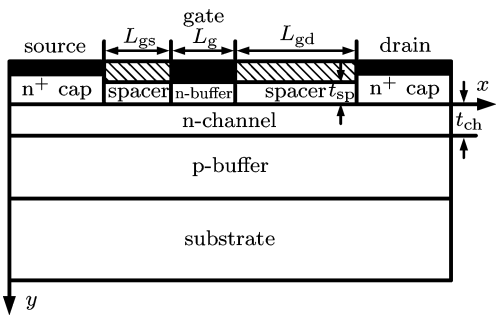


Fig. 1. Schematic cross-section of a SiC MESFET with the proposed structure. $L_{\rm gs}$, $L_{\rm g}$, and $L_{\rm gd}$ are the gate-to-source length, gate length, and gate-to-drain length, respectively; $t_{\rm sp}$ and $t_{\rm ch}$ are the p-spacer layer thickness and channel thickness, respectively.

The detailed parameters of the proposed structure are listed in Table 1, where $t_{\rm gb}$ is the gate-buffer layer thickness.

Table 1. Device structural parameters.

Device parameter	Dimension and value
n^+ source/drain doping/cm^{-3}	1×10^{19}
n-channel doping/cm^{-3}	2×10^{17}
p-buffer doping/cm^{-3}	4.5×10^{15}
p-spacer layer doping/cm^{-3}	5×10^{15}
gate-buffer layer doping/cm^{-3}	1×10^{16}
$L_{\rm g}$/μm	0.5
$L_{\rm gs}/L_{\rm gd}$/(μm/μm)	0.5/1
$t_{\rm ch}$/μm	0.2
$t_{\rm sp}$/nm	75
$t_{\rm gb}$/nm	75

2.2. Physical models

2.2.1. Mobility and velocity-field dependence

At low electric fields, the widely used empirical model for electron mobility is given by[25]

$$\mu_0 = \mu_{\rm min} + \frac{\mu_{\rm max} - \mu_{\rm min}}{1 + \left(N_{\rm D}^+/N_{\rm ref}\right)^{\alpha}}, \tag{1}$$

where $N_{\rm D}^+$ is the ionized impurity concentration and $\mu_{\rm max}$, $\mu_{\rm min}$, $N_{\rm ref}$, α are fitting parameters.

To describe the electron mobility as a function of electric field $\mu(E) = \nu(E)/E$, a multi-parameter model developed for wide-gap semiconductors is used as[26]

$$\nu(E) = \frac{\mu_1 E + \mu_0 E\left(E/E_0\right)^{\theta} + V_{\rm sat}\left(E/E_1\right)^{\eta}}{1 + \left(E/E_0\right)^{\theta} + \left(E/E_1\right)^{\eta}}, \tag{2}$$

where μ_1, E_0, E_1 and θ are influence factors on peak velocity, peak electric field and η is the steepness of $\nu(E)$ in the saturation region. The parameters are detailed in Ref. [26].

2.2.2. Models for Schottky contact

To discuss the gate bias dependence on device characteristics, barrier lowering at Schottky contact is taken into account. The following expression is used to compute the value of barrier lowering:

$$\Delta\Phi_{\rm B}(E) = a_1\left[\left(\frac{E}{E_0}\right)^{p_1} - \left(\frac{E_{\rm eq}}{E_0}\right)^{p_1}\right] + a_2\left[\left(\frac{E}{E_0}\right)^{p_2} - \left(\frac{E_{\rm eq}}{E_0}\right)^{p_2}\right], \tag{3}$$

where E is the electric field, $E_{\rm eq}$ is the electric field at equilibrium, E_0, a_1, p_1, a_2 and p_2 are the fitting parameters. The final value of the Schottky barrier is computed as $\Phi_{\rm B} - \Delta\Phi_{\rm B}(E)$ for n-doped contacts.

A realistic model of the tunneling process at the Schottky contact is important for correct MESFET simulations. The general expression for the tunneling current density through the barrier is given by[27]

$$J_{\rm st}(\varepsilon) = A^* T^2 \int_{\varepsilon}^{\infty} \Gamma_{\rm WKB}(r(\varepsilon')) \times \ln\left(1 + \exp\left(\frac{\varepsilon_{\rm F} - \varepsilon'}{k_{\rm B}T}\right)\right) {\rm d}\varepsilon', \quad (4)$$

where e is the carrier energy at the location r, A^* is the effective Richardson constant for free electrons, T is the carrier temperature, and $\Gamma_{\rm WKB}$ is the tunneling probability.

2.2.3. Models for impact ionization

Accurate models for impact ionization in SiC are significant for studies of the breakdown characteristics. The generating rate due to impact ionization is expressed as follows:

$$G = \frac{1}{q}\left(\alpha_{\rm n}\left|J_{\rm n}\right| + \alpha_{\rm p}\left|J_{\rm p}\right|\right), \quad (5)$$

where $\alpha_{\rm n}$ and $\alpha_{\rm p}$ are the ionization coefficients for electrons and holes, respectively.

The model proposed by Thornber[28] is used for theoretical dependence of hole ionization rate as

$$\alpha_{\rm p} = \frac{qE}{\varepsilon_{\rm i}^{\rm h}} \exp\left(-\frac{\varepsilon_{\rm i}^{\rm h}}{(qE\lambda_{\rm h})^2/e_{\rm v} + qE\lambda_{\rm h}}\right), \quad (6)$$

where $\lambda_{\rm h}$ is the mean free path for the hole, $\varepsilon_{\rm i}^{\rm h}$ is the ionization energy for the hole, and $e_{\rm v}$ is the optical phonon energy. For electrons, a modified form of Eq. (6) is used, which retains only the high field asymptotic part of Thornber's model as

$$\alpha_{\rm n} = \frac{qE}{\varepsilon_{\rm i}^{\rm e}} \left(-\frac{3\varepsilon_{\rm i}^{\rm e} e_{\rm v}}{(qE\lambda_{\rm e})^2}\right), \quad (7)$$

where $\varepsilon_{\rm i}^{\rm e}$ and $\lambda_{\rm e}$ are the corresponding parameters for electrons. All parameters used in the impact ionization models are as follows:[29] $\varepsilon_{\rm i}^{\rm e} = 10$ eV, $\varepsilon_{\rm i}^{\rm h} = 7$ eV, $\lambda_{\rm e} = 29.9$ Å, $\lambda_{\rm h} = 32.5$ Å, and $e_{\rm v} = 0.12$ eV.

3. Results and discussion

A two-dimensional simulator, Sentaurus TCAD,[30] is used in this work. The physical models discussed in Subsection 2.2 are incorporated into the simulator by modifying the default models. To obtain accurate results, some basic models describing the material properties of 4H–SiC are also taken into account, such as bandgap-narrowing for the bandgap and incomplete-ionization for the purity. Figure 2 shows the simulated I–V characteristics of a SiC MESFET with the same structure and parameters as that discussed in Ref. [31]. The simulated results are in good agreement with the measurement results. The slope in the linear region figures out the channel resistance, which determines the accuracy of material-related models. The $I_{\rm ds}$ curves under different values of gate–source voltage $V_{\rm gs}$ reveal that the models for the Schottky gate describe the extending effect of depletion under the gate well.

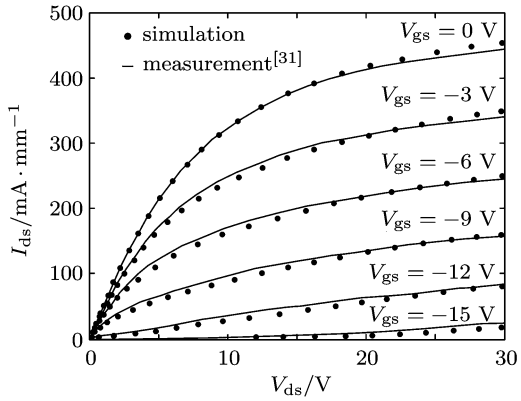


Fig. 2. Simulated I–V characteristics and the experimental data included for comparison.

Although the p-type spacer inserted between the oxide and the channel is shown to improve the gate-lag ratio,[32] the improvement in the frequency characteristic does not seem satisfactory. For the schematic structure shown in Fig. 1, p-type spacers with different doping concentrations and thicknesses are designed to manifest the negative effect on the channel. Figure 3 shows the $I_{\rm ds}$ dependence on the parameters of the p-type spacer, and the thickness of 0 nm denotes a conventional MESFET. According to the charge neutrality condition in the p–n junction, we have

$$qN_{\rm A}x_{\rm p} = qN_{\rm D}x_{\rm n}, \quad (8)$$

where $N_{\rm A}$, $N_{\rm D}$ and $x_{\rm p}$, $x_{\rm n}$ are the doping concentrations and depletion thicknesses in the p-type and the n-type regions, respectively. When the doping concentration of the p-type spacer is two orders of magnitude lower than that of the n-type channel, the depletion in the p–n junction extends mainly to the p-type region, which has a negligible negative effect on the channel. With the increase of the doping concentration of the spacer, $I_{\rm ds}$ starts to decrease due to the fact that the depletion starts to extend to the

channel region. When the doping concentration of the spacer becomes comparable to that of the channel, I_{ds} decays, as shown obviously in Fig. 3. On the other hand, as the thickness of spacer increases, the area of the gate contact to the spacer layer expands. Thus, the reverse-bias across the p–n junction is enhanced and the depletion extends more widely, which accounts for the decrease in I_{ds}. In order to minimize negative effects, the thickness and the doping concentration of the p-type spacer are optimized to 75 nm and 5×10^{15} cm^{-3}, respectively. Further studies are based on these settings.

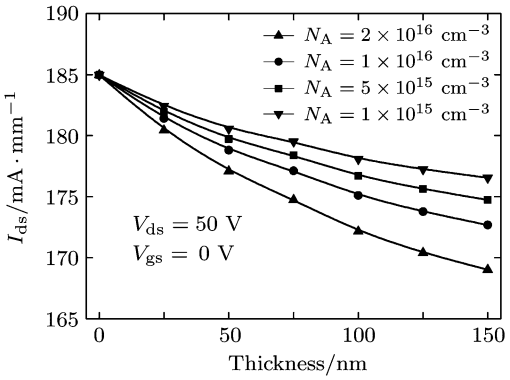


Fig. 3. Dependence of I_{ds} on the parameters of the p-spacer layer at $V_{gs} = 0$ V and $V_{ds} = 50$ V.

Figure 4 shows the transfer (I_{ds} versus V_{gs}) curves with different gate-buffer thicknesses. The thickness of 0 nm corresponds to a conventional MESFET. The pinch-off voltage V_p increases with the increase of the gate-buffer thickness t_{gb}. The distance between the gate electrode and the channel increases with the increase of t_{gb}, so only part of the original depletion exists in the channel in comparison with conventional MESFET. Even under very small V_{ds}, the effects on the V_p are still obvious. The differences in V_p indicate that the proposed structure offers a larger effective channel thickness, which can yield a larger I_{ds} under the same working conditions.

Figure 5 exhibits the typical output characteristics for the conventional and the proposed MESFETs. The V_{gs} of the conventional MESFET varies from 0 V to –8 V in steps of –2 V and from 0 V to –15 V in steps of –3 V for the proposed MESFET. The values of saturation drain current density I_{dsat} at $V_{gs} = 0$ V and $V_{ds} = 40$ V are about 325 mA/mm for the proposed MESFET and around 182 mA/mm for the conventional MESFET. The results support the analysis that the gate-buffer shares in part of the depletion and the effective channel thickness is increased. Owing to the reduction in channel resistance, there is a 79% improvement in I_{dsat}.

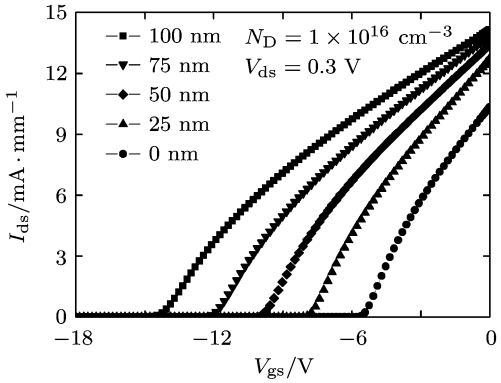


Fig. 4. Transfer curves under $V_{ds} = 0.3$ V.

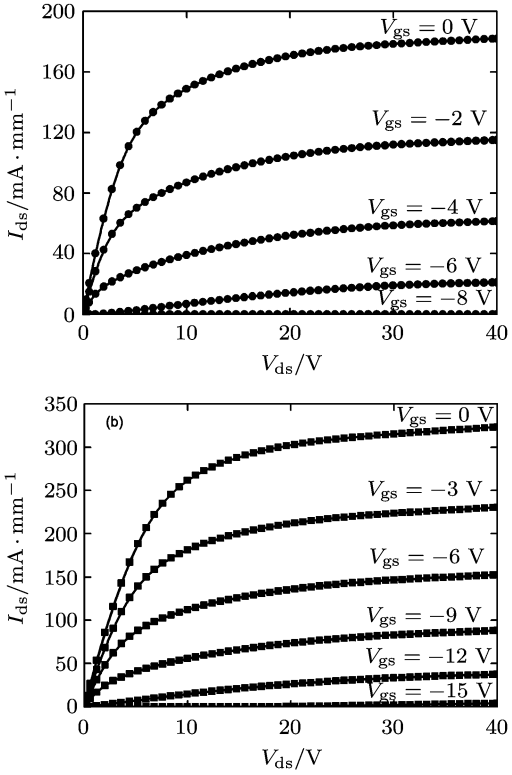


Fig. 5. *I–V* characteristics under different gate voltages for (a) conventional MESFET and (b) proposed MESFET.

To figure out the enhancement due to the improved structure, the values of addition defined as the ratio of $(I_{dsp} - I_{dsc})/I_{ds}$ are discussed with different gate-buffer structures as shown in Fig. 6, where I_{dsp} is I_{ds} of the proposed structure, and I_{dsc} is I_{ds} of the conventional structure. The operation condition is set to be $V_{ds} = 50$ V to drive the device into a deep saturation region. There is a linear relationship between the I_{ds} addition and the thickness (doping) of the gate-buffer. The addition can reach as high as 190% when the thickness and the doping concentration are chosen as 150 nm and 2×10^{17} cm^{-3}, respectively.

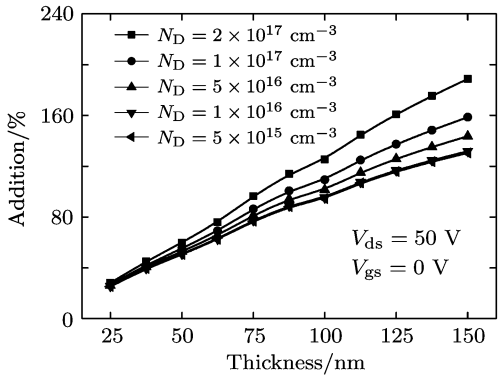


Fig. 6. Relationships between I_{ds} addition and the parameters of gate-buffer layer.

For power MESFETs, reliability is another requirement for device operation. The maximum output power density P_{max} is given by[33]

$$P_{max} = \frac{I_{dsat}\,(V_b - V_{knee})}{8}, \tag{9}$$

where V_b is the breakdown voltage and V_{knee} is the knee voltage of the saturation region. P_{max} is determined by both I_{dsat} and V_b. Figure 7 shows the breakdown characteristics. As can be seen, the p-type spacer incorporated with the gate-buffer raises the V_b of the device. However, with the increase of t_{gb}, the effect on V_b becomes lower. When t_{gb} exceeds 75 nm or the doping concentration exceeds 1×10^{16} cm^{-3} at t_{gb} = 75 nm, V_b starts to decrease. This is mainly due to the limit relationship between the state-on resistance R_{on} and V_b for semiconductor doped with a certain type of impurity, expressed as[34]

$$R_{on} = \frac{4V_b^2}{\mu\varepsilon_s E_{cr}^3}, \tag{10}$$

where μ, ε_s and E_{cr} are the mobility, the dielectric constant and the critical field of the material, respectively. According to Eq. (9), the calculated P_{max} of the proposed and the conventional MESFETs are about 6.1 W/mm and 3.41 W/mm, respectively.

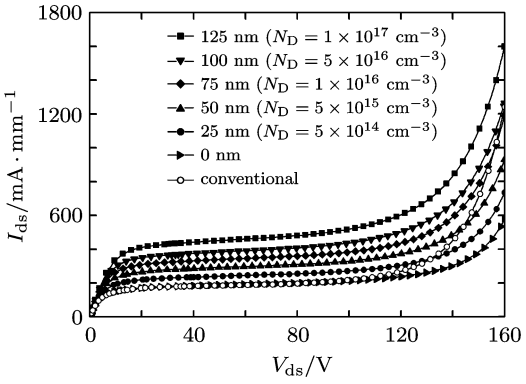


Fig. 7. Breakdown characteristics of MESFETs.

For microwave application, AC characterstics are essential for MESFETs. Figure 8 shows the AC equivalent circuit for MESFETs, which is actually a two-port network. The gate-capacitance C_g equals the sum of the gate–source capacitance C_{gs} and the gate–drain capacitance C_{gd}.

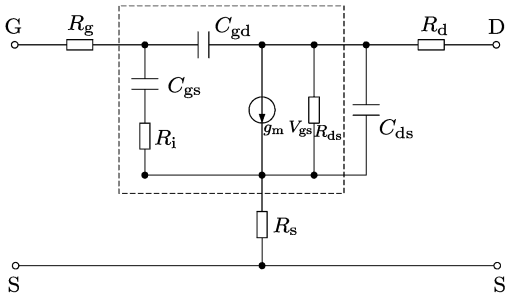


Fig. 8. AC equivalent circuit for MESFET.

The simulated AC characteristics at V_{ds} = 50 V and V_{gs} = −5 V are presented in Fig. 9 in the case of different t_{gb} values and doping concentrations. Results are obtained at a frequency of 3 GHz (in S-band) and a thickness of 0 nm that corresponds to a conventional MESFET. Transconductance g_m reveals the control ability of the gate. As shown in Fig. 9(a), with the increase of t_{gb}, the g_m curves increase to the maxima because the effective channel thickness is increased. When t_{gb} reaches a certain value (within a range of from 75 nm to 100 nm), g_m starts to decrease. This is due to the fact that when t_{gb} exceeds a certain value, the gate-depletion exists mainly in the gate-buffer layer and there is very little depletion existing in the channel. Depletion left in the channel is not able to entirely respond to the variation of the gate bias, especially at high frequencies. Therefore, the control ability of the gate is weakened. The drain conductance g_d in the saturation region is determined mainly by the effective channel length L_{ech}; for short channel MESFETs, L_{ech} increases as the gate depletion is decreased.[35] Therefore, the g_d of the proposed MESFET is larger than that of the conventional MESFET. For a given L_g, C_g (which equals the sum of C_{gs} and C_{gd}) is reversely proportional to the depletion thickness. Since the doping concentration of the gate-buffer is lower than that of the channel, depletion existing in the gate-buffer is larger than that in the channel under the same gate bias. For the proposed MESFET, the total depletion under the gate equals the sum of these two parts. Therefore, the thickness of the depletion under the gate in the proposed MESFET is larger than that in the conventional MESFET, leading to a reduction in C_g. Figures 9(b) and 9(c) show the variation tendencies of g_d and C_g, respectively.

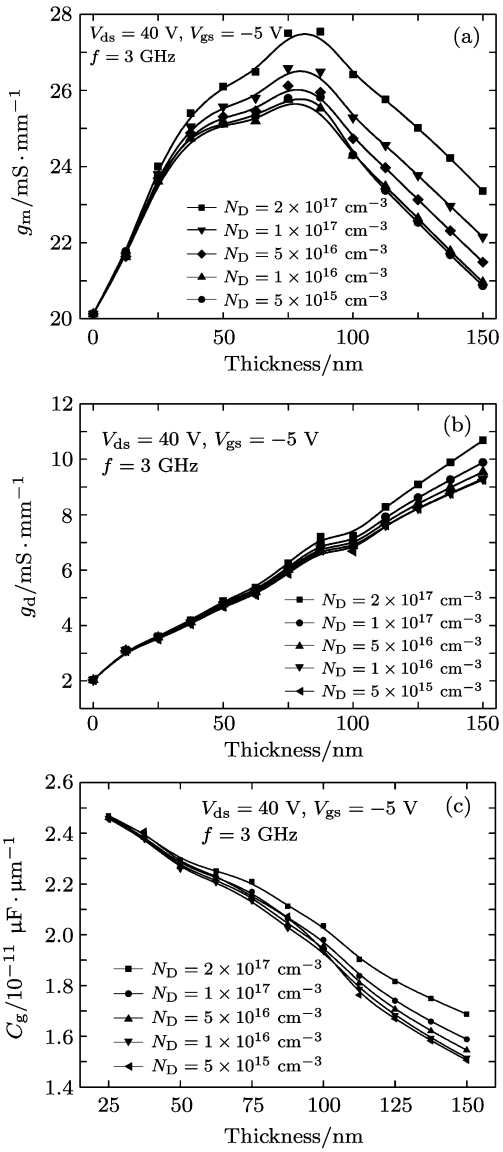


Fig. 9. Simulated AC characteristics of SiC MESFETs for (a) g_m, (b) g_d, and (c) C_g.

The cut-off frequency f_t and the maximum oscillation frequency f_{max} in the AC model for the MESFET obey the following two expressions:[36]

$$f_t = \frac{g_m}{2\pi (C_{gs} + C_{gd})}, \tag{11}$$

$$f_{max} = \frac{f_t}{2\sqrt{r_1 + f_t \tau_3}}, \tag{12}$$

where

$$r_1 = \frac{R_g + R_i + R_s}{R_{ds}}, \tag{13}$$

$$\tau_3 = 2\pi R_g C_{gd}, \tag{14}$$

with R_g being the gate resistance, R_i and R_{ds} the input and the output resistances under the gate, respectively, R_s the source resistance, and C_{gs} and C_{gd} the gate–source and the gate–drain capacitances, respectively. It can be calculated that f_t and f_{max} of the proposed MESFET are 15.1 and 75 GHz, while those of the conventional MESFET are 19.1 and 96 GHz, respectively. There is a 27% improvement in f_t and a 28% in f_{max}, respectively. Figure 10 illustrates the dependences of f_t and f_{max} on the parameters of the gate-buffer. In spite of the negative effect on V_b, the maximum values of f_t and f_{max} can be obtained to be 22.3 and 111 GHz when the thickness of the gate-buffer is chosen to be 150 nm.

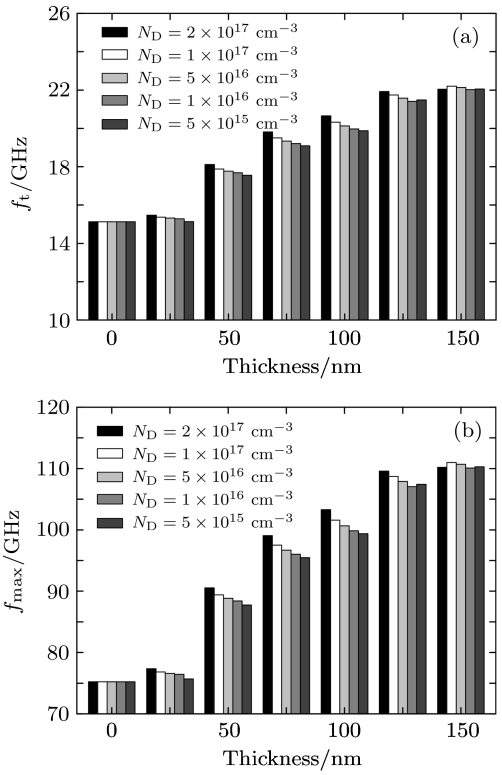


Fig. 10. Characteristics of variations for (a) f_t and (b) f_{max}.

4. Conclusion

An improved structure including a gate-buffer layer combined with a p-type spacer for a SiC MESFET is proposed. Through comparison with a conventional MESFET, it is revealed that the proposed structure provides a solution to the constraint condition between I_{ds} and V_b. Moreover, DC and AC characteristics are improved simultaneously. In addition, the characteristic dependence on the structural parameters is studied and the results show that the whole performance of the device is enhanced when the gate-buffer and the p-type spacer have the same thickness of 75 nm but different doping concentrations of 1×10^{16} cm^{-3} and 5×10^{15} cm^{-3}, respectively.

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