New 4H silicon carbide metal semiconductor field-effect transistor with a buffer layer between the gate and the channel layer*

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A new 4H silicon carbide metal semiconductor field-effect transistor (4H-SiC MESFET) structure with a buffer layer between the gate and the channel layer is proposed in this paper for high power microwave applications. The physics-based analytical models for calculating the performance of the proposed device are obtained by solving one- and two-dimensional Poisson's equations. In the models, we take into account not only two regions under the gate but also a third high field region between the gate and the drain which is usually omitted. The direct-current and the alternating-current performances for the proposed 4H-SiC MESFET with a buffer layer of 0.2 μm are calculated. The calculated results are in good agreement with the experimental data. The current is larger than that of the conventional structure. The cutoff frequency ($f_{\rm T}$) and the maximum oscillation frequency ($f_{\rm max}$) are 20.4 GHz and 101.6 GHz, respectively, which are higher than 7.8 GHz and 45.3 GHz of the conventional structure. Therefore, the proposed 4H-SiC MESFET structure has better power and microwave performances than the conventional structure.

Keywords: 4H silicon carbide, metal semiconductor field-effect transistor, Poisson's equation

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1. Introduction

Silicon carbide metal semiconductor field-effect transistors (SiC MESFETs) are well suited for high-power radio frequency (RF) applications, especially in extremely challenging environments, owing to their superior material properties.[1] With the recent progress in SiC epitaxial material and the device process, excellent power and RF performances of SiC MESFETs have been reported.[2−9] Although the SiC MESFET has a higher RF power density than that based on Si and GaAs, it is still worth investigating potential ways to improve it to better meet the increasing demand for high power microwave applications.

To achieve higher power microwave performances, a large product of the channel doping and the thickness ($N \times a$) and a minimum size of the gate length ($L_{\rm g}$) are required. However, a high doping concentration will lower the breakdown voltage, and a thick channel layer and a small gate length will lead to a low ratio of gate length to channel thickness ($L_{\rm g}/a$), which will degrade the performance of the devices and circuits.[10,11]

In view of these drawbacks, to improve the high power microwave performance, a new 4H-SiC MESFET structure is proposed in this paper for the first time, in which a lower doped gate-buffer layer is inserted between the gate and the channel layer with the channel doping, the thickness, and the gate length the same as those in the conventional structure. Due to the inserted lower doped gate-buffer layer, the proposed structure avoids the reduction of the breakdown voltage, which might occur while improving the device performance in the conventional structure. The analytical models of the current–voltage characteristics and the small-signal parameters for the proposed device are derived by solving one- and two-dimensional Poisson's equations. Using these analytical models, we calculate the direct-current (DC) and the alternating-current (AC) characteristics of the proposed 4H-SiC MESFET. The calculated currents are in excellent agreement with the experimental data. The results show that not only the channel currents but also the cutoff frequency and the maximum oscillation fre-

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quency are improved compared with those of the conventional structure though the channel doping. In addition, the thickness is not increased and the gate length is not reduced either.

2. Device structure and physical model

2.1. DC *I–V* characteristics model

For the SiC material, the dependence of electron mobility on the electric field can be described by the Caughey–Thomas model as[12]

$$\mu(E) = \mu_0 \Big/ \left[1 + \left(\frac{\mu_0 E}{\upsilon_{\rm s}}\right)^{\beta}\right]^{1/\beta}, \tag{1}$$

where μ is the low-field mobility, $\upsilon_{\rm s}$ is the saturation velocity, E is the electric field strength, and β is a curvature parameter of order 1 describing the saturation tendency. For the SiC material, the measured value of β is 1.2 in one experiment.[13] For simplicity, $\beta = 1$ is a reasonably good approximation.[14]

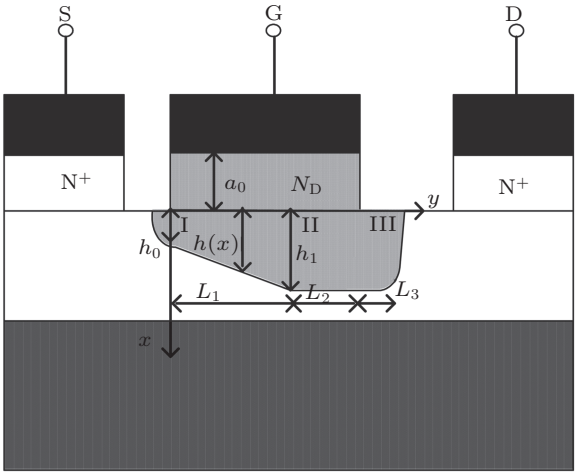


Fig. 1. Schematic diagram of the structure of the proposed SiC MESFET in saturation mode.

Figure 1 is the schematic diagram of the structure of the proposed SiC MESFET structure in this paper. Compared with the conventional SiC MESFET, a low doped gate-buffer layer is inserted between the gate and the channel layer.

To describe the device operation, the channel current at any point in the channel can be expressed as

$$I_{\rm C} = qWn(x)\mu(E)E(x)[a - h(x)], \tag{2}$$

where q is the charge of an electron, W is the channel width, a is the epitaxial channel layer thickness, $E(x)$ is the field strength along the channel, $n(x)$ is the electron concentration, and x is the distance away from the source. For small drain biases, we assume that the gate bias is not large enough to pinch off the channel, and that the electron velocity in the channel does not reach its saturation value. Thus, $n(x)$ is simply the doping concentration $N_{\rm D}$ of the channel. The $h(x)$ is the depletion layer thickness under the gate and can be obtained by solving the one-dimensional Poisson's equation as

$$h(x) = a_0\left(1 - \frac{N_0}{N_{\rm D}} + \frac{V(x) + V_{\rm G} + V_{\rm bi}}{qN_{\rm D}/2\varepsilon \cdot a_0^2}\right)^{\frac{1}{2}} - a_0, \tag{3}$$

where N_0 is the uniformly doped concentration of the buffer layer between the gate and the channel, which is smaller than that of the channel; a_0 is the thickness of the gate buffer layer; ε is the dielectric constant; $V(x)$ is the potential difference between the source and the point x away from the source; $V_{\rm G}$ is the gate bias; and $V_{\rm bi}$ is the built-in voltage.

Under a low drain voltage, the electric field in the channel is less than the saturation field $E_{\rm s}$, and only region I exists with its length L. With the field-dependent mobility incorporated, by integrating over channel length L, the channel current is obtained as

$$I_{\rm C}(V_{\rm G}, V_{\rm D}) = I_{\rm P}\frac{[3(u_{\rm d}^2 - u_0^2) - 2(u_{\rm d}^3 - u_0^3)] - 3a_0/a \cdot [(u_{\rm d}^2 - u_0^2) - 2(u_{\rm d} - u_0)]}{1 + Z(u_{\rm d}^2 - u_0^2) + Z \cdot 2a_0/a \cdot (u_{\rm d} - u_0)}, \tag{4}$$

where u_0 ($u_{\rm d}$) is the depletion layer width h_0 ($h_{\rm d}$) at the source (drain) end of the channel normalized to the epilayer channel layer thickness a and is given by

$$u_0(V_{\rm G}) = \frac{h_0}{a} = \sqrt{\left(1 - \frac{N_0}{N_{\rm D}}\right)\frac{a_0^2}{a^2} + \frac{(V_{\rm G} + V_{\rm bi} + I_{\rm C}R_{\rm S})}{V_{\rm P}}} - \frac{a_0}{a}, \tag{5a}$$

$$u_{\rm d}(V_{\rm G}, V_{\rm D}) = \frac{h_{\rm d}}{a} = \sqrt{\left(1 - \frac{N_0}{N_{\rm D}}\right)\frac{a_0^2}{a^2} + \frac{(V_{\rm D} + V_{\rm G} + V_{\rm bi} - I_{\rm C}R_{\rm D})}{V_{\rm P}}} - \frac{a_0}{a}, \tag{5b}$$

where $V_{\rm D}$ is the drain bias; $R_{\rm S}$ ($R_{\rm D}$) is the epitaxial channel layer resistance between the gate and the source (drain); and $I_{\rm P}$, $V_{\rm P}$, Z are constants expressed by

$$I_{\rm P} = \frac{q^2 N_{\rm D}^2 a^3 \mu_0 W}{6\varepsilon L},$$
$$V_{\rm P} = \frac{qN_{\rm D}a^2}{2\varepsilon}, \quad Z = \frac{qN_{\rm D}a^2\mu_0}{2\varepsilon L \upsilon_{\rm s}}, \tag{6}$$

with L being the gate length.

With the drain bias increasing gradually, the depletion layer at the end of the gate near the drain extends toward the substrate, forcing the channel to shrink progressively. Meanwhile, the lateral electric field in the channel increases, and the electron velocity rises toward its saturation value. It is assumed in our analysis that the saturation in the electron velocity occurs before pinching off the channel by the gate depletion region, and that when the electron velocity approaches its saturation value, i.e. $\upsilon(L) = \gamma\upsilon_{\rm s}$, where γ is a velocity saturation factor that is close to unity, $u_{\rm d} = u_{\rm s}$ and the channel current reaches its saturation value. The reasons are as follows. When $\gamma = 1$ in our model, an infinite field strength in the channel appears at the drain according to Eq. (1). For γ less than but close to unity, e.g. 0.99,[15] we obtain a finite value for the saturation electric field strength $E_{\rm s}$.

At a high drain bias, the channel is in saturation mode and can be divided into three regions, as shown in Fig. 1. In region I, which is L_1 long and near the source under the gate, the electric field is low, and the electron velocity is less than the saturation velocity ($\upsilon_{\rm s}$). The saturation regions below the gate and between the gate and the drain are labeled as regions II and III, respectively.

In region I, according to the analysis in the linear mode, the current is expressed as

$$I_{\rm C}(V_{\rm G}, V_{\rm D}) = I_{\rm P}\frac{[3(u_1^2 - u_0^2) - 2(u_1^3 - u_0^3)] - 3a_0/a \cdot [(u_1^2 - u_0^2) - 2(u_1 - u_0)]}{1 + Z \cdot L/L_1 \cdot (u_1^2 - u_0^2) + Z \cdot L/L_1 \cdot 2a_0/a \cdot (u_1 - u_0)}, \tag{7}$$

where u_1 is the depletion layer thickness normalized to the epilayer channel layer thickness a at the point where the electron reaches saturation velocity. It is given by

$$u_1(V_{\rm G}, V_{\rm D}) = \frac{h_1}{a}$$
$$= \sqrt{\left(1 - \frac{N_0}{N_{\rm D}}\right)\frac{a_0^2}{a^2} + \frac{(V(L_1) + V_{\rm G} + V_{\rm bi})}{V_{\rm P}}} - \frac{a_0}{a}, \tag{8}$$

where h_1 is the depletion layer thickness at the point where the electron reaches the saturation velocity, $V(L_1)$ is the potential difference between the source and the point $x = L_1$, and $\upsilon(L_1) = \gamma\upsilon_{\rm s}$. So the saturation channel current is expressed as

$$I_{\rm csat} = qN_{\rm D}Wa\gamma\upsilon_{\rm s}(1 - u_1). \tag{9}$$

The L_1 can be derived from Eqs. (7) and (9) as

$$L_1 = LZ\left[\frac{(u_1^2 - u_0^2) - \frac{2}{3}(u_1^3 - u_0^3)}{\gamma(1 - u_1)} - (u_1^2 - u_0^2)\right] - LZ \cdot \frac{a_0}{\gamma a}\left\{\frac{(u_1^2 - u_0^2) + 2[(\gamma - 1) - \gamma u_1](u_1 - u_0)}{1 - u_1}\right\}. \tag{10}$$

From Eqs. (9) and (10), for given u_1 or L_1, the saturation current in the channel can be obtained. Thus, other equations involving u_1 or L_1 are required, which can be two-dimensional Poisson's equations.

The two-dimensional Poisson's equations in the depletion layer are

$$\frac{\partial^2\Psi_1(x,y)}{\partial x^2} + \frac{\partial^2\Psi_1(x,y)}{\partial y^2} = -\frac{qN_0}{\varepsilon} \quad \text{for} \quad -a_0 < y < 0, \tag{11a}$$

$$\frac{\partial^2\Psi_2(x,y)}{\partial x^2} + \frac{\partial^2\Psi_2(x,y)}{\partial y^2} = -\frac{qN_{\rm D}}{\varepsilon} \quad \text{for} \quad 0 < y < a. \tag{11b}$$

The potential drop across regions II and III is obtained as

$$V(L + L_3) - V(L_1) = \left[\frac{2(au_1 + a_0)}{\pi} + \frac{L_3}{3}\right]E_{\rm s} \times \sinh\left(\frac{\pi L_2}{2(au_1 + a_0)}\right)\exp\left(\frac{-\pi L_3}{2(au_1 + a_0)}\right) + \frac{E_{\rm s}L_3}{3}\left[2\exp\left(\frac{\pi L_2}{2(au_1 + a_0)}\right) + 1\right]. \tag{12}$$

The equation involving L_3 is

$$\begin{aligned} & L_3^2\left\{\frac{qN_{\rm D}au_1}{\varepsilon}-E_{\rm s}\exp\left(\frac{\pi L_2}{2(au_1+a_0)}\right)\right. \\ & +\frac{E_{\rm s}}{\eta}\sinh\left(\frac{\pi L_2}{2(au_1+a_0)}\right) \\ & \left.\times\left[1+\tan\left(\frac{\pi a_0}{2(au_1+a_0)}\right)\right]\right\} \\ = & (au_1)^2E_{\rm s}\left[\exp\left(\frac{\pi L_2}{2(au_1+a_0)}\right)-1\right. \\ & \left.-\sinh\left(\frac{\pi L_2}{2(au_1+a_0)}\right)\exp\left(\frac{-\pi L_3}{2(au_1+a_0)}\right)\right], \quad (13) \end{aligned}$$

where

$$\begin{aligned} \eta = & \tan\left(\frac{\pi a_0}{2(au_1+a_0)}\right)\cos\left(\frac{\pi au_1}{2(au_1+a_0)}\right) \\ & +\sin\left(\frac{\pi au_1}{2(au_1+a_0)}\right), \\ V(L+L_3) = & V_{\rm D}-I_{\rm C}R_{\rm D}. \end{aligned}$$

From Eqs. (9), (10), (12), and (13), the saturation current in the channel is obtained.

With consideration of the resistance $R_{\rm b}$ of the buffer layer between the channel and the substrate, the drain current is expressed as

$$I_{\rm D}=I_{\rm C}+V_{\rm D}/R_{\rm b}. \quad (14)$$

From the analysis above, for a given SiC MESFET, of which the structural parameters (L, W, a, a_0, $N_{\rm D}$, N_0) are explicit, and a given bias ($V_{\rm D}$, $V_{\rm G}$), the drain current can be obtained.

2.2. AC model for small-signal parameters

For the SiC MESFET, its high frequency application is also of interest to researchers. To evaluate the high frequency performance conveniently, it is important to describe the small-signal parameters analytically.

From Eq. (4) the device drain conductance for the linear region can be derived as

$$g_{\rm dl}=\frac{3I_{\rm P}(u_{\rm d}+a_0/a)}{m_{\rm d}V_{\rm P}}\frac{\left[(1-u_{\rm d})-Z(u_{\rm d}-a_0/a)(u_{\rm d}^2-u_0^2)+2/3\cdot Z(u_{\rm d}^3-u_0^3)-2Z\cdot a_0/a\cdot u_{\rm d}\cdot(u_{\rm d}-u_0)\right]}{\left[1+Z(u_{\rm d}^2-u_0^2)+2Z\cdot a_0/a\cdot(u_{\rm d}-u_0)\right]^2}, \quad (15)$$

where

$$m_{\rm d}=u_{\rm d}+a_0/a.$$

Similarly, the transconductance for the linear region is

$$\begin{aligned} g_{\rm ml} = & \frac{3I_{\rm P}(u_{\rm d}+a_0/a)}{m_{\rm d}V_{\rm P}}\frac{\left[(1-u_{\rm d})-Z(u_{\rm d}-a_0/a)(u_{\rm d}^2-u_0^2)+2/3\cdot Z(u_{\rm d}^3-u_0^3)-2Z\cdot a_0/a\cdot u_{\rm d}\cdot(u_{\rm d}-u_0)\right]}{\left[1+Z(u_{\rm d}^2-u_0^2)+2Z\cdot a_0/a\cdot(u_{\rm d}-u_0)\right]^2} \\ & -\frac{3I_{\rm P}(u_0+a_0/a)}{m_0V_{\rm P}}\frac{\left[(1-u_0)-Z(u_0-a_0/a)(u_{\rm d}^2-u_0^2)+2/3\cdot Z(u_{\rm d}^3-u_0^3)-2Z\cdot a_0/a\cdot u_0\cdot(u_{\rm d}-u_0)\right]}{\left[1+Z(u_{\rm d}^2-u_0^2)+2Z\cdot a_0/a\cdot(u_{\rm d}-u_0)\right]^2}, \quad (16) \end{aligned}$$

where

$$m_0=u_0+a_0/a.$$

Based on Eq. (9), the drain conductance for the saturation region is obtained as

$$g_{\rm ds}=-\frac{3\gamma I_{\rm P}}{2Zm_{L_1}V_{\rm P}}f, \quad (17)$$

where

$$\begin{aligned} f^{-1} = & 1+\frac{1}{2m_{L_1}V_{\rm P}}\left[\frac{2E_{\rm s}a}{\pi}\sinh\frac{\pi\,(L-L_1)}{2\,(au_1+a_0)}\right. \\ & \left.-\frac{E_{\rm s}a\,(L-L_1)}{(au_1+a_0)}\cosh\frac{\pi\,(L-L_1)}{2\,(au_1+a_0)}\right] \\ & -\frac{E_{\rm s}LZ}{2m_{L_1}V_{\rm P}}\cosh\frac{\pi\,(L-L_1)}{2\,(au_1+a_0)} \\ & \times\left\{\left[\frac{2u_1(1-\gamma)}{\gamma}+\frac{(u_1^2-u_0^2)-2/3(u_1^3-u_0^3)}{\gamma(1-u_1)^2}\right]\right. \\ & \left.-\frac{a_0}{\gamma a}\left[\frac{(u_1^2-u_0^2)-(u_1-u_0)}{(1-u_1)^2}-2(1-\gamma)\right]\right\}, \\ m_{L_1} = & u_1+a_0/a. \end{aligned}$$

The expression of the transconductance for the saturation region is

$$g_{\rm ms}=-\frac{3\gamma I_{\rm P}}{2Zm_{L_1}V_{\rm P}}\,(k+1)\,, \quad (18)$$

where

$$\begin{aligned} h = & -\frac{1}{2m_{L_1}V_{\rm P}}\left[\frac{2E_{\rm s}a}{\pi}\sinh\frac{\pi\,(L-L_1)}{2\,(au_1+a_0)}\right. \\ & \left.-\frac{E_{\rm s}a\,(L-L_1)}{(au_1+a_0)}\cosh\frac{\pi\,(L-L_1)}{2\,(au_1+a_0)}\right] \\ & +\frac{E_{\rm s}LZ}{2m_{L_1}V_{\rm P}}\cosh\frac{\pi\,(L-L_1)}{2\,(au_1+a_0)} \\ & \times\left\{\left[\frac{2u_1(1-\gamma)}{\lambda}+\frac{(u_1^2-u_0^2)-2/3(u_1^3-u_0^3)}{\gamma(1-u_1)^2}\right]\right. \end{aligned}$$

$$- \frac{a_0}{\gamma a}\left[\frac{(u_1^2-u_0^2)-(u_1-u_0)}{(1-u_1)^2} - 2(1-\gamma)\right]\Bigg\}$$
$$- \frac{u_0 E_s L Z}{m_0 V_P}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)} \times \left[\frac{1-u_0}{\gamma(1-u_1)} - 1\right]\left(1+\frac{a_0}{au_0}\right),$$
$$k = fh.$$

To find the gate–source capacitance, the quantity of the charge in the depletion layer under the gate is needed. It can be derived from the potential distribution in the depletion layer, which is obtained by solving the two-dimensional Poisson's equation. The expression of the gate–source capacitance is

$$C_{gs} = C_{gs1} + C_{gs2} + C_{gs3}, \tag{19}$$

where

$$C_{gs1} = \frac{4\varepsilon W L V_P I_P}{aID}\Bigg\{\frac{-g_m}{I_D}\Bigg[\left(1-\frac{a_0}{a}\right)(u_1^3-u_0^3) - \frac{3}{4}(u_1^4-u_0^4) + \frac{3a_0}{a}(u_1^2-u_0^2)\Bigg] + \frac{3u_1}{2m_{L_1}V_P}\left(u_1+\frac{a_0}{a}\right)\left(1-u_1-\frac{ZI_D}{3I_P}\right)(k+1) - \frac{3u_0}{2m_0 V_P}\left(u_0+\frac{a_0}{a}\right)\left(1-u_0-\frac{ZI_D}{3I_P}\right)\Bigg\},$$

$$C_{gs2} = \frac{2\varepsilon W L Z u_1}{a}\Bigg\{\frac{g}{2Zm_{L_1}u_1}(k+1) + \frac{u_0}{m_0}\left[\frac{u_1-u_0}{\gamma(1-u_1)} + \frac{1-\gamma}{\gamma}\right]\left(1+\frac{a_0}{au_0}\right)\Bigg\},$$

$$C_{gs3} = -\varepsilon E_s W a\Bigg(\frac{k+1}{2m_{L_1}V_P}\Bigg\{1-\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)} - \frac{\pi(1-u_1)}{2(au_1+a_0)}\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)} \times \left[\frac{a(L-L_1)}{au_1+a_0} - \frac{Lg-L+L_1}{u_1}\right]\Bigg\} + \frac{\pi u_0 L Z(1-u_1)}{2m_0 V_P(au_1+a_0)}\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)} \times \left(\frac{1-u_0}{\gamma(1-u_1)}-1\right)\left(1+\frac{a_0}{au_0}\right)\Bigg),$$

$$g = 1 - \frac{L_1}{L} - Zu_1\Bigg\{\left[\frac{2u_1(1-\gamma)}{\gamma} + \frac{(u_1^2-u_0^2)-2/3(u_1^3-u_0^3)}{\gamma(1-u_1)^2}\right] - \frac{a_0}{\gamma a}\left[\frac{(u_1^2-u_0^2)-(u_1-u_0)}{(1-u_1)^2} - 2(1-\gamma)\right]\Bigg\}.$$

The maximum oscillation frequency is calculated from the following formula:

$$f_{max} = \frac{f_T}{2\sqrt{g_d\cdot(R_c+R_S)}}, \tag{20}$$

where R_c is the channel resistance and is expressed as

$$R_c = \frac{V(L_1)}{I_D} + \frac{a(u_1-u_0)}{\varepsilon \upsilon_s W} + \frac{a+a_0}{\varepsilon\upsilon_s W} \times \ln\left(\frac{1-u_1}{1-u_0}\right) + \frac{L-L_1}{qN_D\mu_0 aW(1-u_1)}.$$

3. Results and discussion

In our proposed SiC MESFET structure, the gate length and the gate width are 0.7 μm and 332 μm, respectively. Meanwhile, the thickness and the doping concentration are 0.26 μm and 1.7×10^{17} cm^{-3} for the channel layer, and 0.2 μm and 1×10^{14} cm^{-3} for the gate-buffer layer between the gate and the channel, respectively.

Using our model, we calculate the I–V characteristics of the proposed 4H-SiC MESFET with a gate-buffer layer of 0.2 μm, as shown in Fig. 2. For the condition $a_0 = 0$ in our model, the current versus the drain voltage describing the properties of a similar conventional SiC MESFET can also be obtained. For comparison, corresponding experimental results for the conventional structure are also included.[16] It can be seen that the I–V characteristics calculated by using our model for the conventional structure are in accordance with the experimental results and our model is verified. Given a gate bias, the drain current achieved in our proposed device is larger than that in the conventional one. For instance, the maximum saturation drain current is 0.18 A, which is larger than 0.1 A in the conventional structure. Since the total depletion layer is composed of the completely depleted gate-buffer layer and the depletion layer in the channel layer, the part in the channel layer shrinks as compared with that in the conventional structure when there exists a gate-buffer layer, as shown in Fig. 1. As a result, the effective channel width is increased, and a larger current occurs in the proposed device than that in the conventional one.

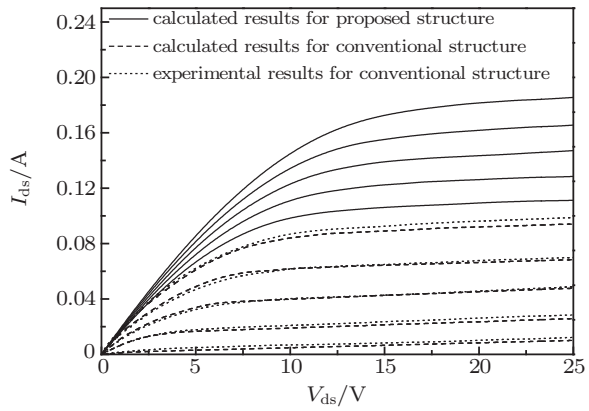


Fig. 2. Calculated and measured I–V characteristics for the proposed and the conventional structures at $V_{gs} = 0$ V, −2 V, −4 V, −6V, −8 V.

Figure 3 shows the drain currents versus the gate-buffer layer thickness under the gate. The thicker the gate-buffer layer, the larger the drain current, as demonstrated in the figure. A detailed investigation of the depletion layer under the gate shows that the increase of the drain current is due to the larger channel width, which is attributed to the decrease of the depletion layer thickness in the channel when the gate-buffer layer thickness is increased. In Fig. 3, a meaningful phenomenon appears, i.e., when the gate-buffer layer is increased sufficiently, the drain current approaches saturation. As a matter of fact, when the gate-buffer layer thickness is large enough, most of the depletion layer lies in the gate-buffer layer, and the remaining part in the channel layer is negligible in comparison with the channel layer thickness. When the gate-buffer layer thickness is further increased, the depletion layer completely lies in the gate-buffer layer, and the conduction channel thickness is as wide as 0.26 μm, which is invariable and leads to a constant current.

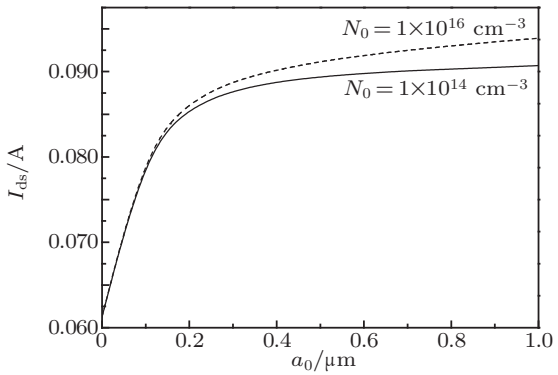


Fig. 3. Dependences of drain current on the buffer layer thickness at $V_{gs} = 0$ V and $V_{ds} = 5$ V.

Figures 4, 5, and 6 show the effects of the gate-buffer layer thickness on the small signal parameters. The transconductance, the gate–source capacitance, and the channel resistance are reduced while the drain conductance is increased with the increase of the inserted lower doped gate-buffer layer thickness (completely depleted), because the total depletion layer thickness under the gate is increased but the part in the channel is decreased, as depicted in Figs. 4 and 5. The cutoff frequency (f_T) increases slowly with the increases of the gate-buffer layer thickness, because the decrease of the transconductance is offset by the decrease of the gate–source capacitance. Since the decrease of the channel resistance with the increase of the gate buffer layer thickness is dominant compared with the increase of the drain conductance, the maximum oscillation frequency (f_{max}) increases more rapidly than the cutoff frequency. The results show that f_T and f_{max} at $V_{gs} = 0$ V and $V_{ds} = 30$ V are 20.4 GHz and 101.6 GHz, respectively. For the conventional structure, f_T and f_{max} are 7.8 GHz and 45.3 GHz, respectively. Therefore, the proposed 4H-SiC MESFET structure has better frequency performance than a similar device based on the conventional structure.

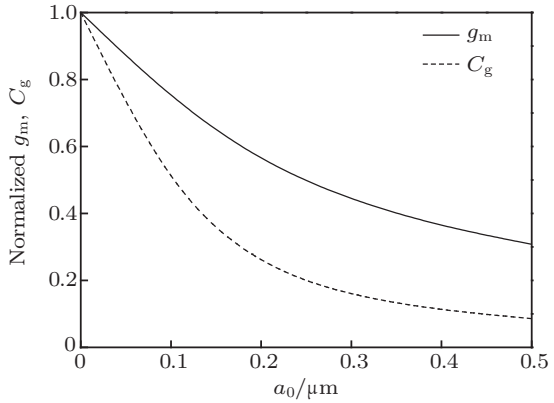


Fig. 4. Dependences of transconductance g_m and gate-source capacitance C_{gs} on gate buffer layer thickness at $V_{gs} = 0$ V and $V_{ds} = 30$ V.

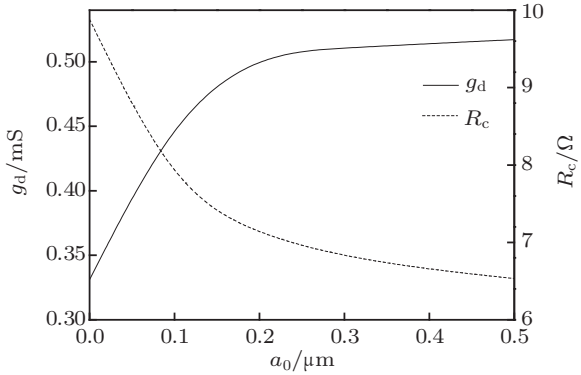


Fig. 5. Dependences of drain conductance g_d and channel resistance R_c on gate buffer layer thickness at $V_{gs} = 0$ V and $V_{ds} = 30$ V.

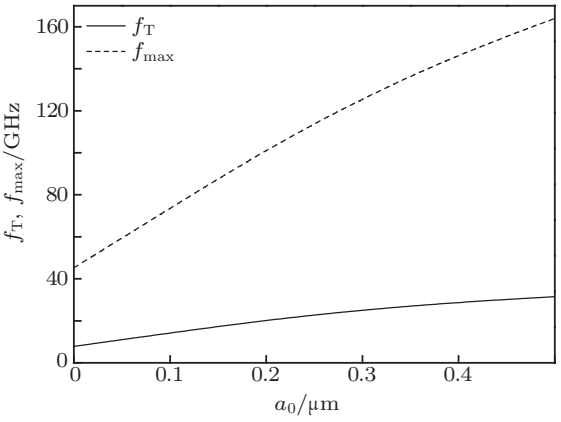


Fig. 6. Dependences of cutoff frequency f_T and maximum oscillation frequency f_{max} on gate buffer layer thickness at $V_{gs} = 0$ V and $V_{ds} = 30$ V.

4. Conclusion

A novel 4H-SiC MESFET structure with a buffer layer between the gate and the channel layer is proposed in this paper for high power microwave applications. Its physics-based analytical models for calculating the performance of the proposed 4H-SiC MESFETs are obtained for the first time by solving one- and two-dimensional Poisson's equations. The calculated results show good agreement with the experimental data. The maximum saturation drain current is about 0.18 A for the proposed 4H-SiC MESFETs, which is higher than 0.1 A for the conventional device. The cutoff frequency and the maximum oscillation frequency of the proposed SiC MESFET structure are 20.4 GHz and 101.6 GHz, respectively, which are inproved compared with 7.8 GHz and 45.3 GHz for the conventional one. Therefore, the proposed 4H-SiC MESFET has better power and microwave performances than a similar device based on the conventional structure. The proposed 4H-SiC MESFET structure and the achieved analytical models for the current–voltage characteristics and the small-signal parameters will provide valuable references to the research on the power microwave semiconductor devices.

References

[1] Zhang J, Zhang B and Li Z 2007 *Electron Lett.* **43** 692

[2] Sayed A and Boeck G 2005 *IEEE Trans. Microw. Theory* **53** 2441

[3] Deng X C, Feng Z, Zhang B, Li Z, Li L and Pan H S 2009 *Chin. Phys.* B **18** 3018

[4] Chen G, Qin Y F, Bai S, Wu P, Li Z Y, Chen Z and Han P 2010 *Solid-State Electron* **54** 353

[5] Zhang J P, Ye Y, Zhou C H, Luo X R, Zhang B and Li Z J 2008 *Microelectron Eng.* **85** 89

[6] Zhang J P, Luo X R, Li Z J and Zhang B 2007 *Microelectron Eng.* **84** 2888

[7] Sriram S, Hagleitner H, Namishia D, Alcorn T, Smith T and Pulz B 2009 *IEEE Trans. Electron Dev. Lett.* **30** 952

[8] Elahipanah H 2010 *Superlattices Microstruct.* **48** 529

[9] Chen G, Bai S, Li Z Y, Wu P, Chen Z and Han P 2009 *Chin. Phys.* B **18** 4474

[10] Zhu C L, Rusli, Tin C C, Zhang G H, Yoon S F and Ahn J 2006 *Microelectron Eng.* **83** 92

[11] Zhu C L, Rusli, Almira J, Tin C C, Yoon S F and Ahn J 2005 *Mater. Sci. Forum* **849** 483

[12] Caughey D M and Thomas R E 1967 *Proc. IEEE* **52** 2192

[13] Khan I A and Cooper J A Jr 2000 *IEEE Trans. Electron Dev.* **47** 269

[14] Murray S P and Roenker K P 2002 *Solid-State Electron* **46** 1495

[15] Chang C S and Fetterman H R 1997 *IEEE Trans. Electron Dev.* **34** 1456

[16] Huang M W, Goldsman N, Chang C H and Mayergoyz I 1998 *J. Appl. Phys.* **84** 2065