Temperature dependence of the P-hit single event transient pulse width in a three-transistor inverter chain*

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A comparison of the temperature dependence of the P-hit single event transient (SET) in a two-transistor (2T) inverter with that in a three-transistor (3T) inverter is carried out based on a three-dimensional numerical simulation. Due to the significantly distinct mechanisms of the single event change collection in the 2T and the 3T inverters, the temperature plays different roles in the SET production and propagation. The SET pulse will be significantly broadened in the 2T inverter chain while will be compressed in the 3T inverter chain as temperature increases. The investigation provides a new insight into the SET mitigation under the extreme environment, where both the high temperature and the single event effects should be considered. The 3T inverter layout structure (or similar layout structures) will be a better solution for spaceborne integrated circuit design for extreme environments.

Keywords: temperature dependence, single event transient, parasitic bipolar amplification effect, charge sharing collection

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1. Introduction

Spaceborne integrated circuits (ICs) are often required to work in extreme environments, where both extreme temperature and single event effects exist. Understanding the impact of the temperature on single event effects will be very important in guiding radiation hardened IC design. The single event transient (SET) is one the most important single event effects and has already become a concern of radiation effect researchers.[1−4] One of the major factors that determine the SET induced soft error is the SET pulse width ($W_{\rm SET}$). The $W_{\rm SET}$ is mainly determined by single event charge collection, which is controlled by the drift, the diffusion, and the parasitic bipolar amplification effect (bipolar effect). For the first time, our previous work showed that the P-hit $W_{\rm SET}$ will increase remarkably with increasing temperature in a two-transistor (2T) inverter in P substrate bulk CMOS technology, and the predominant mechanism causing the increase in $W_{\rm SET}$ is the enhancement of the bipolar effect with the increasing temperature.[5] This conclusion has been further confirmed experimentally by Gadlage *et al.*[6−8]

In the 2T inverter, the source of the PMOS strike is directly connected to the supply voltage ($V_{\rm dd}$), so a number of holes can be efficiently injected into the N well from $V_{\rm dd}$ when the source–channel–drain parasitic P^+–N–P^+ bipolar junction transistor turns on, leading to an increase in the charge collection. However, in the three-transistor (3T) inverter, two serial PMOSs exist in the layout, and the shallow trench isolation (STI) is used to isolate the two serial PMOSs. The holes may not be efficiently injected into the N well from $V_{\rm dd}$, and the drain may not efficiently collect the injected holes due to the conductive path being separated by the STI. So the bipolar effect may be not significant in the 3T inverter. The temperature dependence of P-hit $W_{\rm SET}$ may have significantly distinct characteristics compared with that in the 2T inverter. The investigation may provide a new insight into SET mitigation in extreme environments, where both high temperature and single event effects are present. The 3T inverter layout structure (or similar layout structures) may be a better solution in spaceborne IC design in this extreme environment.

2. Simulation details

Due to its good look-inside capability, three-dimensional mixed-mode technology computer aided

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design (TCAD) simulation has been proven to be a useful means of investigating the mechanism of single event charge collection.[4,6,9−13] In this paper, the SET production and propagation process is simulated in a 3T inverter chain (as shown in Fig. 1(a)). The two serial PMOSs in the second inverter are modeled as a three-dimensional device model (as shown in Fig. 1(b)), and the STI has been used to isolate the two serial PMOSs. The width of the STI is 140 nm to meet the minimum process design rules. The other transistors are modeled by using the Simulation Program with Integrated Circuit Emphasis (SPICE) model. The SET produced at node n2 will propagate through the chain, the SET appearing at node n6 will be recorded, and the pulse width will be calculated. The SET production process in the 2T inverter is also simulated for comparison. The only difference is that the two-PMOS device model is replaced by the one-PMOS device model (the upper PMOS in the two-PMOS device model is removed). The other circuit is not displaced (as shown in Figs. 1 and 2).

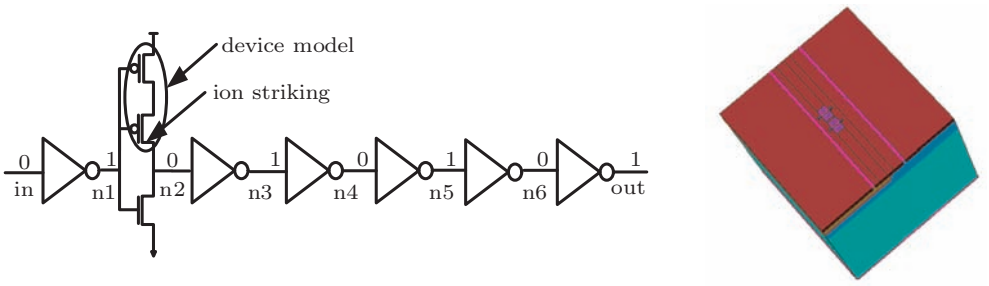


Fig. 1. (colour online) Circuit used for the simulations. (a) The circuit, (b) the two-serial-PMOS device model.

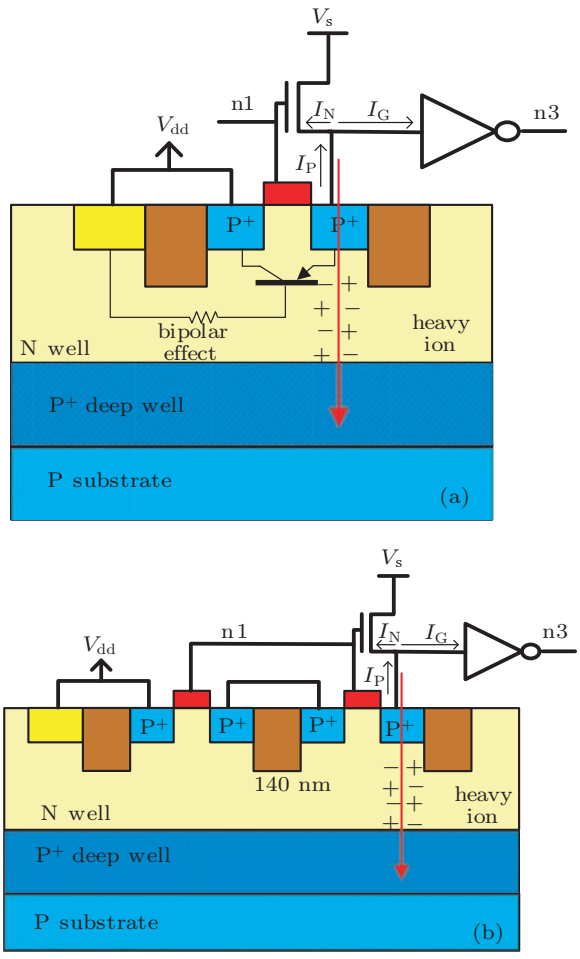


Fig. 2. (colour online) Sketch maps of the device models for (a) single PMOS and (b) double PMOSs.

The Sentaurus TCAD vE-2010.12 from Synopsys is adopted in our work to perform the structure construction and the device simulation. The P^+ deep well bulk CMOS technology is used in our simulations, as shown in Fig. 2. The doping profiles of the devices are calibrated to the 90 nm commercial process by using an inverse modeling approach. The P^+ deep well has a well depth of about 0.8 μm (from 0.80 μm to 1.60 μm). The two-serial-PMOS transistor size is $W_p : L_p = 600\ \text{nm} : 100\ \text{nm}$, the N-well contact distance from the PMOS is 380 nm. The NMOS transistor size is $W_n : L_n = 300\ \text{nm} : 100\ \text{nm}$. Same as that in Ref. [4], a backside substrate contact is used along the bottom surface of the substrate in series with a 1000 Ω resistor.

The heavy ion strike is simulated with an electron–hole pair column with the track as its axis. The ion used in the simulations has a linear energy transfer (LET) of 40 MeV·cm^2/mg. The LET value is kept constant along the heavy ion track. The length and the radius of the ion track are 10 μm and 0.1 μm, respectively. We assume that the ion strikes normally at the centre of the drain of the PMOS strike. The temperature rises from 200 K to 450 K.

The following physic mechanisms are considered: (i) the Fermi–Dirac statistics, (ii) the band-gap narrowing effect, (iii) the doping dependent Shockley–Read–Hall (SRH) recombination and the Auger recombination, and (iv) the temperature, doping, elec-

tric field, carrier–carrier scattering, and interface scattering impacts on the mobility. The hydrodynamic model is used for the carrier transport. Unless otherwise specified, default models and parameters provided by the Sentaurus TCAD vE-2010.12 are used.

3. Simulation results

The SET appearing at node n6 has been recorded, and the pulse width has been calculated. The $W_{\rm SET}$ shows distinct distributions for the 2T and the 3T inverters (as shown in Fig. 3). The $W_{\rm SET}$ increases with the increasing temperature for the 2T inverter. However, $W_{\rm SET}$ shows a parabolic shape with the increasing temperature for the 3T inverter. The pulse disappears at node n6 when the temperature is larger than 300 K, which indicates that the SET pulse attenuates in the propagation at high temperature.

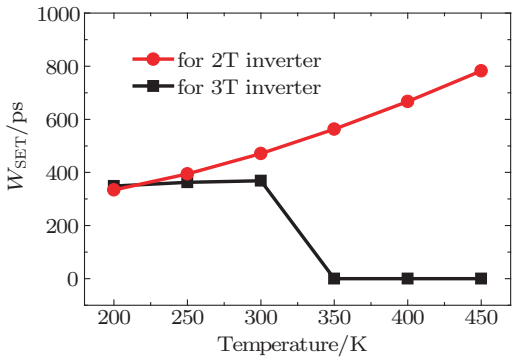


Fig. 3. The $W_{\rm SET}$ versus temperature for the 2T and the 3T inverters.

The SET pulse waveforms appearing at hitting node n2 and node n4 are shown in Figs. 4(a) and 4(b) for the 2T and the 3T inverters, respectively. Figure 4(a) shows that the original $W_{\rm SET}$ increases with the increasing temperature and the pulse amplitude is almost unchanged in the 2T inverter, so the SET can propagate through the inverter chain. However, as shown in Fig. 4(b), the original $W_{\rm SET}$ increases but the pulse amplitude decreases with the increasing temperature at hitting node n2 in the 3T inverter, so the SET pulse cannot propagate through the inverter chain (the pulse with amplitude smaller than $V_{\rm dd}/2$ will be filtered out and will not propagate through the inverter chain), and then the P-hit SET pulse will disappear in the 3T inverter chain at high temperature.

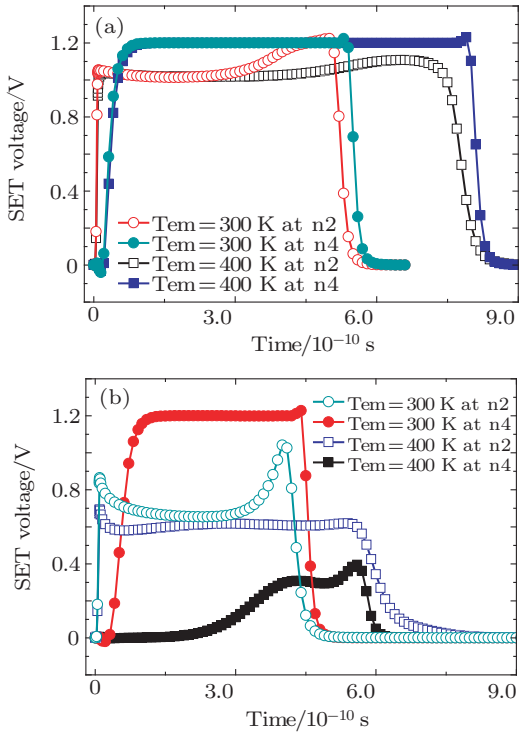


Fig. 4. (colour online) SET pulse waveforms at hitting node n2 and node n4 in (a) 2T and (b) 3T inverters.

4. Discussion

In the PMOS after the ion strike, the reverse-biased P–N junction between the P^+ drain and the N well will collapse, as shown in Fig. 5. The drain potential will collapse to the N well, and the N well potential will modulate the drain potential and further determine the SET pulse amplitude. In the substrate region, the P–N junction between the P^+ deep well and the N well is favourable for preventing the ionized electrons from overflowing out the N well, so a number of surplus ionized electrons are left behind in the N well, and the N well potential will fall.

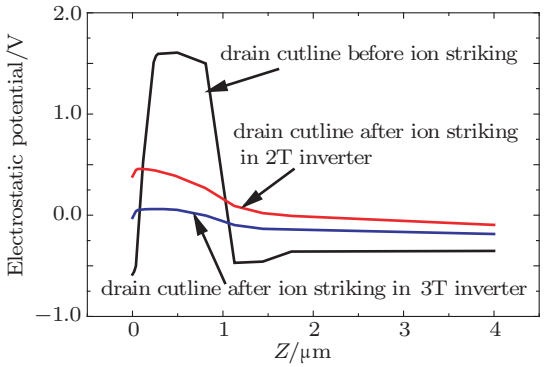


Fig. 5. (colour online) Distributions of the electrostatic potential along the drain cutline before and after 100 ps ion striking. The cutline is shown in Fig. 6. The distributions show that the N well potential falls after the ion strike, and it is smaller in the 3T inverter than that in the 2T inverter. The temperature considered is 300 K.

In the 2T inverter, the source of the PMOS strike is directly connected to V_{dd}, as shown in Fig. 6(a). When the N well potential falls, the P–N junction between the P^+ source and the N well is forward-biased, a large number of holes will be injected into the source, as shown in Figs. 6(a) and 7. The injected holes will lead to an increase in the charge collection and will be beneficial to modulating the N well potential. However, in the 3T inverter, two serial PMOSs exist in the layout, and shallow trench isolation (STI) has been used to isolate the two serial PMOSs, as shown in Fig. 6(b), then the holes cannot be efficiently injected into the N well after the N well potential falling (Figs. 6(b) and 7), and the drain cannot efficiently collect the injected holes due to the conductive path being separated by the STI, so the original W_{SET} is smaller in the 3T inverter than that in the 2T inverter. At the same time, the injected holes can modulate the N well potential, so the N well potential in the 2T inverter is also larger than that in the 3T inverter, as shown in Figs. 5 and 8. Correspondingly, the SET pulse amplitude in the 2T inverter is also larger than that in the 3T inverter at the same temperature.

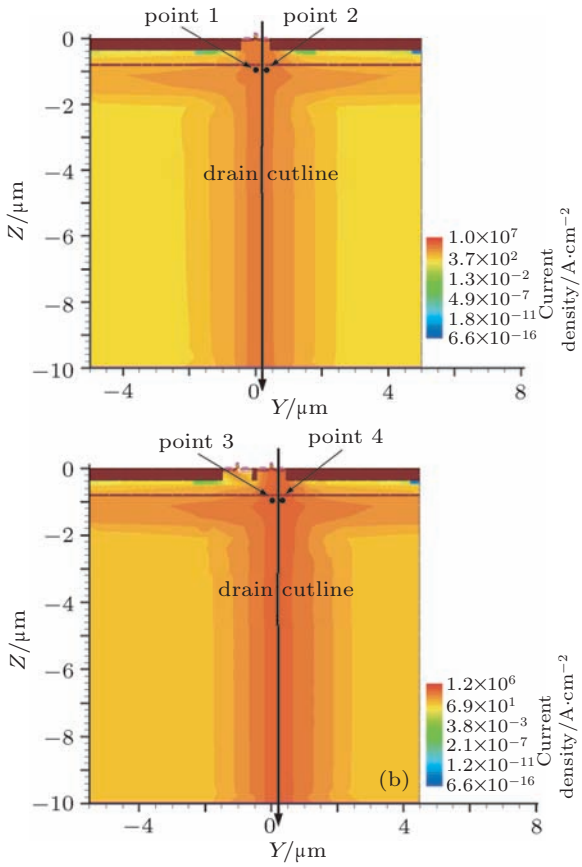


Fig. 6. (colour online) Distributions of hole current density in the PMOS after 100 ps ion striking in (a) 2T and (b) 3T inverters at 300 K.

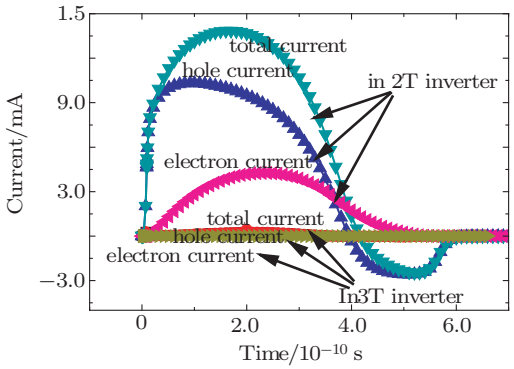


Fig. 7. (colour online) Current components of the electrodes connected to V_{dd} when the holes are injected in the 2T and the 3T inverters. In the 2T inverter, a number of holes are injected into the source of the PMOS strike. However, there is almost no hole injected into the source of the upper PMOS in the 3T inverter. The temperature considered is 300 K.

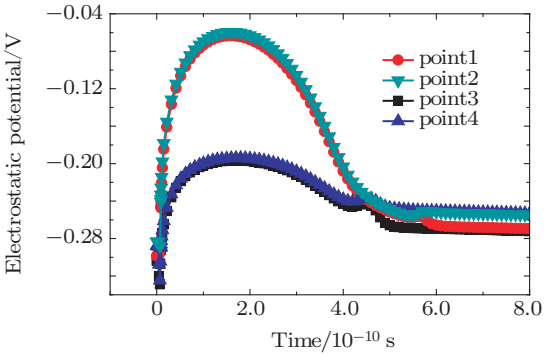


Fig. 8. (colour online) Electrostatic potential evolutions for the denoted points in the deep well layer for the PMOS in the 2T and the 3T inverters. The four points are shown in Fig. 6, points 1 and 3 have the same coordinates, points 2 and 4 also have the same coordinates. After ion striking, the potential in the 3T inverter is smaller than that in the 2T inverter during the charge collection. The temperature considered is 300 K.

Previous works have already shown that the bipolar effect can be significantly enhanced as the temperature increases in the 2T inverter,[5–8] so more holes will be injected into the source of the PMOS strike in the 2T inverter with the increasing temperature, as shown in Fig. 9. The injected holes can increase the charge collection at the drain and can keep the N well potential, so the initial W_{SET} will increase, and the pulse amplitude will be almost unchanged in the 2T inverter with the increasing temperature. However, in the 3T inverter, the injected holes do not significantly increase with the increasing temperature, as shown in Fig. 9, and the injected holes cannot be efficiently collected by the drain because of the conductive path being separated by the STI, as shown in Fig. 6(b), so the pulse amplitude will decrease with the increasing

temperature in the 3T inverter, as shown in Fig. 4(b). When the SET pulse amplitude is smaller than $V_{dd}/2$, the pulse will disappear during the propagation and cannot propagate through the circuit.

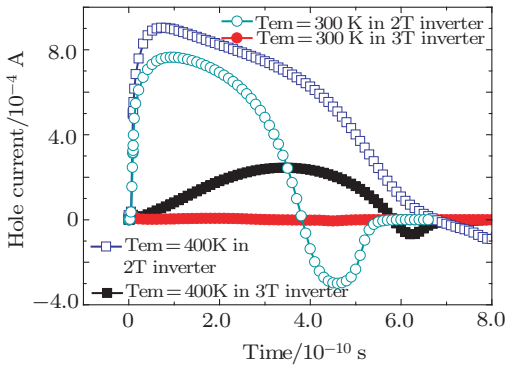


Fig. 9. (colour online) Injected hole currents versus temperature in 2T and 3T inverters.

5. Single event multiple transient in adjacent 3T inverters at high temperature

With the scaling down of technology , one ion strike can lead to multiple transients appearing in the adjacent devices in the combinational logic circuit due to the single event charge sharing collection.[13,14] It has already been shown that the bipolar effect is the main mechanism that induces the charge sharing collection between adjacent PMOSs in adjacent 2T inverters.[10,13,14] The charge sharing collection will increase significantly with the increasing temperature, and the enhancement of the bipolar effect has also been proven to be the predominant mechanism that causes the increase in the charge sharing collection.[13] As shown in Fig. 10, in the 2T inverter chains, two adjacent PMOSs belonging to two different inverter chains will synchronously collect the ion-induced holes after the ion striking (Fig. 11(a)), and two SETs may be produced and propagate through the two chains respectively. Similarly, in the 3T inverter chains, four adjacent PMOSs belonging to two different inverter chains will synchronously collect the ion-induced holes after the ion striking (Fig. 11(b)), and two SETs may be produced and propagate through the two chains.

The single event multiple transient (SEMT) production and propagation process is simulated at high temperature, the temperature is 400 K in all simulations, the LETs of 10 MeV·cm^2/mg, 20 MeV·cm^2/mg, 30 MeV·cm^2/mg, 40 MeV·cm^2/mg, 50 MeV·cm^2/mg, and 60 MeV·cm^2/mg are used, and the results are shown in Fig. 11. The SETs appearing at nodes n14 and n24 have been recorded, and the pulse widths have been calculated. As shown in Fig. 12, two SETs appear in the adjacent 2T inverter chain, and W_{SET} increases with the increasing LET. However, the pulses do not appear in nodes n14 and n24 in the adjacent 3T inverter chain.

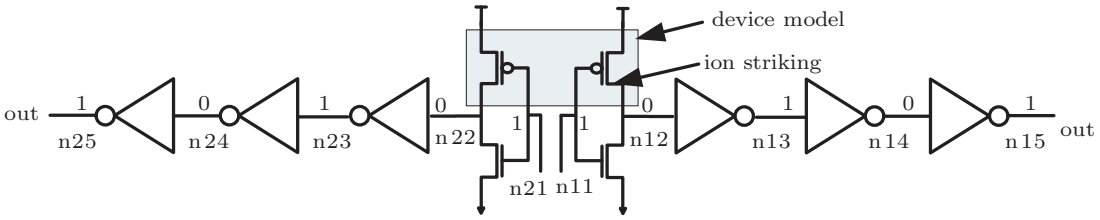


Fig. 10. Circuit used for the simulation. In the circuit, two adjacent PMOSs belonging to two different inverter chains will synchronously collect the ion-induced holes after the ion striking, and two SETs may be produced and propagate through the two chains separately.

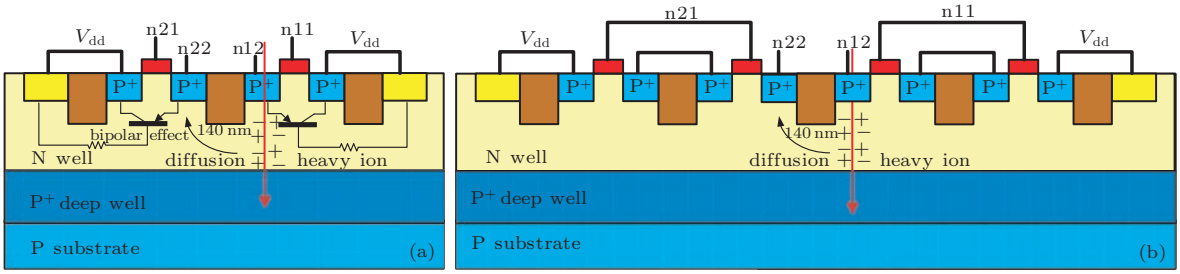


Fig. 11. (colour online) sketch maps of the device models for (a) two adjacent PMOSs in the 2T inverter chain and (b) four adjacent PMOSs in the 3T inverter chain.

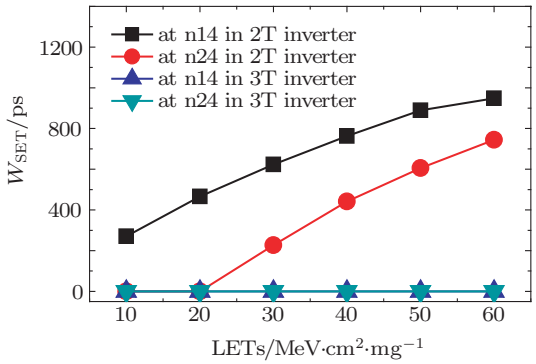


Fig. 12. (colour online) The W_{SET} versus temperature for adjacent 2T and 3T inverters. The temperature is 400 K.

Because the bipolar effect is not significant in the 3T inverter layout configuration, the single event charge sharing collection induced SEMTs can also be significantly mitigated. All of the investigations indicate that the 3T inverter layout configuration is the better solution for the radiation hardened ICs under the extreme environment, where both the high temperature and the single event effects should be considered.

6. Conclusion

In this paper, a comparison of the temperature dependence of a P-hit SET in the 2T inverter with that in a 3T inverter has been carried out based on three-dimensional numerical simulations. Due to the significantly distinct mechanisms of the single event change collection in the 2T and the 3T inverters, the temperature plays different roles in the SET production and propagation. The SET pulse will be significantly broadened in the 2T inverter chain while will be compressed in the 3T inverter chain with the increasing temperature. The P-hit multiple SETs in adjacent 3T inverter chains have also been studied at high temperature. The 3T inverter design can also efficiently mitigate the charge sharing collection induced SEMTs. The investigation provides a new insight into SET mitigation in extreme environments, where both the high temperature and the single event effect should be considered. The 3T inverter layout structure (or similar layout structures) will be a better solution for use in spaceborne integrated circuit design for the extreme environments.

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