New insight into the parasitic bipolar amplification effect in single event transient production*

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In this paper, a new method is proposed to study the mechanism of charge collection in single event transient (SET) production in 90 nm bulk complementary metal oxide semiconductor (CMOS) technology. We find that different from the case in the pMOSFET, the parasitic bipolar amplification effect (bipolar effect) in the balanced inverter does not exist in the nMOSFET after the ion striking. The influence of the substrate process on the bipolar effect is also studied in the pMOSFET. We find that the bipolar effect can be effectively mitigated by a buried deep P^+-well layer and can be removed by a buried SO_2 layer.

Keywords: parasitic bipolar amplification effect (bipolar effect), single event transient, substrate process

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1. Introduction

In recent years, the rapid development of space exploration has led to urgent requirements for radiation hardened integrated circuits (ICs). Single event effects, such as the single event upset (SEU) and the single event transient (SET), are important issues in determining the reliability of spaceborne ICs. As technology scales down, the SET has become the main concern of radiation effect researchers;[1−3] the reason being that IC soft errors will be dominated by the SET.[4,5] One of the major factors that determine the SET induced soft error is the SET pulse width ($W_{\rm SET}$). The $W_{\rm SET}$ is determined by the single event charge collection, which is controlled by the drift, the diffusion, and the parasitic bipolar amplification effect (bipolar effect). Previous investigations have already indicated that the bipolar effect in the balanced inverter is more significant in the pMOSFET than that in the nMOSFET in P substrate bulk CMOS technology.[6,7] However, whether the bipolar effect really exists in the nMOSFET still needs to be evidentially verified. At the same time, an in-depth study of the bipolar effect in the pMOSFET will be beneficial for proposing a suitable scheme for SET mitigation.

In the traditional method to distinguish the bipolar effect from other mechanisms (drift and diffusion), a diode obtained by removing the source and the gate from the original device is used. The diode can break the source-channel-drain parasitic bipolar junction transistor structure to further remove the bipolar effect, so comparing the charge collection of the diode with that of the original device can verify whether a parameter (such as temperature) just affects the bipolar effect.[8,9] However, the method removes the influence of the source on the charge collection, so the role of the source in the SET production cannot be explored clearly. New mechanisms of charge collection may be discovered by a new method, which may be beneficial to explaining why the maximal $W_{\rm SET}$ comes from the ion-struck pMOSFET but not the ion-struck nMOSFET in the balanced inverter.

2. Simulation details

Due to its good look-inside capability, three-dimensional mixed-mode technology computer aided design (TCAD) simulation has been proven to be a useful means for investigating the mechanism of single event charge collection.[6,7,10,11] In this paper, the SET production processes in a two-transistor (2T) in-

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verter and a three-transistor (3T) inverter are simulated. The struck pMOSFET or nMOSFET transistor is simulated as a three-dimensional (3D) numerical model, and the other transistors are simulated as corresponding circuit models. In the 3T inverter, an additional transistor in series is used for preventing the charge from being injected into or overflowing out of the source of the struck device (as shown in Fig. 1), so the charge cannot be injected into or overflow out of the emitter of the parasitic bipolar junction transistor after the ion strike. The role of the source in the SET production can be clearly discovered in the comparison.

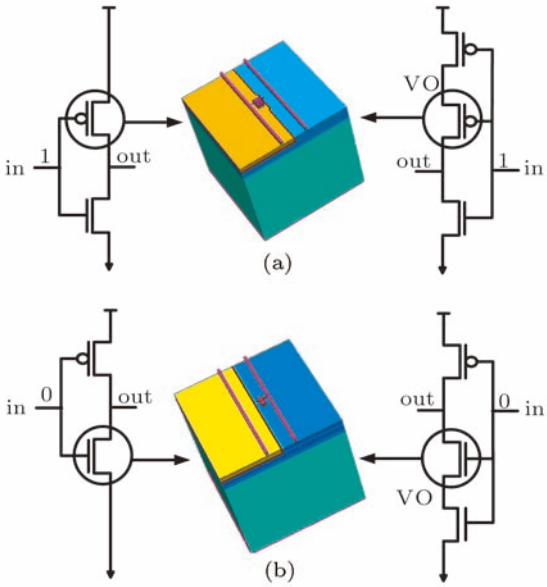


Fig. 1. (colour online) Circuits used for simulations of (a) two pMOSFETs and (b) two nMOSFETs.

Two different combinations are performed in our simulations for the pMOSFET and the nMOSFET, respectively. The off-state pMOSFET or nMOSFET is affected by the ion striking. The node VO in the 3T inverter is initialized to "1" and "0" to keep the same voltage condition as that of the 2T inverter, respectively (as shown in Fig. 1).

The Sentaurus TCAD vE-2010.12 from Synopsys is adopted in our work to perform the structural construction and the device simulation. Common P-substrate bulk CMOS technology is used in our simulations, as shown in Fig. 2. The doping profiles of the devices are calibrated to that of the 90 nm commercial process in China by using an inverse modeling approach. The transistor size is $W_{\rm n} : L_{\rm n} = 300\ {\rm nm} : 100\ {\rm nm}$ and $W_{\rm p} : L_{\rm p} = 600\ {\rm nm} : 100\ {\rm nm}$, and the geometric configuration refers to the layout of the standard cell provided by the foundry.

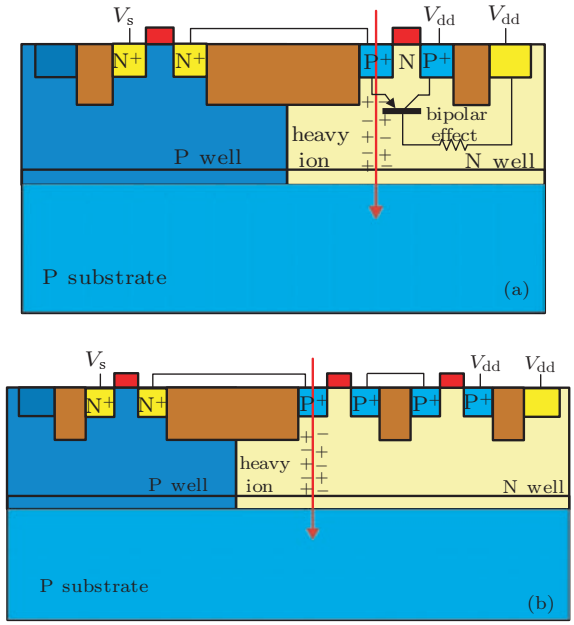


Fig. 2. (colour online) Device layouts of (a) 2T inverter and (b) 3T inverter (two pMOSFETs condition).

The heavy ion striking is simulated as an electron–hole pair column with the track as its axis. The ion used in the simulations has linear energy transfers (LETs) of 5 MeV·cm^2/mg, 10 MeV·cm^2/mg, 30 MeV·cm^2/mg, 50 MeV·cm^2/mg, and 70 MeV·cm^2/mg. The LET value is kept constant along the heavy ion track. The length and the radius of the ion track are 10 μm and 0.1 μm, respectively. We assume that the ions strike at the centre of the drain of the struck device and they strike the surface of the structure normally, the angular effects are not discussed in this paper.

The following aspects are considered: (i) the Fermi-Dirac statistics, (ii) the band-gap narrowing effect, (iii) the doping dependent Shockley–Read–Hall (SRH) recombination and the Auger recombination, (iv) the effects of doping, electric field, carrier-carrier scattering, and interface scattering on the mobility. The hydrodynamic model is used for the carrier transport. The default models and the parameters provided by the Sentaurus TCAD vE-2010.12 are used unless otherwise specified.

3. Simulation results

As shown in Fig. 3, the values of $W_{\rm SET}$ produced in the pMOSFET and the nMOSFET show different distributions in the 2T and the 3T inverters. Figure 3(a) shows that $W_{\rm SET}$ in the 3T inverter

is smaller than that in the 2T inverter in the pMOSFET. The W_{SET} difference between the 2T and the 3T inverters is also shown in Fig. 3(a). The difference is insignificant when the LET is 5 MeV·cm^2/mg. However, the difference becomes significant when the LET is 70 MeV·cm^2/mg (the difference in W_{SET} is 425.352 ps). The results indicate that for the 2T inverter, the source plays a harmful role in the SET production, and the charge is injected into the source of the struck pMOSFET, leading to an increase in W_{SET}.

Figure 3(b) shows that W_{SET} in the 3T inverter is larger than that in the 2T inverter in the nMOSFET. The W_{SET} difference between the 3T and the 2T inverters is also shown in Fig. 3(b), which is insignificant when the LET is 5 MeV·cm^2/mg and also becomes significant when the LET is 70 MeV·cm^2/mg (the difference in W_{SET} is 151.483 ps). The results indicate that for the 2T inverter, the source plays a beneficial role in the SET mitigation, and the charge is not injected into but overflows out of the source of the struck nMOSFET, leading to a decrease in W_{SET}.

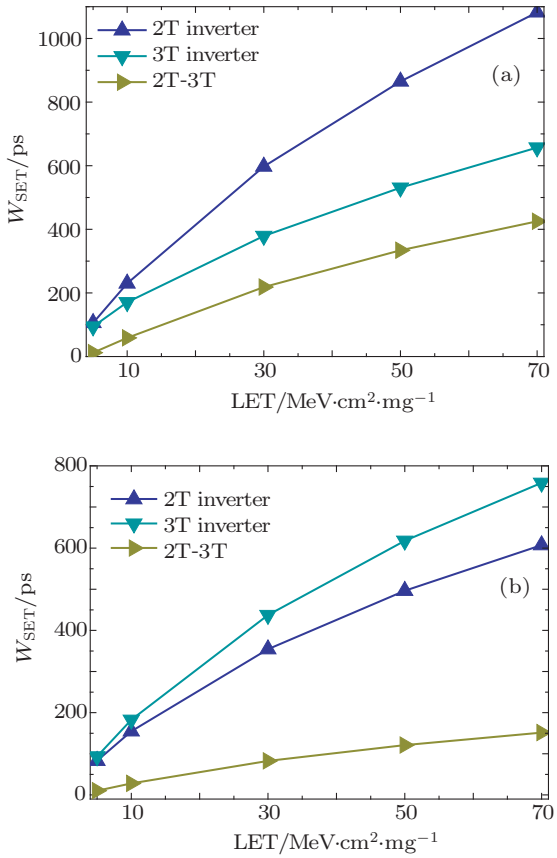


Fig. 3. (colour online) The W_{SET} in 2T and 3T inverters of (a) ion struck pMOSFET and (b) ion struck nMOSFET.

For the balanced 2T inverter, the maximal SET pulse is actually produced in the pMOSFET. The reason is that the bipolar effect exists in the pMOSFET but not in the nMOSFET, so the source plays a different role in the SET production. The source helps to broaden W_{SET} in the pMOSFET but reduces W_{SET} in the nMOSFET.

4. Discussion

The existence of the bipolar effect in the pMOSFET is determined by whether the surplus ionized electrons are left behind in the N well. The surplus ionized electrons can disturb the electric potential of the N well and make the P–N junction between the P^+ source and the N well forward-biased, then the source-channel-drain parasitic P^+NP^+ bipolar junction transistor will be turned on, the source will inject holes into the N well. These holes can pass through the channel and be collected at the drain, where they are added to the original ion-induced holes and can cause an increase in the charge collection, thereby broadening W_{SET}. This is the well-known parasitic bipolar amplification effect.

In the substrate region, like the P–N junction between the P^+ drain and the N well, the P substrate and the N well also form a reverse-biased P–N junction, as shown in Fig. 4(b). According to the electrostatic potential distribution, two reverse-biased P–N junctions exist along the drain cutline before the ion striking. After the ion striking, the two P–N junctions collapse (the two reverse-biased P–N junctions shown in Fig. 4(b) disappear after 100 ps ion striking) and can be regarded as a conductive path,[12] the ionized holes are collected by the drain and the substrate. Because the pull down nMOSFET resists the drain to collect the ionized holes, a large number of the ionized holes will be collected by the substrate. This leads to the surplus ionized electrons staying in the N well, and the P–N junction between the P^+ source and the N well will be forward-biased, so the bipolar effect exists in the pMOSFET and will be significantly affected by the substrate process.

In order to verify that the substrate process is the main factor determining the bipolar effect in the pMOSFETs, a buried deep P^+-well layer or a SO_2 layer has been intentionally added into the original numerical model to perform the simulations, as shown in Fig. 5. The deep P^+-well layer (the boron doping profile is 1×10^{18} cm^{-3}) and the SO_2 layer are directly located under the N well. The deep well has a well depth of about 0.8 μm (from 0.85 μm to 1.65 μm).

As shown in Fig. 5(a), the simulations can help to understand the bipolar effect characteristic of the pMOSFET in the deep P^+-well technology. Even though the device configuration in Fig. 5(b) does not really exist, the simulations can help to understand the bipolar effect characteristic of the pMOSFET in the silicon-on-insulator (SOI) technology, because the device configuration is similar to that in SOI technology.

The simulation results are shown in Fig. 6. Figure 6(a) shows that $W_{\rm SET}$ in the 3T inverter is still smaller than that in the 2T inverter in the deep P^+-well technology, which indicates that the bipolar effect still exists. The $W_{\rm SET}$ difference between the 2T and the 3T inverters is significantly reduced (the difference in $W_{\rm SET}$ is 172.725 ps when the LET is 70 MeV·cm^2/mg), which indicates that the bipolar effect has already been effectively mitigated by the buried deep P^+ well. However, different from the results shown in Figs. 3(a) and 6(a), the interesting results in Fig. 6(b) show that $W_{\rm SET}$ is larger in the 3T inverter than that in the 2T inverter in the second configuration shown in Fig. 5(b), the source plays a beneficial role in the SET mitigation, and the bipolar effect does not exist.

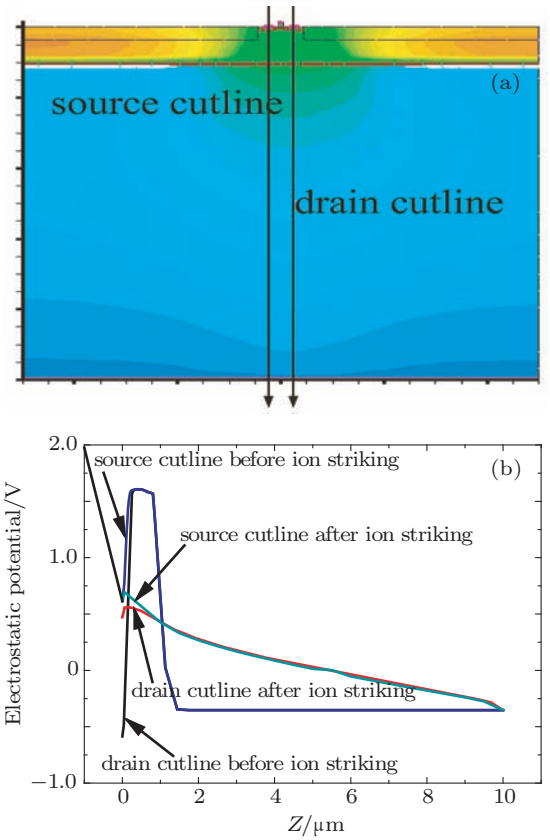


Fig. 4. (colour online) Electrostatic potentials along the source and the drain cutlines before and after 100 ps ion striking: (a) cross section of the pMOSFET after ion striking; (b) electrostatic potential.

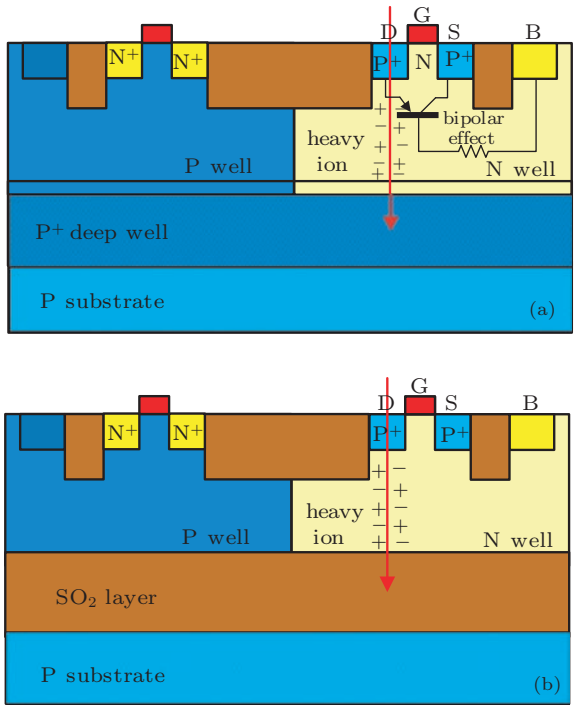


Fig. 5. (colour online) The buried deep P^+-well layer (a) and SO_2 layer (b) added into the original numerical model.

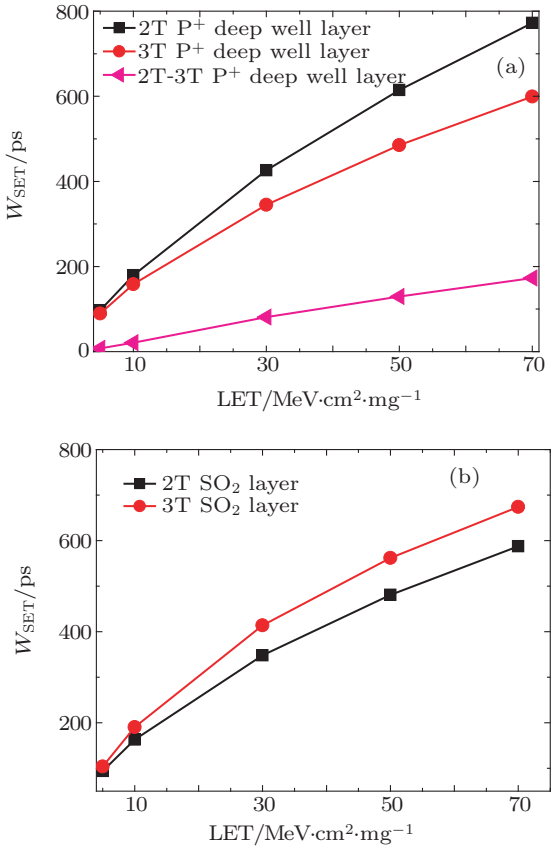


Fig. 6. (colour online) The $W_{\rm SET}$ produced in 2T and 3T inverters of pMOSFETs with (a) a deep P^+-well layer and (b) an SO_2 layer, respectively.

The additional deep P^+-well layer will help to form two P–N junctions (a P–N junction between the deep P^+ well and the N well and a P–N junction between the deep P^+ well and the P substrate, as shown in Fig. 7(a)). The two P–N junctions existing in the deep P^+-well technology restrict the electrostatic potential in the deep P^+-well layer (as shown in Fig. 7(a), the electrostatic potential from 0.85 μm to 1.65 μm is much smaller before the ion striking). After the ion striking, the P–N junctions also collapse, however the electrostatic potential is still smaller than that in the common bulk CMOS technology. Even the electric field is still favourable for collecting the holes, the holes drifting out of the N well decrease relatively. At the same time, the surplus electrons left in the N well also decrease. So the bipolar effect will be effectively mitigated by the deep P^+-well layer. Figure 7(b) also shows that the substrate collected holes are actually less in the deep P^+-well technology than that in the common technology. So the bipolar effect is effectively mitigated by the buried deep P^+ well.

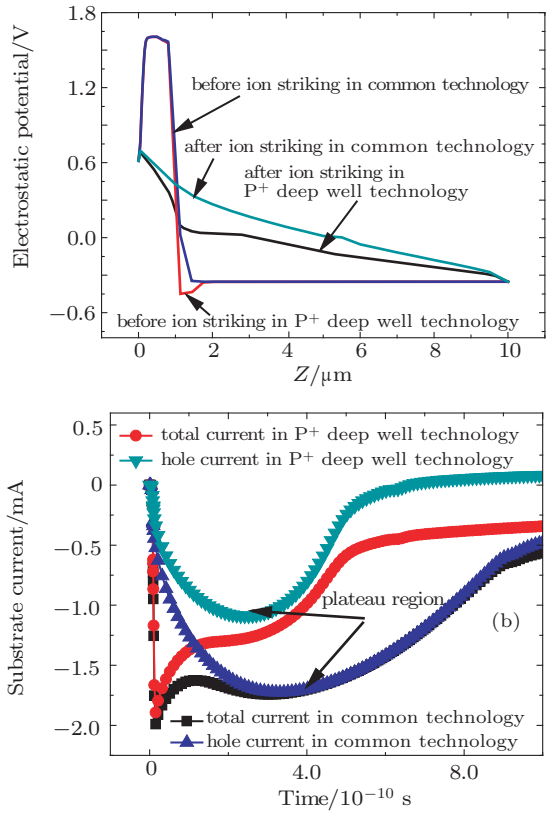


Fig. 7. (colour online) (a) Electrostatic potentials along the source cutline, and (b) substrate current components of pMOSFET in the common technology and the deep P^+-well technology. The LET is equal to 50 MeV·cm^2/mg.

In the second configuration, the buried SO_2 layer prevents the substrate from collecting the ionized holes. Even the ionized holes can also be collected by the drain, the pull-down nMOSFET restrains the holes from being largely collected. At the same time, the ionized electrons can be collected by the N-well contacts. Even the N-well potential falls slightly, the P–N junction between the P^+ source and the N well is still reverse-biased. In this condition, the source-channel-drain parasitic P^+NP^+ bipolar junction transistor is not turned on, and the source will help to collect the ionized holes to mitigate the SET pulse, and the bipolar effect does not exist. As shown in Fig. 8 (In the Sentaurus TCAD numerical simulations, the positive electron current indicates that the electrons overflow out of the electrode, and the positive hole current indicates that the holes are injected into the electrode), the source actually plays different roles in the SET production in these two different device configurations. In common technology, after the ion striking, the P–N junction between the P^+ source and the N well is forward-biased, and a large number of holes are injected into the source. When the buried SO_2 layer replaces the deep P^+-well layer, the P–N junction is still reverse-biased, but the holes overflow out of the source to help mitigate the SET. So the substrate process plays a key role in determining the existence of the bipolar effect.

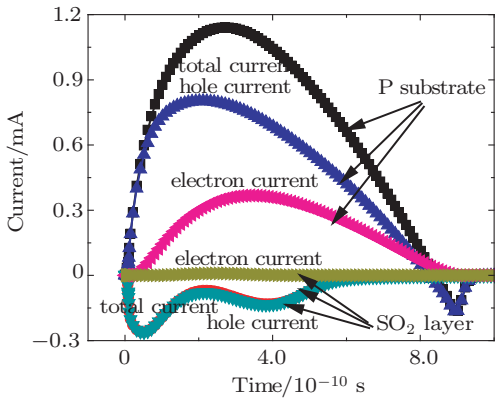


Fig. 8. (colour online) source current components of pMOSFETs in two different configurations. The LET is equal to 50 MeV·cm^2/mg.

Similarly, the existence of the bipolar effect in the nMOSFET is determined by whether the surplus ionized holes are left behind in the P well. Based on the above discussion, it is not surprising that in our simulations, W_{SET} in the 3T inverter is also larger than that in the 2T inverter for the nMOSFET. Different from that in the pMOSFET, only a weaker P–N junction between the P well and the P substrate exists in the substrate region in the nMOSFET. After the ion

striking, the ionized holes and electrons both are dispersed throughout the P substrate. Even the P-well potential rises up slightly, the P–N junction between the N^+ source and the P well is still reverse-biased (as shown in Fig. 9(a)), so the source will help to collect the ionized electrons to mitigate the SET, as shown in Fig. 9(b).

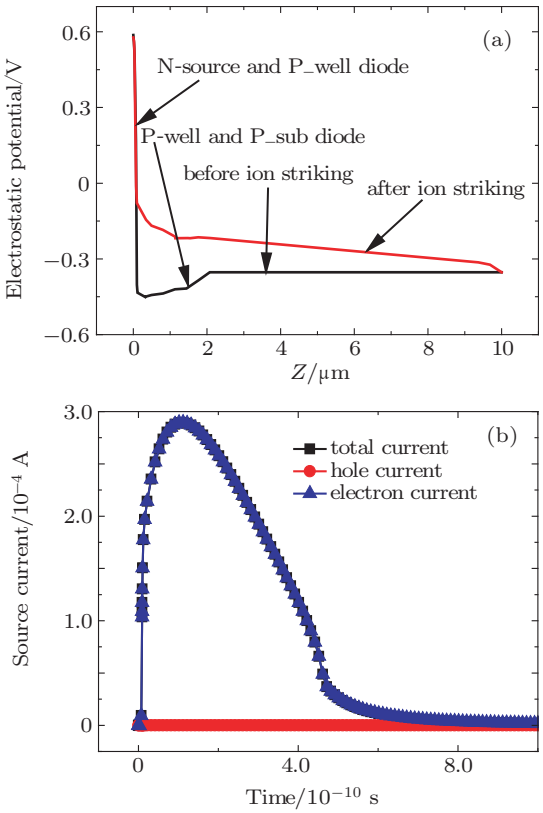


Fig. 9. (colour online) (a) Electrostatic potentials along the source cutline and (b) source current components of nMOSFET. The LET is equal to 50 MeV·cm^2/mg.

5. Conclusion

In this paper, a new analytical method is proposed to study the influence of the parasitic bipolar amplification effect on $W_{\rm SET}$. The results indicate that the bipolar effect does not exist in the inverter of the nMOSFET. For the pMOSFET, the substrate process is the main factor determining the existence of the bipolar effect, and the bipolar effect can be effectively mitigated by the buried deep P^+ well. When a buried SO_2 layer is used instead of the deep P^+-well layer, the bipolar effect does not exist in the nMOSFET either.

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