Dispersion effect on the current voltage characteristic of AlGaN/GaN high electron mobility transistors*

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The current voltage (IV) characteristics are greatly influenced by the dispersion effects in AlGaN/GaN high electron mobility transistors. The direct current (DC) IV and pulsed IV measurements are performed to give a deep investigation into the dispersion effects, which are mainly related to the trap and self-heating mechanisms. The results show that traps play an important role in the kink effects, and high stress can introduce more traps and defects in the device. With the help of the pulsed IV measurements, the trapping effects and self-heating effects can be separated. The impact of time constants on the dispersion effects is also discussed. In order to achieve an accurate static DC IV measurement, the steady state of the bias points must be considered carefully to avoid the dispersion effects.

Keywords: dispersion effects, pulsed current voltage measurement, trap, self-heating

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1. Introduction

Because of the superior properties, such as wide band gap, high electron mobility, large electron saturated velocity and high breakdown voltage, the GaN-based high electron mobility transistors (HEMTs) become excellent candidates for high power, high frequency and high temperature microwave device applications.[1−4] Although the material growth and processing techniques have been greatly improved,[5,6] the presence of traps in the device is still one of the major issues limiting the performance of GaN-based devices. The kink effect, an anomalous increase in the drain current at relatively low drain source voltages, was first discovered in a floating body partially-depleted silicon on an insulator device due both to impact ionization current filtering and to drain-body coupling.[7] In InAlAs/InGaAs/InP HEMTs, it is shown that the time constant was strongly dependent on $V_{\rm ds}$ and $V_{\rm gs}$, the drain voltage and the gate voltage, and the kink turn-on dynamics correlated with impact ionization.[8] The kink dynamics were governed by hole emission and capture phenomena in AlGaAs/GaAs heterostructure field effect transistors.[9] Recently, the kink effect was also discovered in AlGaN/GaN HEMT devices, which was ascribed to the presence of slow traps in the GaN buffer.[10] Current collapse, as a result of which the output power at microwave frequency is considerably smaller than the expected one based on direct current (DC) characterization, is a severe phenomenon in AlGaN/GaN HEMTs.[11,12] Vetury *et al.*[13] proposed the possible locations of the traps, and found that the negative charge on the surface acted as a virtual gate which limited the drain current conduction in the channel. Binari *et al.*[14] showed that the current collapse was attributed to surface and buffer layer trapping. Deep level transient spectroscopy (DLTS) measurement was used to analyse traps corresponding to surface states and bulk defects.[15,16] All devices suffer from the self-heating effect, which is caused by the power dissipation, especially for the microwave power devices. The junction temperature is very high under high drain voltage for AlGaN/GaN HEMTs, and the current is badly reduced leading to current collapse.[17] The channel temperature is usually evaluated to calculate thermal resistance,[18,19] which is helpful in the evaluation of device reliability.

The device performance is greatly degraded by the trap-related and thermal effects. All these con-

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ditions above can be attributed to dispersion effects which are considered to be the discrepancy between the static and the dynamic device characteristics. Dispersion effects are sometimes referred to as memory effects or as dynamic bias,[20] which results in the inconsistency with the transconductance and output conductance from DC to radio frequency (RF) conditions.[21] The observed anomalous phenomena are given in this paper to explain the intrinsic mechanisms which are related to the dispersion effects.

2. Device structure and fabrication

The device presented in this study had a 0.2-μm-long and 1 × 100-μm-wide gate. The layers were grown on sapphire substrate by metal organic chemical vapour deposition. The epitaxial layer consists of a 100-nm AlN buffer, a 2-μm undoped GaN layer, a 22-nm $Al_{0.2}Ga_{0.8}N$ barrier layer, and a 3-nm GaN cap layer on the top. Ohmic contacts were formed by depositing the metals Ti/Al/Ni/Au (200 Å/1800 Å/550 Å/450 Å) followed by rapid thermal annealing at 870 °C for 50 s in nitrogen atmosphere, which resulted in a low Ohmic contact resistivity of $l0^{-6}$ $\Omega \cdot$cm. The gate recess was etched by using a fluorine-based and subsequent chlorine-based inductively coupled plasma process, and Ni/Au (400 Å/4500 Å) metals were evapourated for the T-shaped Schottky gate metallization. A 300-nm thick passivation layer of Si_3N_4 was deposited by using a plasma enhanced chemical vapour deposition system. The Si_3N_4 was then patterned and etched by using SF_6 plasma in an reactive ion etching system to open windows to the contact pads, a thick layer of Au normally plated to form the air-bridge structures.

3. Experiments and analyses

The DC current voltage (IV) measurement is made by the HP4155A, and two time factors are used here to investigate the trapping and thermal dependency of the IV curves. The hold time is the gate voltage spacing, and the output drain current will not be obtained although the gate voltage is applied until the hold time is reached. The spacing of each bias point in the drain voltage sweep is the delay time, during which the device does not work. The pulsed IV measurement is performed by the NC4832 provided by the 13th Institute of China Electronics Technology Group Corporation.

Figure 1 gives a set of IV curves with different hold times and zero delay time. The normal DC IV measurement is the same as the condition of delay time equal to hold time of 0 s. The kink effect which is accounted for the traps is observed in continuous wave (CW) sweep, and the electron capture and release processes can be seen clearly. The electrons are injected into the traps in the vicinity of the channel or the device surface when the drain voltage V_{ds} is applied; but as the voltage increases gradually, the trapped electrons have enough time to escape from the traps, and the anomalous behaviour occurs around the knee voltage where the drain current I_{ds} is close to saturation. If the hold time is set to be a few seconds instead of zero as shown in Fig.1, the drain current is only sampled after the hold time is reached, so the trap effects have time to respond to the signal in the period, and then the kink effect is alleviative or even disappeared. Because the modulation of the channel by the gate voltage V_{gs} is finished in the hold time, the trap states have been fixed. However, the self-heating still influences the DC IV characteristic, which degrades the drain current at higher drain voltage.

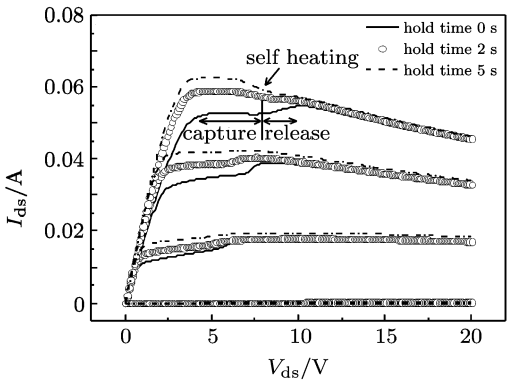


Fig. 1. The DC IV curves with different hold times when the delay time is 0 s. V_{gs} is from −3 V to 1 V with step of 1 V.

As shown in Fig. 2, if a delay time is added between every bias point, the trapping and thermal effects both have time to reach the steady state at each measurement point. The drain currents of D2H0 (the delay time is 2 s and the hold time is 0 s) and D5H0 (the delay time is 5 s and the hold times is 0 s) conditions are larger than those of D0H2 and D0H5 conditions respectively. Although they all suffer from the self-heating effects, there is a little time to dissipate the produced heat in the channel with the nonzero de-

lay time. The longer the delay time is, the weaker the self-heating effect is.

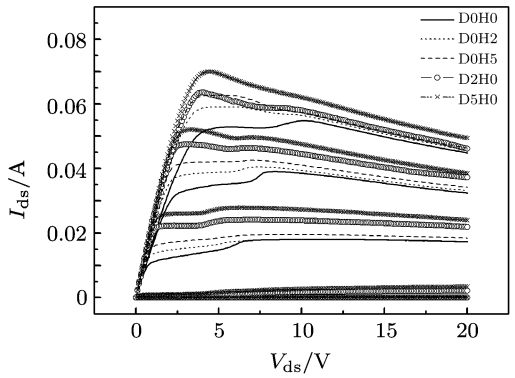


Fig. 2. The DC IV curves with different delay and hold times. V_{gs} is from −3 V to 1 V with step of 1 V.

It is indicated that the trapping and thermal effects have a great impact on the static IV measurement. To achieve accurate DC IV curves, enough time must be taken to let every bias operating point reach the steady state to alleviate the dependence on dispersion effects.

As shown in Fig. 3, the operating condition (I) when sweeping down to the measurement points is different from the condition (II) when sweeping up to the same points. Compared with the drain current of $V_{gs} = 1$ V in condition (II), the drain current of condition (I) is bigger and shows less kink effect, but the later curves in condition (I) all have more obvious kink effect than that in condition (II). It can be concluded that if the device is driven by very high voltage and current, more traps induced in the material will take part in the trapping and detrapping processes. More detailed research has been investigated by DLTS measurements, and it shows that high voltage and high DC current stressing can lead to the increase in the density of deep-levels and to more traps in the device.[16,22,23]

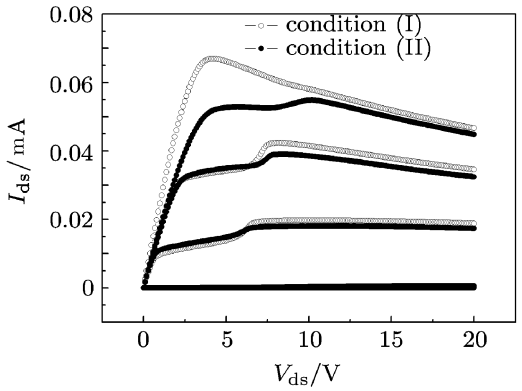


Fig. 3. The DC IV curves with different sweeping sequences. Condition (I): V_{gs} is from 1 V to −3 V with step of −1 V; condition (II): V_{gs} is from −3 V to 1 V with step of 1 V.

The gate and drain are driven respectively by pulse and step modes with four conditions identified as (a), (b), (c), (d) in Fig. 4. The trapping effect is usually neglected at the bias condition of $V_{gs} = 0$ V and $V_{ds} = 0$ V.[24] If the pulse width is shorter and the duty cycle is small enough to prevent the heating, the IV characteristics without dispersion effects can be obtained at the condition (a). It is noticeable that conditions (a) and (c) are almost the same. The pulse mode at gate has little influence on the IV curves, which means that surface states or traps in the barriers layer can be negligible because of the passivation of the Si_3N_4 in the device.[25] The current collapse of condition (b) is more serious than that of condition (a). It is demonstrated that the traps in the buffer layer interact with the two-dimensional electron gas (2DEG), and the pulsed mode at drain can greatly improve the drain currents. ondition (d) has noteworthy current collapse, the same as the DC IV curves. It is concluded that the drain conditions have a great impact on the performance of the device rather than the gate conditions.

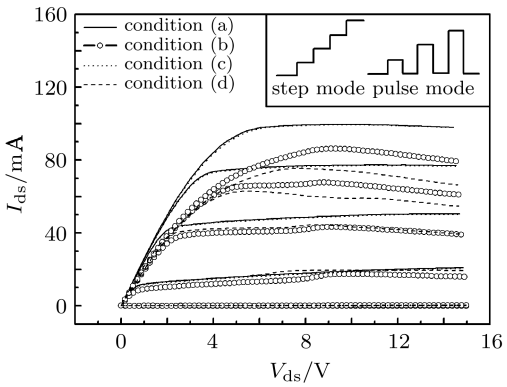


Fig. 4. The IV curves with different measurement modes with the bias at $V_{gs} = 0$ V and $V_{ds} = 0$ V, and 2-μs pulse width, 1-kHz pulse rate. The pulse mode and step mode are shown in the insert. Condition (a), gate pulse and drain pulse; condition (b), gate pulse and drain step; condition (c), gate step and drain pulse; condition (d), gate step and drain step.

As shown in Fig. 5, the self-heating effect is the dominant property of DC characteristics, a great drain current reduction is observed in CW compared with the pulsed condition. To distinguish the contribution of trapping from the self-heating effects, pulsed IV measurement is performed at two different bias points but almost with the same DC power dissipation.[26] The two bias conditions of $V_{gs} = -0.69$ V and $V_{ds} = 7.5$ V, and $V_{gs} = -1.31$ V and $V_{ds} = 15$ V in the isothermal counter have the same power of 175 mW. The trapping and thermal effects have an

effect on both of them compared with the condition of $V_{gs} = 0$ V and $V_{ds} = 0$ V, under which condition we can consider that trapping and self-heating effects do not exist. The drain currents at $V_{gs} = -1.31$ V and $V_{ds} = 15$ V are smaller than those at $V_{gs} = -0.69$ V and $V_{ds} = 7.5$ V when the self-heating effects can be considered equivalent, which proves that high drain voltage can induce more traps interacting with the carriers in the channel. The traps may be in the surface, the interface between two materials, even in the epitaxial layers.

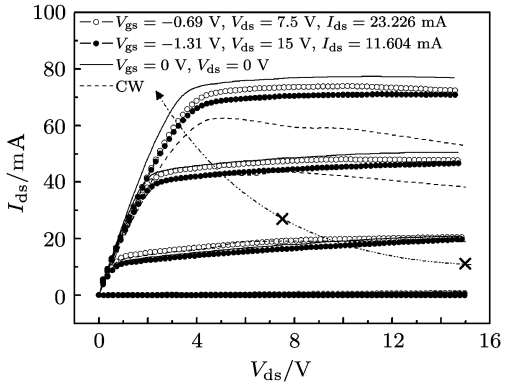


Fig. 5. The constant DC power dissipation at two bias conditions (×) with 2-μs pulse width and 1-kHz pulse rate.

4. Discussion

The generation of traps has many different reasons. The unwanted impurities (donors or acceptors) and defects will be produced in the growth of the epitaxial layers, some of which may introduce deep levels and create semi-insulating layers by pinning the Fermi-level at the middle of the bandgap. Due to the different lattice constants and thermal expansion constants between each of the materials, the dislocations and interface states also appeared in the heterostructure interfaces, even in the materials themselves. Although the spontaneous and piezoelectric polarizations in the AlGaN/GaN material provide high 2DEG density, the surface states are also involved in the HEMT devices.[27] As shown in Fig. 6, the traps may exist wherever in the device. There are more surface states in the surface between the gate and drain space, interface states between every two layers, and traps in the barrier layer and buffer layer, etc.[28]

The electrons in the channel are trapped when there is enough activation energy that can come from the voltage or the heat, sometimes even from the illumination. They can also be detrapped if the time is long enough or they are activated again. The electrons interact with the traps through the variations of the activation energy when the conditions of the device change. The changes of the trap state result in the redistribution of the depleted region, and the change rate of the trap state is the limiting mechanism of the charge. Consequently, the behaviour of traps is the main inherent cause of dispersion effects, which are strongly correlated to the alterations of bias voltage and the signal frequency.[20]

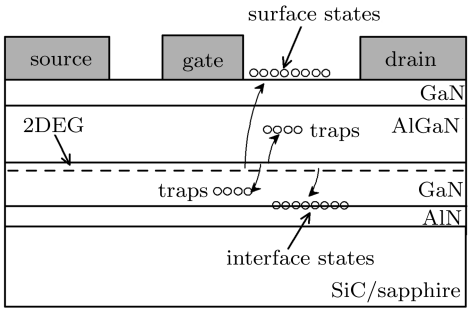


Fig. 6. The location of traps and defects in AlGaN/GaN HEMTs.

The kink effects and the current collapse are trap-related phenomena. The kink effects occur at low drain voltage with DC or low frequency condition. Some electrons can be trapped by the deep levels when the channel is open. If the trapping process can follow the low frequency signal, the electrons can be released later, leading to an unusual drain current increase. When the RF signal is superimposed on the device, the trap levels capture the electrons, but have no time to release them. With the increase of drain voltage, there will be more induced deep trap levels in the buffer layers or device surface being involved. The drain current drops a lot at higher drain voltage as shown in Fig. 5. In Fig. 7, the induced trap levels at high stress can capture more electrons, which obviously decrease the drain source current, and then the current collapse is observed instead of the kink effects. Therefore, the shallow trap levels are related to the kink effects at lower drain voltage for low frequency, and the current collapse is not only related to the shallow levels, but also bound up with deeper trap levels at high drain voltage.

As discussed above, traps are the most important reason for the kink effects. In Figs. 1 and 2, the kink effects are studied by the time factors with HP4155A. The impact ionizations can take place under all conditions in Figs. 1 and 2, but only the D0H0 condition shows the dramatic kink effects, and the other conditions have ruled out the influence of traps, so it can

be concluded that the trap effect is the main cause of the kink effects. With the impact ionization or floating-body effect only,[7,8] the kink effects cannot be apparently found in AlGaN/GaN HEMTs.

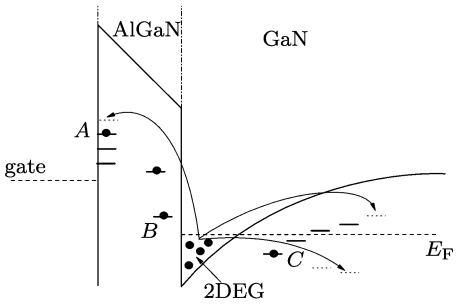


Fig. 7. The influence of the trap or deep levels on carriers in AlGaN/GaN HEMTs. A: the surface states in the device surface, B: the traps in the AlGaN barrier, C: the traps in the GaN buffer. Solid lines are existed trap levels, dashed lines are induced trap levels by high drain voltage or large drain current.

From Figs. 3–5, we can see that drain voltage influences the state of traps significantly, and higher drain voltage can excite more trap levels in the device, which leads to serious current collapse. When high voltage is applied to the drain source terminal, it is inevitable to dissipate much heat in the channel. The electron velocity in the channel decreases due to thermal effects on the mobility and saturated velocity, which gives rise to the negative output conductance at high drain bias. This is another kind of current collapse.

The thermal emission rate of the trap $e_{\rm n,p}$ depends on the trap energy $E_{\rm t}$ and the temperature T, and it could be expressed as[29]

$$\begin{aligned} e_{\rm n,p} &= \frac{N_{\rm n,p}\sigma_{\rm n,p}v_{\rm n,p}}{g}\exp\left(\frac{-E_{\rm t}}{kT}\right) \\ &= AT^2\exp\left(\frac{-E_{\rm t}}{kT}\right), \end{aligned} \tag{1}$$

where $N_{\rm n,p}$ is the effective density of states in the conduction band or valence band, $\sigma_{\rm n,p}$ is the capture cross section of the trap, $v_{\rm n,p}$ is the carrier velocity, and g is the level degeneracy factor.

High voltage can generate more energy to the trap levels with large activation energy $E_{\rm t}$, and this is the reason for the excitation of deeper trap levels under high drain bias. It is perceived that the behaviour of the trap is greatly affected by the temperature, and the heat makes the traps so active that they can easily trap or detrap the electrons.

The correlation between $e_{\rm n,p}$ and T can be used to confirm the location of the traps by DLTS,[16] and $e_{\rm n,p}$ is considered to have a relationship with trap relaxation time, which is the time that the trap takes from one steady state to another. As the time constant of the trap has the same variation trend of the relaxation time, the $e_{\rm n,p}$ can be used to estimate the time constant of the traps.

The capture and release of the electrons by traps or surface states greatly affect the free carrier concentrations and carrier transport properties, which results in the current fluctuation in the channel. The traps in the device introduce deep levels, whose depth confirms the locations of the traps. There exists a time constant which can be expressed as $\tau_{\rm trap}$ related to the trapping process responding to the change of the signal, and the rate of charge trapping is typically in the range from millisecond to second.[30] The same as the current gain cutoff frequency of the transistor, the cutoff frequency of the trap can be defined by

$$f_{\rm trap} = \frac{1}{2\pi\tau_{\rm trap}}. \tag{2}$$

The cutoff frequency of traps can be used to judge whether the traps respond to the signals applied to the device. When DC IV measurement is performed on the device, if the signal is too slow in comparison with the $f_{\rm trap}$, the trapping and detrapping processes can be discovered in the DC IV curves. In high frequency operation, the signal alters so fast that the traps cannot follow the variations of the RF signal. The traps at different regions correspond to different time constants, and the quantity of traps responding to the signal is diverse when the conditions of the device change, which will result in trap dependent dispersion with different extent.

As a power device, it suffers a lot of power dissipation when AlGaN/GaN HEMT is operated in the high drain voltage condition. Due to the undesirable thermal effects, the current in the channel decreases a lot at high power level. A sub-circuit shown in Fig. 8 is often introduced to model the power dissipation as[31]

$$P_{\rm diss}(t) = \frac{(T-T_0)}{R_{\rm th}} + C_{\rm th}\frac{{\rm d}(T-T_0)}{{\rm d}t}, \tag{3}$$

where T is the channel temperature and T_0 is the ambient temperature.

The thermal resistance $R_{\rm th}$ is defined by

$$R_{\rm th} = \frac{T_1 - T_2}{P_{\rm diss}}, \tag{4}$$

where T_1 and T_2 are two isothermal surface temperatures, and $P_{\rm diss}$ is the dissipation power.

It is used to characterize the static temperature difference between two isothermal surfaces. The thermal capacitance $C_{\rm th}$ can be obtained by

$$C_{\rm th} = \rho c V, \tag{5}$$

where ρ is the material density, c is the specific heat of the material, and V is volume of the material.

It predicts the thermal dynamic variation prior to thermal equilibrium. The cutoff frequency of thermal can be defined in the same way as

$$f_{\rm th} = \frac{1}{2\pi\tau_{\rm th}} = \frac{1}{2\pi R_{\rm th} C_{\rm th}}. \tag{6}$$

The thermal time constant $\tau_{\rm th}$ is the product of $R_{\rm th}$ and $C_{\rm th}$, and it can be also obtained by transient IV measurement directly.[32,33]

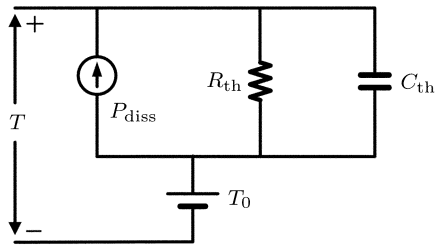


Fig. 8. The thermal RC equivalent sub-circuit.

The thermal time constant is generally of the order from microseconds to milliseconds. If the rate of the temperature change is slower than $f_{\rm th}$, which means that the thermal time constant is larger than the period of the RF signal, then the self-heating effect is negligible as the channel temperature cannot follow the instantaneous power dissipation. On the contrary, if the heat conduction is fast enough to follow the power dissipation, the drain current and the output power will reduce a lot with obvious self-heating effect.

To differentiate trap effects from thermal effects, the time constants must be separated from each other by a specific frequency signal. For example, when $\tau_{\rm trap} < \tau_{\rm th}$ or $f_{\rm trap} > f_{\rm th}$, if the frequency is higher than $f_{\rm trap}$, trapping and thermal effects cannot happen. If the frequency is higher than $f_{\rm th}$ but lower than $f_{\rm trap}$, only the trapping effect can be observed. If the frequency is lower than $f_{\rm th}$, both of them will take effect and we cannot tell the difference. It is the time dependency of the traps or thermal that leads to dispersion effects, and the time constant is a good reference for further research into dispersion effects.

It is more accurate for DC IV curve to portray the characteristics of the device after the bias point has settled to establish a constant quiescent condition. In order to ascertain that, the bias condition should be holding on sufficient time that is longer than not only the trap time constants but also the thermal time constants. The pulsed IV measurement is often used to investigate the dispersion effects, and there exists a unique IV characteristic set at each bias point. According to the different cutoff frequencies, the trapping effects and self-heating effects can be separated from each other. These effects are related to some frequency response to the signal that leads to the differences between DC and RF characteristics of the device.

5. Conclusion

The DC IV characteristic with different hold time and delay time, and also the pulsed IV characteristic have been used to investigate the trap and thermal phenomena, whose bias and frequency dependency result in the dispersion effects. The traps at different locations in the device lead to various behaviours, which are known as kink effects, current collapse, etc. It is observed that the drain voltage is the essential factor to current collapse when the device is working, and more traps are induced in high drain voltage condition. The trap time constant and thermal time constant are presented, and they are very instructional in obtaining exact static IV curves of the device, which are important for predicting the RF operation.

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