An improvement to computational efficiency of the drain current model for double-gate MOSFET*

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(Received 18 January 2011; revised manuscript received 28 February 2011)

As a connection between the process and the circuit design, the device model is greatly desired for emerging devices, such as the double-gate MOSFET. Time efficiency is one of the most important requirements for device modeling. In this paper, an improvement to the computational efficiency of the drain current model for double-gate MOSFETs is extended, and different calculation methods are compared and discussed. The results show that the calculation speed of the improved model is substantially enhanced. A two-dimensional device simulation is performed to verify the improved model. Furthermore, the model is implemented into the HSPICE circuit simulator in Verilog-A for practical application.

Keywords: computational efficiency, compact model, double-gate, MOSFET

PACS: 73.40.Ty, 73.40.Qv, 61.44.Br **DOI:** 10.1088/1674-1056/20/9/097304

1. Introduction

With the conventional bulk MOSFET technology scaling down towards the practical limit,[1] double-gate (DG) MOSFETs as one of the most promising devices have attracted substantial research interests due to the superior short channel effect immunity, the volume inversion, and the near ideal sub-threshold slope.[2,3] To predict or to simulate the DG MOSFET-based circuit performance in the future, accurate and time computationally efficient compact models for the DG MOSFETs are desirable. Much work has been devoted to the modeling and the simulation of the DG MOSFETs.[4−13] The compact core models for the undoped DG MOSFETs are well reviewed in Ref. [14].

A unified compact model for the double-gate MOSFETs, which is valid for symmetric, asymmetric, and independent-gate operation modes as well as computationally efficient, is absolutely required. We have proposed a calculation method to improve the efficiency of the potential computation in a previous unified model.[15] In this paper, a drain current model based on the improved potential model in Ref. [16] is extended and discussed, and different calculation methods are compared in detail. The model is validated by the extended two-dimensional (2D) device simulation (TCAD).[17] The proposed model is implemented into the HSPICE in Verilog-A. The advantages and the limits of the model are discussed.

2. Model improvement

Figure 1 shows the schematic structure of an undoped double-gate MOSFET, where x is the direction across the silicon film thickness, y is the horizontal direction along the channel, $t_{\rm si}$ and $t_{\rm oxf}$ ($t_{\rm oxb}$) denote the thicknesses of the silicon film and the front (back) gate oxide, respectively, $V_{\rm gf,apply}$, $V_{\rm gb,apply}$, and $V_{\rm ds,apply}$

*Project supported by the National Natural Science Foundation of China (Grant No. 60876027), the National Science Foundation for Distinguished Young Scholars of China (Grant No. 60925015), the National Basic Research Program of China (Grant No. 2011CBA00600), and the Fundamental Research Project of Shenzhen Science & Technology Foundation, China (Grant No. JC200903160353A).

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are the terminal voltages.

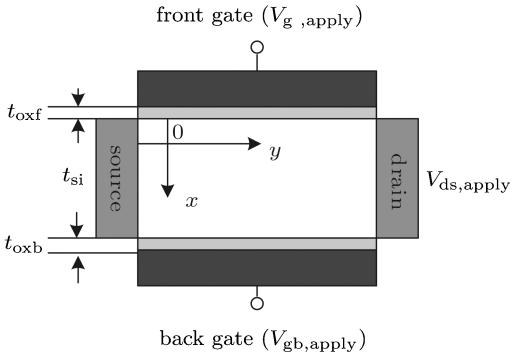


Fig. 1. Schematic structure of a double-gate MOSFET.

As the previous research results have shown[8,9,11], there are two solutions of the Poisson's equation for the DG MOSFET, the trigonometric and the hyperbolic solutions. Therefore, the key step is to decide which solution should be selected for different bias conditions. A critical voltage $V_{\rm critical}$, which is a very important intermediate parameter during the calculation process, is defined to determine the solution adopted.[9,11] In this paper, the critical voltage is denoted as $V_{\rm cmcritical}$, which has the form[11]

$$V_{\rm cmcritical} = \frac{V_{\rm dm}}{2} + 2\phi_{\rm t} \ln\left[\frac{4L_{\rm d}}{t_{\rm si}\,(s-1)}\right] + \frac{4\phi_{\rm t} r_{\rm f}}{s-1}, \quad (1)$$

where $V_{\rm dm} = V_{\rm gb} - V_{\rm gf}$, $V_{\rm gf} = V_{\rm gf,apply} - \Delta\phi_{\rm f}$, and $V_{\rm gb} = V_{\rm gb,apply} - \Delta\phi_{\rm b}$. The $\Delta\phi_{\rm f}$ and $\Delta\phi_{\rm b}$ are respectively the front and the back gate work function differences, both of which are set to zero in this work. The $\phi_{\rm t}$ is the thermal voltage, $L_{\rm d}$ denotes the intrinsic Debye length, $r_{\rm f} = \varepsilon_{\rm si} t_{\rm oxf}/t_{\rm si}/\varepsilon_{\rm ox}$, and $\varepsilon_{\rm si}(\varepsilon_{\rm ox})$ is the permittivity of silicon (silicon oxide). Variable s can be obtained numerically from the equation

$$\ln\left(\frac{s+1}{s-1}\right) + 2\left(\frac{r_{\rm f}}{s-1} + \frac{r_{\rm b}}{s+1}\right) + \frac{V_{\rm dm}}{2\phi_t} = 0, \quad (2)$$

where $r_{\rm b} = \varepsilon_{\rm si} t_{\rm oxb}/t_{\rm si}/\varepsilon_{\rm ox}$.

Figure 2(a) demonstrates the establishment of an operation region or mode with different back-gate biases. The relationship between the critical voltage ($V_{\rm cmcritical}$) and the common mode voltage ($V_{\rm cm}$) varies with the bias condition. The common mode voltage is defined as

$$V_{\rm cm} = \frac{1}{2}\left[(V_{\rm gb} - \Delta\phi_{\rm b}) + (V_{\rm gf} - \Delta\phi_{\rm f})\right] - V_{\rm ch}, \quad (3)$$

where $V_{\rm ch}$ is the channel voltage. The whole plane is divided into two regions corresponding to the trigonometric ($V_{\rm cm} > V_{\rm cmcritical}$, mode 2) and the hyperbolic ($V_{\rm cm} < V_{\rm cmcritical}$, mode 1) solutions, respectively. During the calculation of $V_{\rm cmcritical}$, the gate voltages and the structural parameters corresponding to the two gates are exchanged for each other under the condition that the back-gate voltage is higher than the front-gate voltage.

Recently, some efforts have been devoted to the convergence and the computation problems resulted from the Poisson's equation for the DG MOSFET,[12,13] in which computing the critical voltage $V_{\rm cmcritical}$ is switched to computing the critical voltages $V_{\rm gfcr}$ and $V_{\rm gbcr}$ of $V_{\rm gf}$ and $V_{\rm gb}$, respectively. In fact, the expressions for $V_{\rm gfcr}$ and $V_{\rm gbcr}$ in Refs. [12] and [13] are mathematically equivalent. As shown in Fig. 2(b), lines Γ_1 and Γ_2 correspond to $V_{\rm gbcr}$ and $V_{\rm gfcr}$ under the conditions of $t_{\rm si} = 10$ nm, $t_{\rm oxf} = 2$ nm, $t_{\rm oxb} = 40$ nm, and $V_{\rm ch} = 0.5$ V. When $V_{\rm gf} > V_{\rm gb}$, $V_{\rm gb}$ is compared with $V_{\rm gbcr}$ to establish the region of operation. If $V_{\rm gb} > V_{\rm gbcr}$, the trigonometric solution (mode 2) is adopted. Otherwise, the hyperbolic solution (mode 1) is selected. Similarly, the region of operation is determined by comparing $V_{\rm gf}$ with $V_{\rm gfcr}$ when $V_{\rm gf} < V_{\rm gb}$.

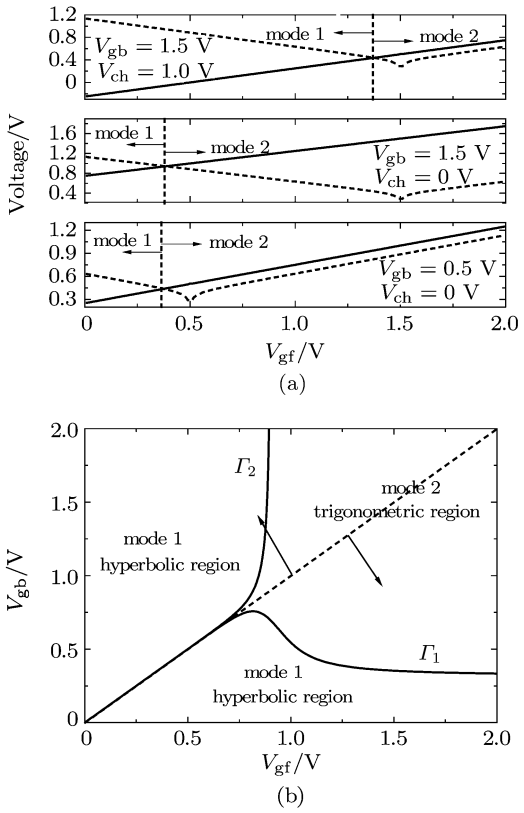


Fig. 2. Establishment of the operation region or operation mode based on (a) the numerical calculation of $V_{\rm cmcritical}$ (solid lines for $V_{\rm cm}$, dashed lines for $V_{\rm cmcritial}$) and (b)the calculation of $V_{\rm gfcr}$ and $V_{\rm gbcr}$ with the Lambert W function.

Although the Lambert W function is used to simplify the computational procedure in Refs. [12] and [13], it does not improve the computational efficiency as expected. Therefore, the critical voltage $V_{\rm cmcritical}$ is still used to establish the operation region in this paper. The calculation of $V_{\rm cmcritical}$ based on a numerical method with an appropriate initial guess is faster than that of $V_{\rm gfcr}$ in the form of the Lambert W function, which will be shown in the next section.

Based on the Jacobian–Newton method, an improved calculation method for the Poisson's equation for generic DG MOSFETs has been proposed in Ref. [15]. In this paper, the improved calculation method is implemented into the final drain current model given in Ref. [11] to enhance the computational efficiency.

Finally, to implement the compact model in the HSPICE, the model has been written in Verilog-A, which has advantages over the C language. Moreover, the model is tested on an inverter circuit.

3. Results and discussion

The improved drain current model is validated and discussed in detail in this section by comparing with the TCAD results. The corresponding parameters are given as (unless otherwise specified) $t_{\rm si}$ = 20 nm, $t_{\rm oxf} = t_{\rm oxb} = 2$ nm. The width and the length of the device are $W = L = 1$ μm, and the electron mobility is $\mu = 400$ cm^2·V^{-1}·s^{-1}.

Figure 3 shows the verification of the characteristics predicted by the model by using the device simulation. Figure 3(a) plots the drain current versus the front-gate voltage under a variety of back-gate voltages, which inflects the tuning ability of the back-gate voltage on the threshold voltage. Figure 3(b) demonstrates the output characteristics of the DG MOSFET with the zero back-gate voltage. It is observed that the results given by the model match the 2D simulation results very well.

In addition, the calculation efficiency is greatly improved, as shown in Table 1. Table 1 displays the runtime comparison of the models based on a personal computer with a four-core CPU. The runtime is taken by reproducing the procedure 100 times, and the computations are performed on matlab.[18] The average runtime for one-time procedure is obtained by dividing the total time by 100. In this paper, the one-time procedure means that the drain current is calculated for various front-gate voltages from 0 V to 2 V with a step of 0.1 V at $V_{\rm gb} = 0$. The results show that the computation speed of the improved model is dramatically enhanced. The improved model with the operation modes determined by $V_{\rm cmcritical}$ runs faster than that with modes determined by $V_{\rm gfcr}$ and $V_{\rm gbcr}$, because it takes more time to calculate the Lambert W function embedded in matlab.

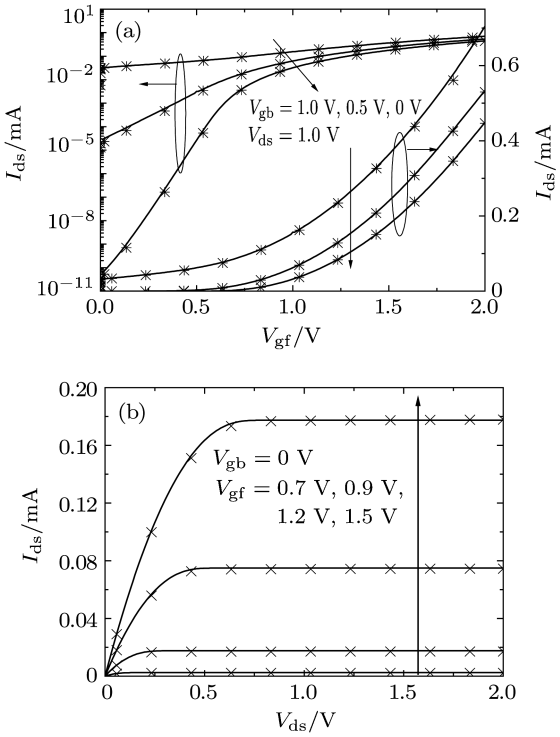


Fig. 3. Comparison of characteristics obtained from the model and the simulation: (a) $I_{\rm ds} - V_{\rm gf}$ curves with different back-gate biases, (b) output characteristics with various front gate voltages. Lines denote model predications, symbols denote TCAD results.

Table 1. Runtime comparison of drain current models.

Model	Average runtime/s
Previous model in Ref. [11]	95.50
Improved model with $V_{\rm gfcr}$ and $V_{\rm gbcr}$	13.75
Improved model with $V_{\rm cmcritical}$	2.16

With the improved computational efficiency, the compact drain current model is easily implemented into the circuit simulator HSPICE in Verilog-A. Figure 4 shows direct current (DC) characteristics of an inverter with the improved DG MOSFET model implemented. The back gates of the two devices in the inverter circuit are set to different voltages, and the applied power voltage is set to 2 V. It can be seen that the back-gate voltage has the potential of tuning the characteristics of the inverter, which may cause new circuit topology. However, there are still some converge problems in the transient simulation, which

may result from many causes including the model itself. The problem still can not be well solved, and is still under investigation by us.

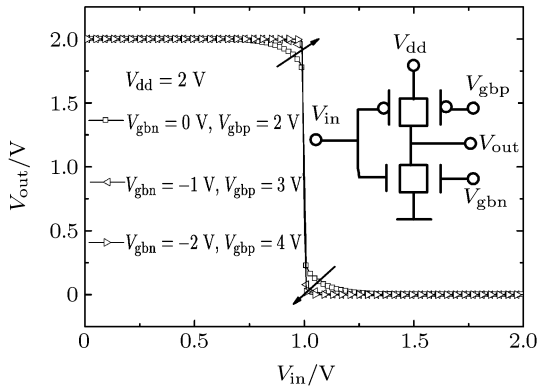


Fig. 4. The DC characteristics of an inverter with the improved DG MOSFET model implemented in the HSPICE. The parameters are shown in the plot.

4. Summary

Based on our previous potential model, an improved computationally efficient drain current model for DG MOSFETs is presented in this paper, and different models are compared and discussed. A 2D device simulation is performed to validate the proposed model. The comparison results illustrate good agreement between the model and the simulation results. Based on the Jacobian–Newton method with a suitable initial guess, the calculation speed of the model is greatly enhanced, which allows the model to be implemented into the HSPICE for the practical application. There is still much work left to improve the model, such as the incorporation of the advanced effect, which will be our next work.

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