Flat-band voltage shift in metal-gate/high-k/Si stacks*

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In metal-gate/high-k stacks adopted by the 45 nm technology node, the flat-band voltage ($V_{\rm fb}$) shift remains one of the most critical challenges, particularly the flat-band voltage roll-off ($V_{\rm fb}$ roll-off) phenomenon in p-channel metal-oxide-semiconductor (pMOS) devices with an ultrathin oxide layer. In this paper, recent progress on the investigation of the $V_{\rm fb}$ shift and the origin of the $V_{\rm fb}$ roll-off in the metal-gate/high-k pMOS stacks are reviewed. Methods that can alleviate the $V_{\rm fb}$ shift phenomenon are summarized and the future research trend is described.

Keywords: flat-band voltage shift, $V_{\rm fb}$ roll-off, metal gate, high-k dielectrics

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1. Introduction

As a result of the aggressive downscaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) in the semiconductor industry, metal and high-k oxides have replaced polycrystalline silicon and SiO_2 as the gate materials in the 45 nm MOS technology and beyond.[1,2] High-k oxides presently still underperform in comparison with SiO_2 in some aspects, including the threshold voltage ($V_{\rm th}$), mobility and defects.[3,4] Among them, the influence of the flat-band voltage ($V_{\rm fb}$) on the threshold voltage must be controlled to a certain level. Unfortunately, as metal gate/high-k stacks are applied in 45 nm MOS technology, substantial shifts in $V_{\rm fb}$ have been observed, especially along the negative direction in the p-channel MOS (pMOS).[5] In spite of the shrinking equivalent oxide thickness (EOT), the $V_{\rm fb}$ roll-off phenomenon is also observed.[6] Many factors can shift $V_{\rm fb}$ to the negative direction in the pMOS stacks, for example, Fermi-level pining, oxygen vacancies with positive charge in the dielectric layer and dipoles at the bottom interfacial layer (high-k/SiO_2 or interfacial SiO_2/Si layer).[7−12] Various methods have been proposed to reduce the $V_{\rm fb}$ shift, such as inserting capping layers, decreasing annealing temperature and doping.[10−14] In this paper, recent progress and future challenges pertaining to the $V_{\rm fb}$ shift to the negative direction in the pMOS as well as the origin of the $V_{\rm fb}$ roll-off phenomenon are reviewed. In addition, methods to alleviate the magnitude of the $V_{\rm fb}$ shift are summarized and the future research trend is discussed.

2. Factors affecting $V_{\rm fb}$ in pMOS

Since high-k dielectrics are introduced into MOSFETs to reduce the leakage currents in 45 nm technology, it is necessary to replace the poly-Si with a metal that has an appropriate work function as the gate electrode. The metal gate electrode can not only eliminate the gate depletion and the boron penetration, but also greatly reduce the gate resistance.[15] Unfortunately, in metal-gate/high-k pMOS stacks, $V_{\rm fb}$ shifts of about −0.7 V compared with those of the SiO_2 dielectric have been observed, as shown in Fig. 1.[8,16] In particular, the aggressive negative $V_{\rm fb}$ shift called

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the $V_{\rm fb}$ roll-off emerges with the scaling down of the ultrathin EOT, as shown in Fig. 2.[6]

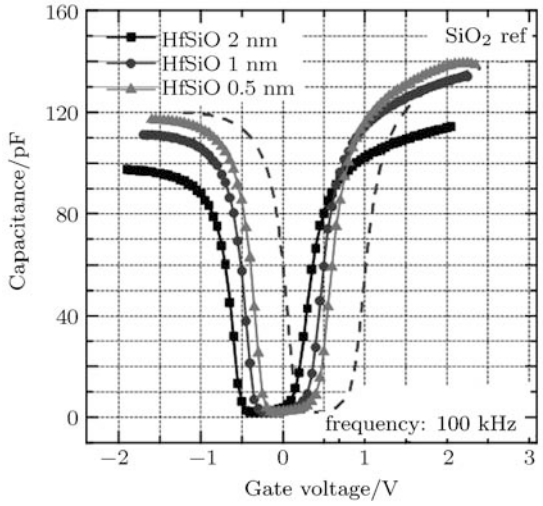


Fig. 1. Capacitance–voltage (C–V) characteristics of a pMOS with different high-k thicknesses. The area of the capacitance is 1.2×10^{-4} cm^2.[16]

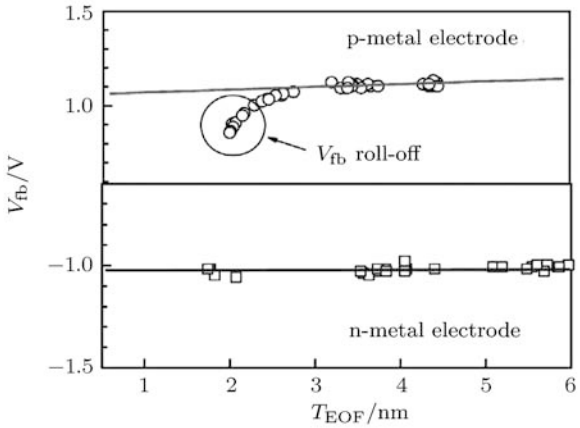


Fig. 2. The $V_{\rm fb}$–$T_{\rm EOT}$ curves of a typical n-metal electrode and a p-metal electrode. The p-metal electrode MOS shows $V_{\rm fb}$ roll-off towards the mid-gap as the thickness of the interlayer SiO_2 is reduced.[6]

Generally, in metal-gate/high-k pMOS stacks, $V_{\rm fb}$ can be expressed as[10,17]

$$V_{\rm fb} = \phi_{\rm m,eff} - \phi_{\rm s} - \phi_{\rm D} - \frac{1}{\varepsilon_{\rm h}} \int_0^{t_{\rm h}} x \cdot \rho_{\rm b}(x) {\rm d}x - \frac{1}{\varepsilon_{\rm ox}} \int_{t_{\rm h}}^{t} x \cdot \rho_{\rm i}(x) {\rm d}x - \frac{Q_{\rm i} \times t_{\rm h}}{\varepsilon_{\rm h}} - \frac{Q_{\rm f} \times T_{\rm EOT}}{\varepsilon_{\rm ox}}, \quad (1)$$

where $\phi_{\rm m,eff}$ is the effective work function (EWF) of the metal gate, $\phi_{\rm s}$ is the work function of the silicon, $\phi_{\rm D}$ is the potential difference due to the dipole layer, $\rho_{\rm b}$ and $\rho_{\rm i}$ are the charges in the high-k and the bottom oxides, respectively, $Q_{\rm i}$ and $Q_{\rm f}$ are the charges at the interfaces between the high-k and the bottom oxides and between the bottom oxide and the Si substrate, respectively, $t_{\rm h}$ is the physical thickness of the high-k layer, t is the thickness of the whole dielectric layer, $T_{\rm EOT}$ is the equivalent oxide thickness, $\varepsilon_{\rm h}$ and $\varepsilon_{\rm ox}$ are the dielectric constants of the high-k layer and the interlayer SiO_2, respectively.

Based on Eq. (1), the negative shift of $V_{\rm fb}$ in the pMOS may be caused by the EWF, which is closely related to the Fermi-level pining. Meanwhile, the positively charged defects generated in the high-k layer or in the interlayer SiO_2 (IL SiO_2) and the dipoles formed at the interface can also influence the negative shift of $V_{\rm fb}$. The details are reviewed in the following sections.

2.1. EWF influenced by the Fermi level pinning

In the pMOS stack, the EWF is much lower than the corresponding work function in vacuum. Research has shown that the difference is induced by the pinning of the metal Fermi-level on the dielectric (denoted as the Fermi-level pining) and can be characterized with the pinning factor as

$$\phi_{\rm m,eff} = \phi_{\rm CNL} + S \cdot (\phi_{\rm m} - \phi_{\rm CNL}), \quad (2)$$

where $\phi_{\rm CNL}$, S and $\phi_{\rm m}$ are the charge neutrality level (CNL), the pinning factor and the vacuum work function of the gate electrode, respectively. The Fermi-level pinning can be an origin of the $V_{\rm fb}$ shift in metal-gate/high-k stacks (as shown in Eq. (2)) and makes it much difficult to find the proper metal gate materials to obtain a small $V_{\rm fb}$. This is particularly acute in the pMOS.[15] The Fermi-level pinning phenomenon is commonly caused by metal induced gap states (MIGS).[8] However, a deviation between the MIGS line and the experimental data has been found in metal/high-k MOS stacks for 45 nm technology node and beyond, which implies that there may be other factors influencing the Fermi-level pinning. Recently, it has been shown that the electron state density in the metal gate is also an important factor.[18]

2.1.1. Metal-induced gap states

In the calculation of the bulk material band structure, it is assumed that the size of the crystal is infinite. When the finite size of the crystal is taken into account, the electron wave function is altered and

states that were forbidden within the bulk gap are allowed at the surface. Thus, when a metal gate contacts a semiconductor layer or a dielectric layer, the wave functions of the electrons in the semiconductor or in the dielectric must keep continuity at the interface. The gap states will decay deeper into the semiconductor or the dielectric. The states are called MIGS, which are intrinsic states in the band gap. The charge transfers along the gap states are due to the difference between the metal Fermi level and the high-k's CNL. The charging of these states gives rise to a dipole across the interface, which distorts the Fermi level and induces the Fermi-level pinning. Generally, the factor caused by the MIGS can be denoted by a constant pinning coefficient S for a given high-k dielectric and can be expressed as[19]

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}, \tag{3}$$

where ε_∞ is a dielectric constant. The S characterizes the difference between the work function in vacuum and the EWF of the metal gate on the high-k layer. The dependence on dielectric constant ε_∞ suggests that dielectrics with higher dielectric constants will induce larger pinning.[15] By adopting a value of $S = 0.53$ for HfO_2, a linear correlation between the work function and the EWF of different metal gates on HfO_2 can be predicted.[15]

However, it is also found that the EWFs predicted by the MIGS are inconsistent with experimental data. Wen *et al.* have analysed recent experimental results addressing the intrinsic and the extrinsic factors controlling the EWF of the metal gate on Hf-based high-k layers and found that the extrinsic factors also played an important role.[20] The investigation of the properties at the Re/HfO_2 interface in the Re/HfO_2/SiO_2/Si MOS stack showed that the Fermi level was partially pinned at the Re/HfO_2 interface extrinsically and the associated dipole was about 0.5 eV.[20] In addition, the difference between experimental results and the prediction of the MIGS mode was also observed.[21,22] The EWF at the metal/HfSiON pMOS stacks has been examined by Koyama *et al.*[23] In order to eliminate the extrinsic defects at the interface, the metal/HfSiON (Hf ratio= 50%) stacks were prepared by thermal evaporation of Pt, Au and Al. Post-deposition annealing was not performed to avoid the interfacial reactions.[24] When the EWF was plotted as a function of the vacuum work function, the slope of the metal/HfSiON was not smaller than that of the metal/SiO_2, indicating that the vacuum work function dominated the band alignment even in the metal/HfSiON. This result contradicts that of previous reports, in which the MIGS critically affected the band alignment in high-k gate materials. This means that the $V_{\rm fb}$ shift should also be influenced by the extrinsic factors.[25–28]

2.1.2. Electron state density in metal gates

Fermi-level pinning has been found to be largely determined by the distortion of the vacuum level of the metal gate, which is quantitatively governed by the electron state density in the metal gate.[18] The pinning factor is adjusted by considering the influence of the electron state density of the metal gate and can be expressed as

$$S = \left[1 + \frac{e^2 N_{\rm B}}{\varepsilon_0 E_{\rm gh}} \left(\frac{d_{MK}}{k} + \sqrt{\frac{\varepsilon_0}{e^2 D}}\right)\right]^{-1}, \tag{4}$$

where e is the charge of an electron, ε_0 is the vacuum permittivity, $d_{\rm MK}$ is the thickness of the metal-gate/high-k interfacial layer, $E_{\rm gh}$ is the band gap of the high-k dielectric layer, k is the relative permittivity of the high-$k$dielectric, $N_{\rm B}$ is the density of state and D is the electron state density. The calculated relationship between the metal EWF on HfO_2 and the work function of the metal gate is nearly the same as that obtained from the experiments,[18] as presented in Fig. 3. It suggests that a metal with a large electron state density exhibits a high degree of Fermi-level pinning and this constitutes one of the criteria to select proper metal gate materials.[18]

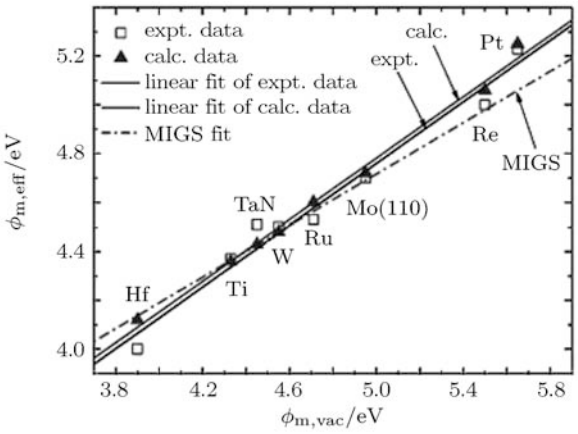


Fig. 3. Comparison among the MIGS fit, the calculation correlation considering the influence of the electron state density of the metal gate and the experimental trend of the metal EWF on HfO_2 for different metal gates.[18] The $\phi_{\rm m,vac}$ is the vacuum metal work function.

2.1.3. Positively charged oxygen vacancies in dielectrics

The Fermi-level pinning governed by the MIGS and the electron state density in a metal gate mainly determines the $V_{\rm fb}$ shift in metal-gate/high-k pMOS stacks. However, when the IL SiO_2 between the high-k dielectric and the Si substrate is introduced to improve the overall electrical properties of the metal/high-k MOS stacks (as shown in Fig. (4)), the above theory hardly explains the sharp roll-off of $V_{\rm fb}$, which critically depends on the thickness of the IL SiO_2 as well as the high temperature.[27] Recent experimental results show that annealing the metal electrodes at high temperature causes $E_{\rm F}$ to drift towards the mid gap. Metals with high work functions, such as Pt, Re and Ru, are unstable under oxygen-deficient conditions when they contact the high-k layer and are transparent to oxygen during post-annealing at high temperature.[28] It suggests that the $V_{\rm fb}$ shift, especially the $V_{\rm fb}$ roll-off, may be related to the oxygen vacancies created during the post-annealing at high temperature.[29]

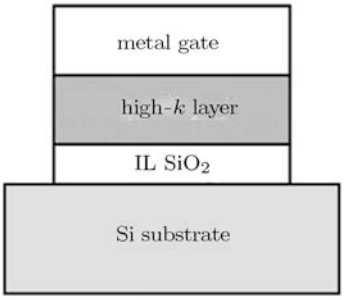


Fig. 4. MOS stack with an IL SiO_2 between the high-k dielectric and the Si substrate.

2.1.4. Oxygen vacancies in a high-k layer

It is well known that HfO_2 contains a much higher content of oxygen vacancies than SiO_2. This is because HfO_2 is an ionic crystal, which makes the property of the oxygen vacancy in HfO_2 different from that in SiO_2. The $V_{\rm fb}$ shift induced by oxygen vacancies in Hf-based high-k gate stacks has been verified by Shiraishi *et al.*[29,30] If an oxygen vacancy is formed in HfO_2 by removing an O atom from the crystal, two surplus electrons are generated. The electrons are transferred into the gate electrode and positive oxygen vacancies will be generated in the high-k layer.[30] Related research was also done by Robertson *et al.* and it was found that the Fermi-level is just below the Si valence band, thus, band bending due to the vacancy concentration shifts $V_{\rm fb}$ to the negative direction.[17]

Song *et al.* have presented a possible mechanism for the $V_{\rm fb}$ roll-off phenomenon based on the progressive oxygen vacancy generation in the high-k layer as the scaling down of the IL SiO_2.[10] When the metal gate with a high work function contacts the high-k layer, oxygen is transferred to the metal gate from the high-k layer, leaving $V_{\rm o}^{+}$ in the high-k layer. In order to compensate the $V_{\rm o}^{+}$, O from the bottom portion flows up to minimize $V_{\rm o}^{+}$ in the high-k layer. When the thickness of the IL SiO_2 becomes thinner, less O transports to compensate $V_{\rm o}^{+}$ and $V_{\rm fb}$ roll-off occurs, as shown in Fig. 5.[10] Choi *et al.* have observed the $V_{\rm fb}$ roll-off phenomenon in capacitors fabricated on terraced IL SiO_2 with Al_2O_3 dielectric films. It was found the the $V_{\rm fb}$ roll-off phenomenon is also influenced by the thickness of the IL SiO_2.[32,33]

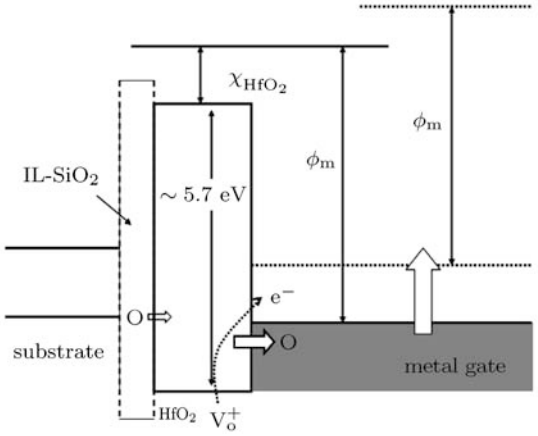


Fig. 5. Mechanism of $V_{\rm fb}$ roll-off in metal gate/high-k/IL-SiO_2/Si MOS stacks.[10]

2.1.5. Oxygen vacancy in interlayer SiO_2

Attention has been paid to the $V_{\rm fb}$ roll-off on the bottom IL SiO_2.[34] The $V_{\rm fb}$ roll-off phenomenon was proposed to be explained as a result of the enhanced positively charged oxygen vacancies in the IL SiO_2 layer when the thickness was below a certain critical value.[35] Oxygen vacancies are formed in the IL SiO_2 due to the interaction with the overlaying high-k film.[36] They are significantly enhanced when O atoms are consumed in the highly strained transitional SiO_2 region adjacent to the Si substrate.[37] Since the vacancy distribution through the thickness of SiO_2 is O diffusion is limited, the enhancement in the generated vacancy can be observed only when the thickness of SiO_2 becomes comparable with the characteristic O diffusion depth under the given processing conditions. Finally, the density gradient of the oxygen vacancies in SiO_2 is affected by the processing temperature, the

SiO_2 thickness and the high-k film composition. Thus, the V_{fb} roll-off occurs with a sharp rise in the oxygen vacancy density on the same scale of the IL SiO_2.[11]

2.2. Dipoles at the bottom interfacial layer

The oxygen related dipole formed at high temperature is a possible origin of the V_{fb} roll-off. Choi *et al.* have analyzed the possible causes for the V_{fb} roll-off. If the positive charge, such as oxygen vacancies, diffuses from the thin bottom IL SiO_2 into the high-k layer, it is difficult to explain the nonlinear EOT–V_{fb} curves. If the positive charge is created at the Si/SiO_2 interface, the magnitude of the V_{fb} roll-off should be a function of the EOT of the entire dielectric stack, as shown in Eq. (1). It is not applicable in this case, since the amount of V_{fb} roll-off is independent of the thickness of the high-k layer. If the positive charge is in the bulk SiO_2, when the IL SiO_2 becomes ultrathin, the positive bulk charge in the IL SiO_2 can be treated as a sheet charge. Consequently, the same problem is encountered for the SiO_2/Si interfacial layer.[33] Interface dipoles have been suggested to be responsible for the V_{fb} shift, especially for the V_{fb} roll-off, and the influence of the dipole on V_{fb} does not depend on the EOT.[9]

2.2.1. Dipole at high-k/IL-SiO_2 interface

Recent studies show that the dipole at a high-k/SiO_2 interface may play an important role in the V_{fb} shift.[38–41] By using bilayer high-k dielectric structures whose top and bottom high-k layers were HfO_2 and Al_2O_3 with different thicknesses, Iwamoto *et al.* found that when the top high-k layer thickness was varied and the bottom high-k layer was fixed, the V_{fb} shift was not observed. When the top high-k layer was fixed and the bottom high-k layer was varied, the V_{fb} shift was obvious, as shown in Fig. 6[40] and providing the evidences that the V_{fb} shift is closely linked to the high-k/SiO_2 interface.[40] Several proposals were provided to discuss the influencing factors between the high-k and the IL SiO_2 layers. A model to explain the physical origin of the dipole formed at the high-k/SiO_2 interface was proposed by Kita *et al.*[38] As a result of the areal density difference of the oxygen atoms at the high-k/SiO_2 interface, the oxygen movement from a

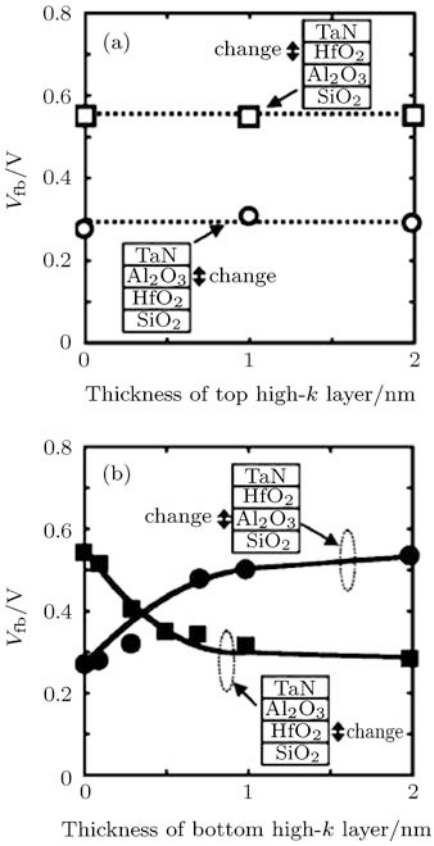


Fig. 6. (a) The V_{fb} of TaN-gate p-MOS capacitors with bilayer high-k dielectrics as a function of the thickness of the top high-k layer. (b) The V_{fb} as a function of the bottom high-k layer thickness. The V_{fb} shifts are evidently observed only when the bottom high-k layer thickness is varied.[40]

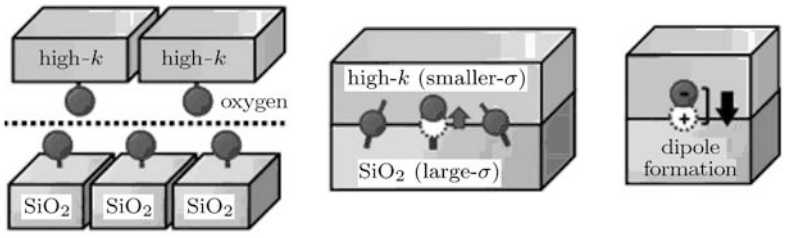


Fig. 7. Schematics to explain dipole formation at a high-k/SiO_2 interface based on the difference of the areal density of oxygen atoms (σ) for the case that high-k oxides have a smaller σ than SiO_2.[38]

higher-oxygen-density side to a lower-oxygen-density one determines the direction of the interface dipole. As shown in Fig. 7, when the interface is formed, the positions of the oxygen atoms are modified to relax the structure. The oxygen atom in SiO_2 moves toward the high-k side due to the density difference. The oxygen transfer creates the positively charged oxygen vacancy in the SiO_2 side and the negatively charged centre in the high-k side. Thus, the dipole at the high-k/IL-SiO_2 interface is formed, which induces the shift of V_{fb}.

In our previous work, we found that the dielectric contact induced gap states (DCIGS) at the high-k/SiO_2 interface could also be an important factor to induce the V_{fb} shift in metal/high-k MOS stacks.[41] In Fig. 8, ϕ_0 is the lowest energy level of the DCIGS, Q_{ss} is the DCIGS charge, Q_{sc} represents the space charge and E_F is the Fermi level of the high-k and SiO_2. When the DCIGS on the SiO_2 side are assumed to play the dominant role in the energy band bending of the high-k/SiO_2 system, electrons will flow from the high-k layer to SiO_2. A dipole will be formed as negative charge builds up on the SiO_2 side and an equal amount of positive charge builds up on the high-k side, as shown in Fig. 8(b). When the DCIGS on the high-k side are assumed to play the dominant role, the dipole will be in the opposite direction, as shown in Figs. 8(c) and 8(d).[41] In the pMOS, the density of the DCIGS on the high-k side is usually higher than that on the SiO_2 side, so the direction of the interfacial dipole points to the SiO_2 layer, which induces the negative shift of V_{fb}.

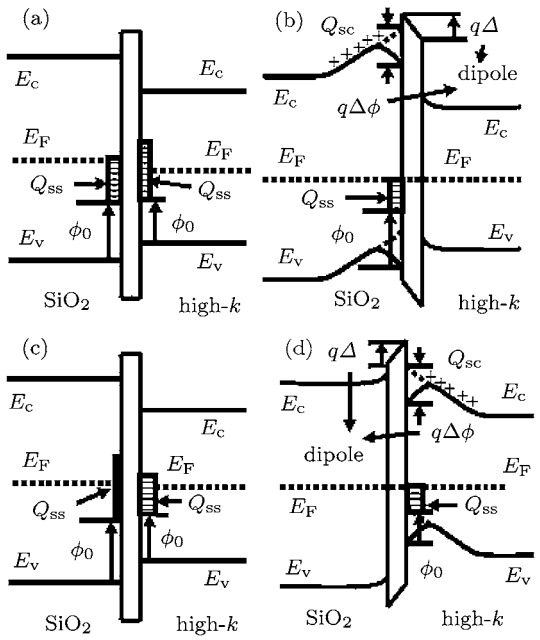


Fig. 8. Detailed energy band diagrams of high-k/SiO_2 systems based on the DCIGS model. (a) The DCIGS on the SiO_2 side is assumed to play the dominant role before contact, (b) band diagram at thermal equilibrium after contact. (c) The DCIGS on the high-k side is assumed to play the dominant role before contact, and (d) band diagram at thermal equilibrium after contact.[41]

2.2.2. Dipole at the IL SiO_2/Si interface

The crosssectional TEM images of the W/HfO_2 (6 nm)/SiO_2 stacks without and with the post Si-deposition annealing (PSA) at 1000 °C in N_2 for 100 s are shown in Fig. 9. It is obvious that the IL SiO_2 thickness increases after the PSA treatment. The V_{fb} roll-off behaviour in the thinner EOT region may be associated with the charge or the dipole in the bottom reaction layer induced by the re-oxidation at the IL-SiO_2/Si interface.[42] Hence, the dipole at the IL-SiO_2/Si interfacial layer may be responsible for the V_{fb} roll-off phenomenon.

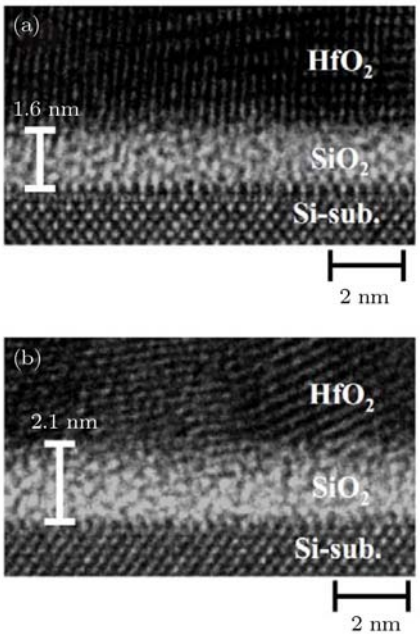


Fig. 9. Crosssectional TEM images of W/HfO_2 (6 nm)/SiO_2 stacks (a) without and (b) with PSA treatment at 1000 °C in N_2 for 100 s.[42]

A model describing the role of the dipoles at the SiO_2/Si interface on the V_{fb} sharp roll-off has been proposed.[43] An excess amount of dissociative O diffuses into the IL SiO_2 during the process, forming O=Si dipoles at the ultrathin IL-SiO_2/Si interface[44] and consequently playing an important role in the V_{fb} sharp roll-off. When the thickness of the IL SiO_2 is larger than the O diffusion depth, there is not enough dissociative O to form the interfacial dipoles between

the IL SiO_2 and the Si substrate.[45,46] As the thickness of the IL SiO_2 diminishes to below the diffusion depth, Si=O dipoles form more easily and they impose a negative sheet charge on the SiO_2 side and a positive sheet charge on the Si substrate side, as illustrated in Fig. 10. The electric field induced by the dipoles is at the SiO_2/Si interface and the extra voltage induced by the electric field shifts V_{fb} negatively, as shown in Fig. 11.[43]

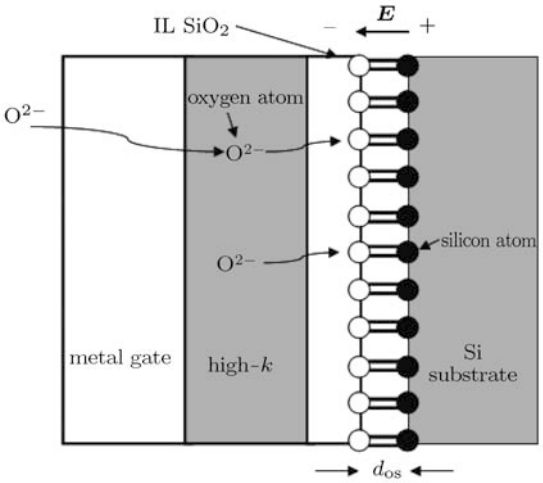


Fig. 10. The O diffuses into the IL SiO_2 from the high-k layer to form dipoles at the SiO_2/Si interface. The interface is similar to that of a parallel-plate capacitor.[43]

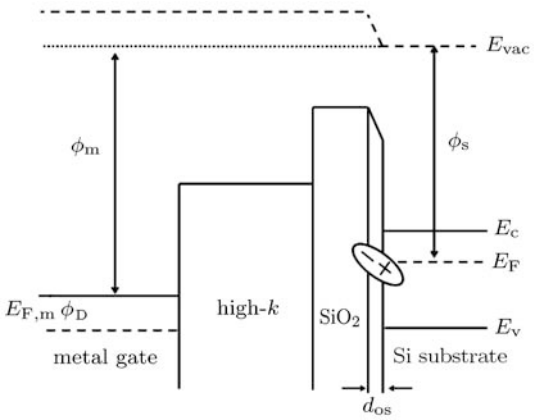


Fig. 11. The V_{fb} shifts negatively by modulating the difference of potential ϕ_D induced by dipoles at the SiO_2/Si interface, ϕ_m and ϕ_s denote the work functions of the metal gate and Si, respectively.[43]

3. Methods to reduce V_{fb} shift in pMOS

On account of the demand for energy conservation in modern electron devices, a small V_{th} is imperative for the MOS technology. Modulating the EWF of the metal gate and alleviating the V_{fb} roll-off phenomenon are effective for achieving a small V_{fb} shift, consequently shrinking the pMOSFETs. In this section, we summarize the methods used for this purpose.

3.1. EWF modulation in pMOS

Despite the advantages of direct metal gates, it is difficult to attain a proper metal couple having dual work functions in MOS devices, especially metal gates with a high enough EWF for the pMOS.[15] It has recently been found that inserting an Al-based capping layer or using Al doping alloy metal gate stacks can effectively modulate the EWF towards the p-type band edge on high-k dielectrics. The underlying mechanism of the EWF modulation in the pMOS by the incorporation of Al is discussed in this section.

3.1.1. Al-based capping layer

Introducing AlO_x or AlN capping layers to the high-k dielectrics has been proposed as an effective method to modulate the EWF towards the p-type band edge. The EWF (~ 5.1 eV) has been achieved on Hf-based high-k materials using an AlN_x interfacial layer and TiSiN electrodes in the pMOS by Alshareef *et al.*[47] As shown in Fig. 12, the gate stack with an AlN_x capping layer between the TiSiN gate and the Hf-based high-k layer can elevate the EWF by more than 260 meV and effectively reduces the magnitude of the V_{fb} shift to the negative direction.[47]

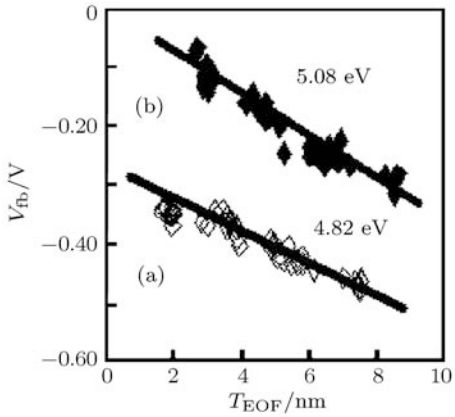


Fig. 12. Effect of an AlN_x interfacial layer on the TiSiN electrode work function. The V_{fb}–T_{EOT} plots are shown for TiSiN/$HfSiO_x$ and TiSiN/AlN_x/$HfSiO_x$ gate stacks.[47]

3.1.2. Al-doped alloy gate stack

Although inserting an Al-based capping layer can reduce the magnitude of the V_{fb} shift, it will increase the EOT because of the relatively low k value. To take advantage of the EWF without the EOT increment, attention has focused on incorporating Al into

the gate electrode or the high-k layer.[48] As shown in Fig. 13, compared to TaN and MoN gates, the EWF is elevated by more than 220 meV and a positive $V_{\rm fb}$ shift of $\sim$200 mV is observed in the pMOS with Al-doped gate stacks.[48]

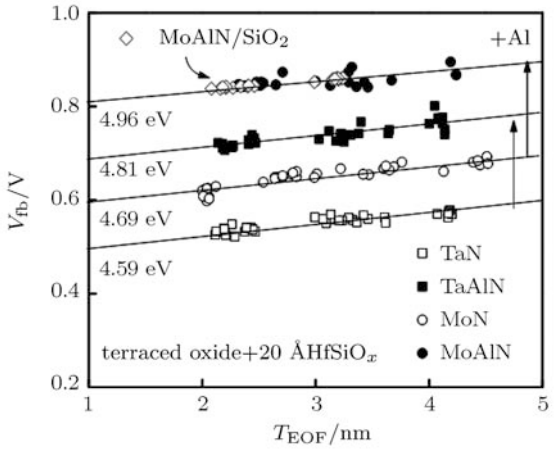


Fig. 13. The $V_{\rm fb}$–$T_{\rm EOT}$ plots and the EWF values for terraced oxide capacitors using electrodes with and without Al doping.[48]

The Al doping of the high-k layer can also significantly shift the band alignment between the metal gate and the high-k dielectric layer, consequently alleviating the $V_{\rm fb}$ shift in the pMOS. Experimental results have shown that with increasing Al contents, the valence band alignment can be achieved by the difference in the valence band maximum between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the H-terminated Si, as shown in Fig. 14.[49] Sharia *et al.* showed that the oxygen vacancies are stabilized in the vicinity of the substitutional Al in the IL SiO_2 when Al diffuses down from the high-k layer. The Al interstitial atoms pair up and form a stable Al–vacancy dipole in the vicinity of the HfO_2/SiO_2 interface, which plays an important role in the elevation of the EWF in the pMOS.[50]

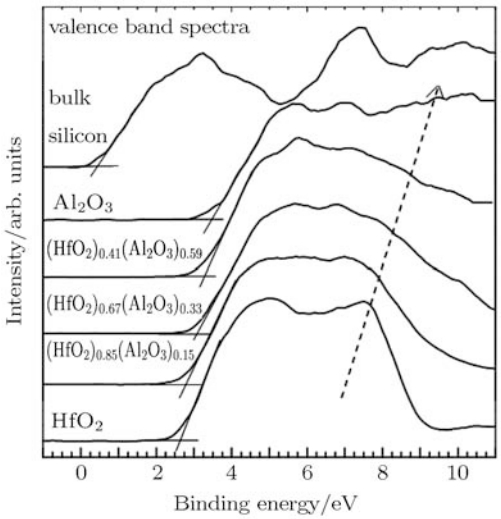


Fig. 14. X-ray photoelectron spectra of the valence band taken from various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples and H-terminated bulk Si. The dashed arrow indicates the gradual change of the valence band state density of the Hf aluminate.[49]

3.1.3. EWF modulation mechanism by Al incorporation

The EWF increment is attributed to the formation of the dipole at the high-k/SiO_2 interface as a result of the incorporation of Al ions.[47,48] The interfaced dipole and its role in the modulation of the EWF have been quantitatively evaluated by using electrochemical potential equalization and electrostatic potential methods, respectively.[51] The results show that the interface dipole causes an electrostatic potential difference across the metal/high-k interface, which significantly shifts the band alignment between the metal and the high-k layer, consequently modulating the EWF (Fig. 15). The modulation of the EWF (denoted as $\Delta_{\rm EWF}$) can be calculated by

$$\Delta_{\rm EWF} = e^2 N_{\rm B} d_{HS}(\chi_S - \phi_H + E_{\rm g}/2)/4k\varepsilon_0 E_{\rm g}, \quad (5)$$

where $d_{\rm HS}$ is the thickness of the high-k/SiO_2 interfacial layer, $E_{\rm g}$ is the band gap of the Si substrate and χ_S is the electron affinity of Si. The results calculated using Eq. (5) are compared to the experimental data from various metal gate electrode systems with a 1 nm Al-based capping layer, as shown in Table 1. Good agreement between the calculated results and the experimental data is obtained, suggesting that the dipole at the high-k/SiO_2 interfacial layer plays an important role in the modulation of the EWF.[51]

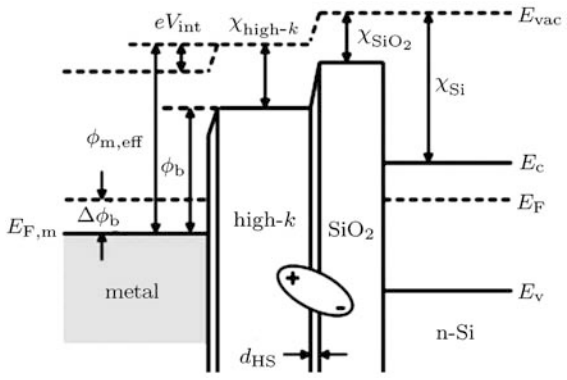


Fig. 15. Schematic of the metal-oxide-semiconductor band alignment modulated by the dipole related with Al at the high-k/SiO_2 interface.[51] The χ is the electron affinity.

Table 1. Modulation of EWF calculated using Eq. (5) ($\Delta_{\rm EWF,c}$) in comparison with that from experimental data ($\Delta_{\rm EWF,e}$).[51]

Metal	Capping layer (1 nm)	High-k dielectric	k	$\Delta_{\rm EWF,e}$ /meV	$\Delta_{\rm EWF,c}$/meV
			Expt.	Expt.	Calc.
TiSiN	AlN_x	$HfSiO_x$	11	260	260
TiSiN	AlO_x	$HfSiO_x$	11	240	260
TiN	AlO_x	$HfSiO_x$	11	280	260
TiSiN	Al_2O_3	$HfAlO_x$	10	300	287
TaCN	Al_2O_3	$HfAlO_x$	10	300	287
TiN	Al_2O_3	$HfAlO_x$	10	300	287

3.2. Methods to alleviate $V_{\rm fb}$ roll-off

The $V_{\rm fb}$ roll-off phenomenon is experimentally demonstrated to be closely related to oxygen diffusion, high temperature processing and positively charged defects in the pMOS. Many methods have been proposed to alleviate $V_{\rm fb}$ roll-off.

An effective method is to introduce a remote reactive sink layer to the metal-gate/high-k/beveled-SiO_2/Si MOS stack. For example, a 5 nm Ta remote reactive sink layer on the W/HfO_2 (3 nm)/beveled-SiO_2/Si MOS stacks reported by Akiyama *et al.* is shown in Fig. 16. The $V_{\rm fb}$ roll-off is not observed when the thickness of W is kept at $\sim$10 nm. This may be because Ta can easily absorb O from the gate stack and thus reduces the oxygen related defects and dipoles, consequently alleviating the $V_{\rm fb}$ roll-off.[34] The second method is to insert a top SiO_2 layer between the metal gate and the high-k dielectrics.[52] No $V_{\rm fb}$ roll-off is observed with 1 nm or 2 nm thick top SiO_2, however the $V_{\rm fb}$ roll-off is enhanced when the top-SiO_2 thickness is increased from 3 nm to 5 nm, as shown in Fig. 17.[52] The relative mechanism is as follows. As an opposite dipole layer, the thickness of the top layer SiO_2 is smaller than the oxygen diffusion depth.[43] The third method is to incorporate elements that can suppress the defects in the oxide layer. It has been reported that F^+ doping in the IL SiO_2 can reduce the magnitude of the $V_{\rm fb}$ roll-off by more than 200 mV through the passivation of the positively charged defects and the additional negative charge associated with the F atoms (Fig. 18).[11,13,14] Low temperature ($<$ 500 °C) oxygen incorporation is another effective method to alleviate $V_{\rm fb}$ roll-off. It was proposed that oxygen vacancies in the high-k layer and in the IL SiO_2 can be reduced by the suppression of the reaction at the IL-SiO_2/Si interfacial layer at a low processing temperature.[10,53]

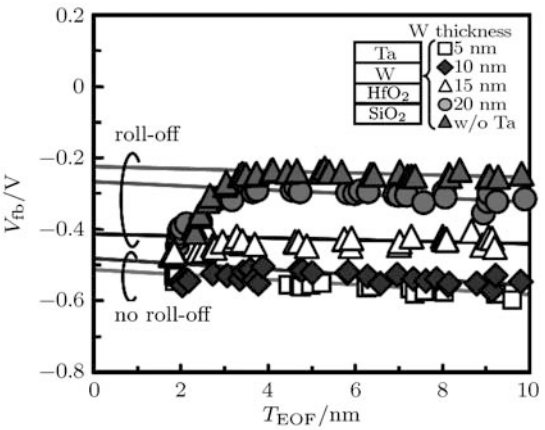


Fig. 16. Suppression of $V_{\rm fb}$ roll-off behaviour in a W/HfO_2(3 nm)/beveled-SiO_2 stack using Ta films on W. The $V_{\rm fb}$ roll-off behaviour disappears with decreasing W thickness.[34]

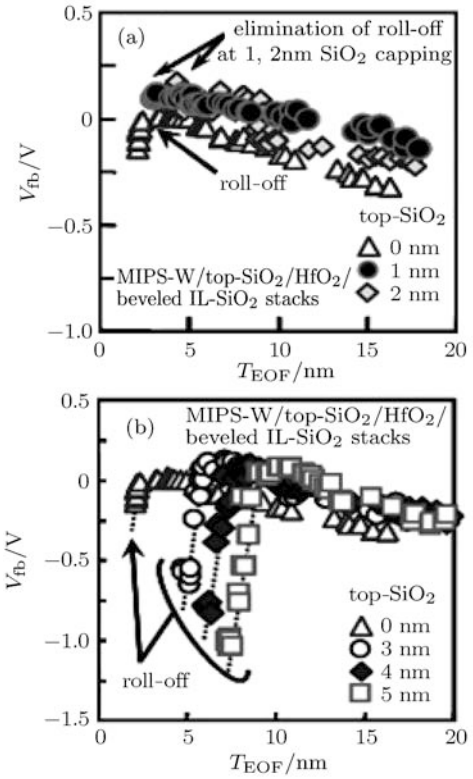


Fig. 17. The $V_{\rm fb}$–$T_{\rm EOT}$ relationship in 3 nm HfO_2/beveled IL-SiO_2/Si MOS with various top-SiO_2 layers between W and HfO_2: (a) 1 nm-thick and 2 nm-thick top-SiO_2, and (b) 3 nm-thick to 5 nm-thick top-SiO_2.[52]

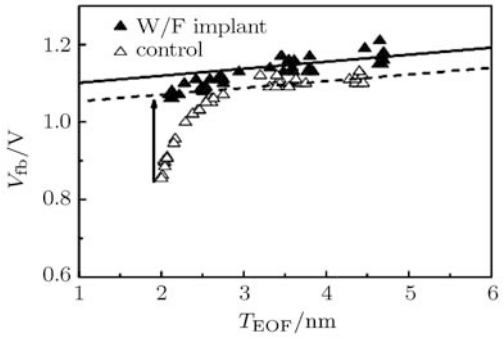


Fig. 18. The V_{fb} roll-off phenomenon is suppressed by F incorporation into the IL SiO_2 layer.[14]

4. Conclusion

In this paper, recent progress in the study of V_{fb} shift and roll-off in the pMOS is reviewed. The underlying mechanism dictating the V_{fb} shift in the pMOS and the V_{fb} roll-off phenomenon are discussed. Moreover, methods to modulate the EWF of the metal gate and to alleviate the V_{fb} roll-off phenomenon are described.

In order to further improve the performance of the pMOS in sub-45 nm devices, it is necessary to explore substitute gate materials with high EWF and substrates with high mobility.[54,55] Recent preparation of FETs based on graphene (GFET) with high conductivity and other C-based material[56] have suggested an alternative technology for sub-10 nm MOSFETs. However, there are still tremendous challenges ahead concerning the design of novel MOSFET structures suitable for the next generation of nano-electronic devices.

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