The effect of a HfO_2 insulator on the improvement of breakdown voltage in field-plated GaN-based HEMT*

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A $GaN/Al_{0.3}Ga_{0.7}N/AlN/GaN$ high-electron mobility transistor utilizing a field plate (with a 0.3 μm overhang towards the drain and a 0.2 μm overhang towards the source) over a 165-nm sputtered HfO_2 insulator (HfO_2-FP-HEMT) is fabricated on a sapphire substrate. Compared with the conventional field-plated HEMT, which has the same geometric structure but uses a 60-nm SiN insulator beneath the field plate (SiN-FP-HEMT), the HfO_2-FP-HEMT exhibits a significant improvement of the breakdown voltage (up to 181 V) as well as a record field-plate efficiency (up to 276 V/μm). This is because the HfO_2 insulator can further improve the modulation of the field plate on the electric field distribution in the device channel, which is proved by the numerical simulation results. Based on the simulation results, a novel approach named the proportional design is proposed to predict the optimal dielectric thickness beneath the field plate. It can simplify the field-plated HEMT design significantly.

Keywords: HfO_2 insulator, HfO_2-FP-HEMT, FP efficiency, proportional design

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1. Introduction

GaN-based high-electron mobility transistors (HEMTs) have widely been used in high-power, high-temperature, and high-frequency applications[1,2] since their first demonstration by Asif *et al.*[3] in 1993 due to their superior material properties. With great improvements and breakthroughs in material growth, device design, and processing technologies, microwave power densities of the GaN HEMTs have been demonstrated to be at least ten times greater than those of the GaAs-based devices. In order to further improve the device power performance, we need to increase the device off-state breakdown voltage and simultaneously eliminate the radio frequency dispersion.[4] For this purpose, numerous technologies have been developed, among which the field-plate (FP) techniques are most effective with their origins in the context of high-voltage p–n junctions.[5] So far, various FP technologies have been proposed and developed, including gate-connected FPs,[6,7] gate-and-drain-connected dual-FPs,[8] source-connected FPs,[9] gate-connected multiple-FPs,[10] source-and-drain-connected dual-FPs,[11] gate-and-source-connected dual-FPs,[12,13] and slant FPs.[14,15] However, in the conventional field-plated HEMTs, the insulators used beneath the FP are usually SiO_2 or Si_3N_4 rather than the high permittivity (high k) dielectrics. As a matter of fact, it is of great importance to make some attempts in this interesting domain, in which the high k dielectrics are introduced into the field-plated devices to improve the device breakdown performance. Amazing results may be obtained.

In this paper, the fabrication and breakdown characteristics of the $GaN/Al_{0.3}Ga_{0.7}N/AlN/GaN$ HEMT on a sapphire substrate utilizing an FP (with a 0.3 μm overhang towards the drain and a 0.2 μm overhang towards the source) over a 165-nm sputtered HfO_2 insulator (HfO_2-FP-HEMT) are demonstrated. The HfO_2, having a high permittivity (20–25) and

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being highly insulating with a large band gap (5.6–5.8 eV), has recently been studied extensively as the passivation film and/or the gate dielectric in GaN-based HEMTs.[16,17] With the adoption of the HfO_2 insulator under the FP, the off-state three-terminal breakdown voltage and the FP efficiency of the HfO_2-FP-HEMT are improved significantly compared with those of the conventional field-plated HEMT with the same structure using an optimized 60 nm SiN insulator (SiN-FP-HEMT). The simulations of mechanism, in which the HfO_2 insulator beneath the FP is conducible to better modulation of the device channel electric field, are investigated by using the Silvaco ATLAS. In addition, a simple and effective approach is proposed for the determination of the structure of the FP when different insulators are used. It is of great practical importance for the high power field-plated HEMT design.

2. Device fabrication

The device epilayer heterostructure used here was grown on the *c*-plane sapphire substrate by using metal–organic chemical vapour deposition (MOCVD). Two wafers were prepared at the same time with the same MOCVD process. The epilayer heterostructure was composed of a 1.4-μm undoped GaN buffer layer, a 1.5-nm AlN interlayer, a 23-nm undoped $Al_{0.3}Ga_{0.7}N$ barrier layer, and a 2-nm undoped GaN cap layer. A carrier density of 1.2×10^{13} cm^{-2} and a mobility of 1418 $cm^2\cdot V^{-1}\cdot s^{-1}$ were obtained from the Hall measurement at room temperature.

Figure 1 shows the cross section of the HfO_2-FP-HEMT. The device fabrication started with mesa isolation using the Cl_2 plasma in a reactive ion etch (RIE) system. Then, Ti/Al/Ni/Au metals were evaporated and alloyed using rapid thermal annealing at 870 °C for 40 s in N_2 ambient to form ohmic contacts. Next, 0.6 μm gates with Ni/Au/Ni were fabricated by using ultraviolet (UV) lithography followed by e-beam evaporation. Then the surfaces of the devices were passivated by a 165-nm HfO_2 insulator deposited by the magnetron sputtering at 200 °C using an elemental Hf target sputtered in O_2 atmosphere. The opening of the contact windows in the passivation layers was achieved by using CF_4 and Ar plasma in an RIE system. Subsequent to that, the FP, being 1.1 μm long and having a 0.3 μm overhang towards the drain and a 0.2 μm overhang towards the source, was deposited on top of the HfO_2 layer. The gate and the FP were connected in the gate-pad region. Finally, a 180-nm SiN layer was deposited using plasma-enhanced chemical vapour deposition (PEVCD) for the purpose of device protection, and the HfO_2-FP-HEMT was finished on one wafer. At the same time, the devices with the HfO_2 insulator passivation but without the FP (HfO_2-HEMT) were also fabricated on the same wafer. The gate width was 100 μm. The source–drain and the gate–drain spacings were 5 μm and 3.5 μm, respectively. For comparison, both the conventional SiN passivated HEMT without the FP (SiN-HEMT) and the SiN-FP-HEMT with the FP over a 60-nm PECVD deposited SiN layer, which had the same dimensions as the HfO_2-FP-HEMT, were also fabricated on the second wafer. Based on our earlier work, the thickness of SiN beneath the FP in the SiN-FP-HEMT was chosen to be 60 nm, an optimized thickness determined by experiments, with which the highest breakdown voltages can be achieved.

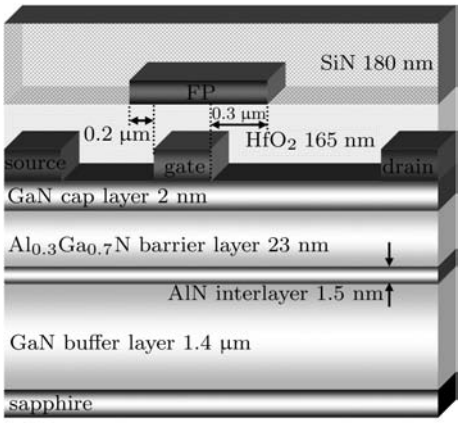


Fig. 1. Cross section of the HfO_2-FP-HEMT.

3. Device performance and discussion

In order to ensure the good quality of the HfO_2 insulator, X-ray photoelectron spectroscopy (XPS), a quantitative spectroscopic technique, was used to measure the elemental composition of the HfO_2 insulator deposited. Figure 2 shows the Hf 4f and the O 1s core level XPS spectra of the as-deposited HfO_2 measured in an XPS system with a monochromatic Al Kα source (1486.6 eV). The XPS spectra shown in the figure have been shifted based on the adventitious carbon peak. It can be seen in Fig. 2 that the measured binding energies of the Hf $4f_{7/2}$ (16.958 eV and 18.554 eV) and the O 1s (530.13 eV) peaks are in good agreement with the reference values (16.7 eV for Hf $4f_{7/2}$ peak and 530.4 eV for O 1s peak).[18]

This demonstrates that the Hf element is fully oxidized to the Hf^{4+} state. Furthermore, the O:Hf atomic ratio obtained from the quantitative XPS calculation is 2.19, which again clearly demonstrates a good film stoichiometry.

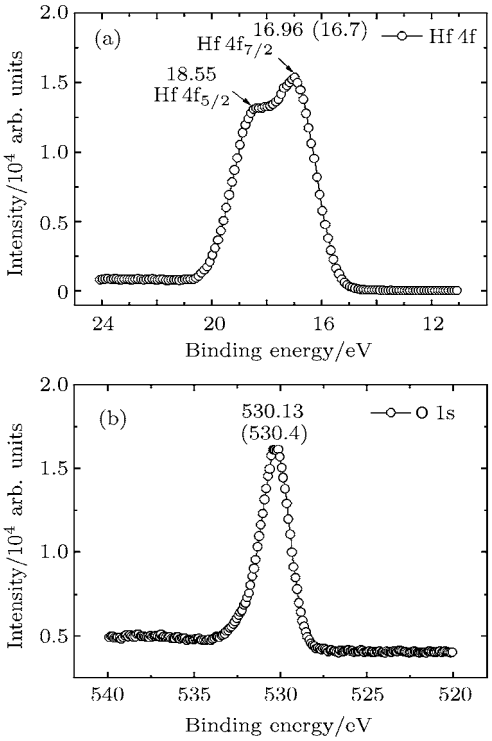


Fig. 2. Core level XPS spectra of the as-deposited HfO_2 for Hf 4f (a) and O 1s (b).

Figure 3 shows the comparisons of the transfer and the transconductance characteristics between the HfO_2-FP-HEMT and the SiN-FP-HEMT at the drain bias $V_{DS} = 10$ V. It can be seen that both the maximum current density (I_{DS}) and the peak transconductance (Gm) of the HfO_2-FP-HEMT are slightly smaller than those of the SiN-FP-HEMT. This is probably due to the effect of the etch damage introduced during the etch process of the HfO_2insulator with the Ar plasma and could be avoided by properly optimizing the etch process.

The off-state three-terminal drain–source breakdown voltage ($V_{DS,B}$) was measured at gate bias $V_{GS} = -8$ V below the pinch-off voltage using an Agilent 4156B semiconductor parameter analyzer. The breakdown voltages of the HfO_2-FP-HEMT, the HfO_2-HEMT, the SiN-FP-HEMT, and the SiN-HEMT are shown in Fig. 4. In this paper, the breakdown voltage is defined as the drain voltage when the drain current density is 0.1 mA/mm, which is consistent with the rapidly increasing current in the avalanche breakdown. The breakdown voltage of the HfO_2-FP-HEMT was measured to be 181 V, while that of the conventional SiN-FP-HEMT was only 146 V. The FP efficiency,[19] defined as the ratio of the breakdown voltage increment to the 0.3 μm overhang length of the FP towards the drain (the effective part of the FP), is used to describe the ability of the FP to improve the breakdown voltage. Compared with the SiN-HEMT, the SiN-FP-HEMT has a breakdown voltage increment of 57 V, and the FP efficiency is calculated to be 190 V/μm, which is a value large enough for field-plated HEMTs with SiO_2 or SiN insulator. The breakdown voltage increment for the HfO_2-FP-HEMT (compared with the HfO_2-HEMT) is as large as 83 V, and the corresponding FP efficiency is up to 276 V/μm, the highest FP efficiency ever achieved for any field-plated GaN-based HEMT to the best of our knowledge. The significant and exciting improvements to the breakdown voltage and the FP efficiency in the HfO_2-FP-HEMT compared with that in the SiN-FP-HEMT are attributed to the adoption of the high k HfO_2 insulator beneath the FP, the mechanism of which will be investigated by the following numerical simulations.

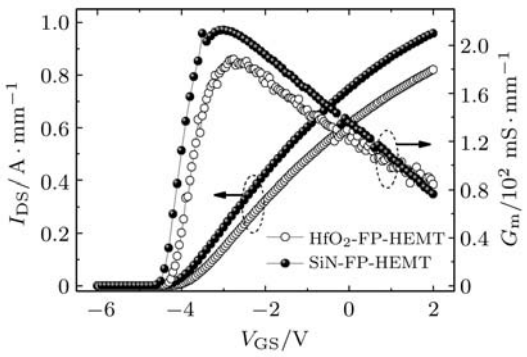


Fig. 3. Comparisons of transfer and transconductance characteristics between HfO_2-FP-HEMT and SiN-FP-HEMT.

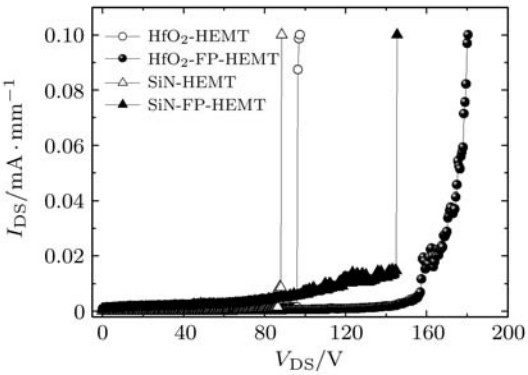


Fig. 4. Comparison of off-state breakdown voltage among HfO_2-FP-HEMT, HfO_2-HEMT, SiN-FP-HEMT, and SiN-HEMT.

4. Numerical simulations and analyses

In this paper, the two-dimensional physics-based device simulator Silvaco-ATLAS was used to get an insight into the characteristics observed for all the devices mentioned above. A background carrier concentration of 1×10^{15} cm^{-3} was used for all the materials, and the surface state at the interface between the passivation film and the semiconductor was neglected. The Shockley–Read–Hall recombination model and the Caughey and Thomas field-dependent mobility model were included in the simulations. The Van Overstraeten–de Man impact ionization model, described as $\alpha = \alpha_0 \, \mathrm{e}^{-E_\mathrm{c}/E}$, where α is the ionization coefficient and E is the electric field, was used to calculate the impact ionization rate with measured model coefficients $\alpha_0 = 2.9 \times 10^8$/cm and $E_\mathrm{c} = 3.4 \times 10^7$ V/cm.[20] The Schottky barrier tunneling and the thermionic emission were considered for the gate current. The polarization effect was modeled as a single positive sheet charge[21] of 1.22×10^{13} cm^{-2}, which was determined by making the simulated transfer characteristics consistent with the experimental results located along the heterojunction. The simulation and the experimental results for the transfer characteristics of the SiN-FP-HEMT are shown in Fig. 5. Usually, the experimental transfer characteristics under the direct current (DC) condition in the fabricated HEMTs could be affected by the self-heating effect, which could make the current lower than that expected. However, the self-heating effect was not taken into account in the simulations. In order to compare the experimental results with those simulated, the experimental transfer characteristic was obtained by using the double-pulse measurements to avoid the self-heating effect. The double-pulse measurements, with a pulse width of 500 ns and a pulse period of 0.1 ms, were carried out by pulsing both the drain–source and the gate–source voltages synchronously away from the baseline bias points ($V_\mathrm{GQ} = 0$ V, $V_\mathrm{DQ} = 0$ V) to the points (V_GS, V_DS), where the current was measured. As can be seen, the simulation results are in good agreement with the experimental ones, indicating the feasibility of our device model.

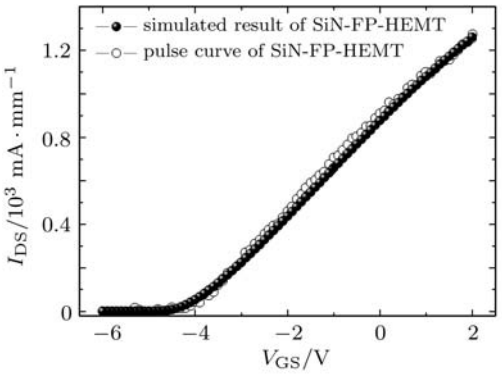


Fig. 5. Comparison of transfer characteristics between the simulations and the experiments for the SiN-FP-HEMT.

Figure 6(a) shows the simulated off-state breakdown characteristics of the HfO_2-FP-HEMT, the HfO_2-HEMT, the SiN-FP-HEMT, and the SiN-HEMT. The simulated off-state breakdown characteristics of the SiN-FP-HEMT with different thicknesses of SiN beneath the FP for the purpose of optimization are shown in Fig. 6(b). The gate bias V_GS is set to be –4.5 V, at which all devices are nearly pinched off. To the best of our knowledge, it is very difficult to compare the simulation results with the experimental ones by using the same definition for the breakdown voltage due to the absence and/or the inaccuracy of some GaN parameters used in the simulations. Thus, the breakdown voltage in the simulations is defined as the intersection between the extrapolated saturation segment and the impact ionization induced rapidly rising segment,[21] as shown in the inset of Fig. 6(a). The simulation results in this paper, as expected, show the trend of the experimental results. A similar method was used in other literature.[22] 130 nm, the SiN thickness beneath the FP for the SiN-FP-HEMT used in Fig. 6(a), is the optimal thickness according to the results shown in Fig. 6(b). The thickness of HfO_2 beneath the FP for the HfO_2-FP-HEMT used in Fig. 6(a) is calculated by (130 nm×165 nm)/60 nm = 358 nm, where 130 nm is the simulated optimal SiN thickness beneath the FP for the SiN-FP-HEMT, 165 nm the experimental HfO_2 thickness, and 60 nm the experimental optimal SiN thickness. It can be seen that the results in Fig. 6(a) are in good agreement with those in Fig. 4. The breakdown voltages of the HfO_2-FP-HEMT and the SiN-FP-HEMT are calculated to be 455 V and 310 V, respectively. The breakdown voltage increment for the HfO_2-FP-HEMT compared with the breakdown voltage for the HfO_2-HEMT is 265 V. Correspondingly, the increment in the breakdown voltage for the SiN-FP-HEMT compared with the breakdown voltage for

the SiN-HEMT is 190 V. The greater increment in the breakdown voltage achieved by means of the HfO_2 insulator demonstrates the effect of the HfO_2 insulator on the improvement of the breakdown voltage in the field-plated HEMTs. Furthermore, the ratio of the breakdown voltage increment for the HfO_2-FP-HEMT to that for the SiN-FP-HEMT obtained by the simulations is 1.39 (=265/190), which is very close to the 1.46 (=83/57) obtained in the experiment. Thus, we come to the conclusion that the simulation results are in accordance with the experimental ones.

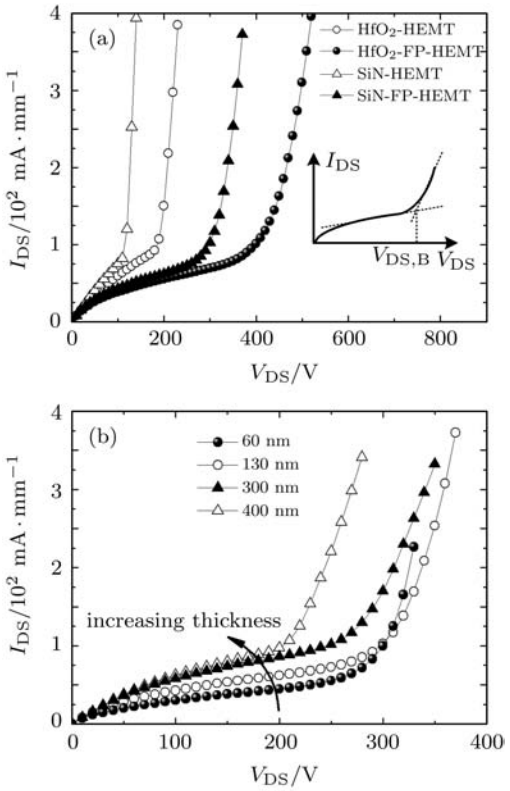


Fig. 6. (a) Simulated off-state breakdown characteristics of HfO_2-FP-HEMT, HfO_2-HEMT, SiN-FP-HEMT, and SiN-HEMT. (b) Simulated off-state breakdown characteristics of the SiN-FP-HEMT with different thicknesses of SiN beneath the FP for the purpose of optimization. The insert in (a) shows definition of breakdown voltage.

Figure 7 shows the simulated off-state electron concentration distributions in the AlGaN barrier layers for the SiN-FP-HEMT (a) and the HfO_2-FP-HEMT (b) at $V_{GS} = -4.5$ V and $V_{DS} = 310$ V. As can be seen, compared with the SiN-FP-HEMT, the HfO_2-FP-HEMT shows a significant depletion of electrons in the barrier layer between the gate and the drain, and the depletion region is further spread towards the drain due to the adoption of HfO_2 beneath the FP. This indicates a more uniform distribution of applied voltage V_{DS} along the device channel between the gate and the drain in the HfO_2-FP-HEMT. Thus, a more smooth distribution of electric field could be obtained in the HfO_2-FP-HEMT device channel. Figure 8 shows the total off-state electric field distributions in the device channels for the HfO_2-FP-HEMT (at $V_{DS} = 455$ V) and the SiN-FP-HEMT (at $V_{DS} = 310$ V). As can be seen, with the HfO_2 insulator beneath the FP, the ability of the FP in the HfO_2-FP-HEMT to uniform the total electric field (E) along the device channel in the gate–drain spacing is improved considerably.

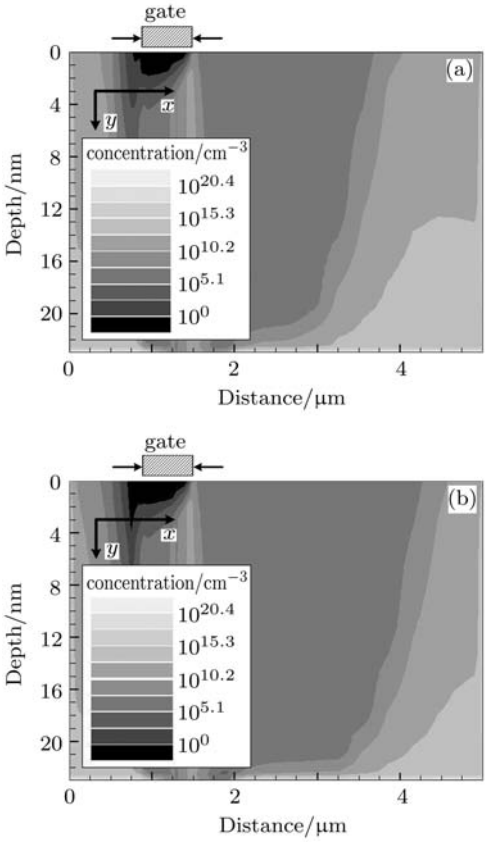


Fig. 7. Simulated off-state electron concentration distributions in the barrier layer for SiN-FP-HEMT (a) and HfO_2-FP-HEMT (b).

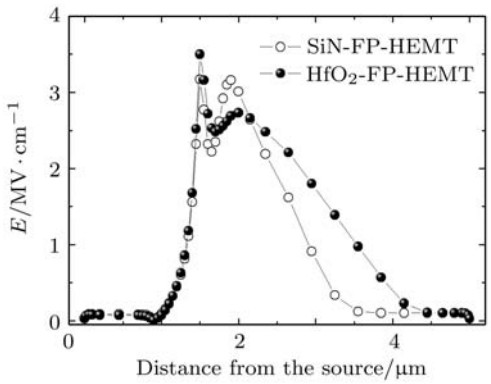


Fig. 8. Total off-state electric field distributions in the device channels for HfO_2-FP-HEMT at $V_{DS} = 455$ V and SiN-FP-HEMT at $V_{DS} = 310$ V.

A broader electric field distribution in the HfO_2-FP-HEMT channel is obtained compared with that in the SiN-FP-HEMT channel. Thus, the avalanche multiplication effect can be suppressed at high V_{DS} to a great extent, and pronounced improvement of the breakdown voltage can be achieved in the HfO_2-FP-HEMT.

A simple and useful design approach for the FP structure named the proportional design is proposed based on the simulations in this paper, with which we can easily predict the optimal dielectric thickness beneath the FP. This approach is described as $\varepsilon_1/d_1 = \varepsilon_2/d_2$, where $\varepsilon_1(\varepsilon_2)$ and $d_1(d_2)$ are the dielectric constant and the optimal dielectric thickness beneath the FP, respectively. Based on the proportional design relation of $\varepsilon_{SiN}/d_{SiN} = \varepsilon_{HfO_2}/d_{HfO_2}$, where $\varepsilon_{SiN} = 7.5$, $d_{SiN} = 130$ nm, and $\varepsilon_{HfO_2} = 20$, the predicted optimal HfO_2 thickness for the simulations is determined to be 347 nm. Figure 9 shows the simulated off-state breakdown characteristics of the HfO_2-FP-HEMT with different thicknesses of HfO_2 beneath the FP for the purpose of optimization. The optimized thickness of HfO_2 beneath the FP is determined to be 400 nm, with which a maximum breakdown voltage of 470 V for the HfO_2-FP-HEMT is achieved. The breakdown voltage for the HfO_2-FP-HEMT with the predicted optimal HfO_2 thickness of 347 nm is determined to be 440 V, which is only 30 V less than that with an optimized HfO_2 thickness of 400 nm. This indicates a good effectiveness of our proportional design approach in predicting the optimal dielectric thickness beneath the FP with only a slight deviation. The effectiveness of our proportional design approach can be further verified by similar simulations for the HEMT with an $HfSiO_4$ insulator beneath the FP ($HfSiO_4$-FP-HEMT). The predicted optimal $HfSiO_4$ thickness is 208 nm according to the proportional design relation of $\varepsilon_{SiN}/d_{SiN} = \varepsilon_{HfSiO_4}/d_{HfSiO_4}$, where $\varepsilon_{SiN} = 7.5$, $d_{SiN} = 130$ nm, and $\varepsilon_{HfSiO_4} = 12$. The simulation results (not shown) of the $HfSiO_4$-FP-HEMT show that the breakdown voltage of the device with 208 nm $HfSiO_4$ insulator is only 25 V less than the maximum breakdown voltage of the device with the simulated optimized $HfSiO_4$ thickness of 260 nm. In fact, the practical HfO_2 thickness of 165 nm for the fabricated HfO_2-FP-HEMT mentioned above is very close to the predicted optimal HfO_2 thickness of 160 nm calculated by the relation of $\varepsilon_{SiN}/d_{SiN} = \varepsilon_{HfO_2}/d_{HfO_2}$, where $\varepsilon_{SiN} = 7.5$, $d_{SiN} = 60$ nm, and $\varepsilon_{HfO_2} = 20$. This indicates that the breakdown voltage of 181 V for the fabricated HfO_2-FP-HEMT with 165 nm HfO_2 is approximately the maximum.

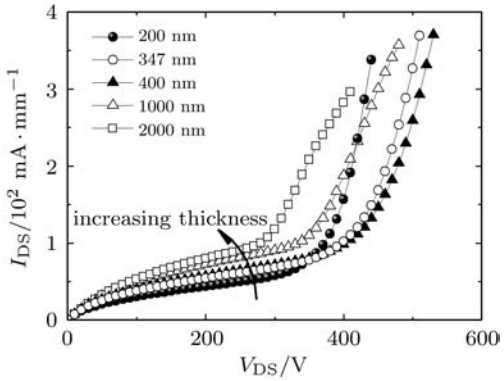


Fig. 9. Simulated off-state breakdown characteristics of HfO_2-FP-HEMT with different thicknesses of HfO_2 beneath the FP for the purpose of optimization.

5. Conclusion

The GaN/$Al_{0.3}Ga_{0.7}$N/AlN/GaN HfO_2-FP-HEMT utilizing an FP (a 0.3 μm overhang towards the drain and a 0.2 μm overhang towards the source) over a 165 nm sputtered HfO_2 insulator is fabricated, and its breakdown characteristics are investigated. The HfO_2-FP-HEMT exhibits a breakdown voltage as high as 181 V, leading to a record FP efficiency of up to 276 V/μm. The numerical simulations on the breakdown characteristics show that the FP with the HfO_2 insulator could further spread the distribution of the depletion region in the AlGaN barrier layer compared with the FP with the SiN insulator. It indicates a uniform distribution of the applied voltage along the device channel in the gate–drain spacing for the HfO_2-FP-HEMT compared with that for the SiN-FP-HEMT. Thus, significant improvements in the ability of the FP with the HfO_2 insulator to uniform the electric field along the 2DEG channel could be achieved, which results in a considerable increase in the breakdown voltage and the FP efficiency of the HfO_2-FP-HEMT. The excellent and exciting breakdown characteristics of the HfO_2-FP-HEMT in the simulations and the experiments demonstrate the great potential and superiority of the HfO_2 insulator for high-breakdown applications. Furthermore, a simple and effective proportional design approach for the FP structure is proposed, which could make it easy to predict the optimal dielectric thickness beneath the FP without a complex optimization procedure.

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