Top contact organic field effect transistors fabricated using a photolithographic process*

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This paper proposes an effective method of fabricating top contact organic field effect transistors by using a photolithographic process. The semiconductor layer is protected by a passivation layer. Through photolithographic and etching processes, parts of the passivation layer are etched off to form source/drain electrode patterns. Combined with conventional evaporation and lift-off techniques, organic field effect transistors with a top contact are fabricated successfully, whose properties are comparable to those prepared with the shadow mask method and one order of magnitude higher than the bottom contact devices fabricated by using a photolithographic process.

Keywords: organic field effect transistors, top contact, photolithographic

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1. Introduction

During the past few decades, organic field effect transistors (OFETs) have attracted extensive attention for such potential applications as flat panel displays, identification tags, and integrated circuits,[1−3] and tremendous progress has been achieved in both device performance and integrated techniques.[4,5] Nowadays, the performance of OFETs are comparable to those of amorphous silicon (a-Si:H) devices.[6] In addition, various types of organic integrated circuits have been demonstrated.[7−9] The OFETs with top contact (TC) geometry, excellent electrode/organic layer contact, and good device performance can be obtained; but in practical circuits, because of their compatibility with photolithographic techniques,[10−13] most of the devices have adopted a bottom contact (BC) configuration, which suffers from lower device performance due to the poor organic molecular ordering, larger contact resistance, and low charge injection efficiency.[14−16]

Recently, there some simple circuits have been fabricated by using the shadow method based on TC OFETs,[17,18] but integration complex circuits were almost impossible. Meanwhile, a lot of work has been done to improve the performance of BC OFETs, such as self-assembled monolayer modification,[19] incorporating an organic semiconductor layer between the electrodes and the active layer.[20] Additionally, Chu *et al.* adopted metal oxides as the buffer layers to enhance the hole injection into semiconductors.[21] With this interlayer, metals even with a lower work function, such as Al, can still be used as efficient source-drain (S/D) contacts. However, the performances of BC OFETs is still difficult to compare with TC ones. In addition, most of these methods are more efficient for TC OFETs,[22,23] so it is necessary to find some methods to fabricate TC OFETs that are compatible with large-scale integration.

In this paper, we propose a method to fabricate TC OFETs using photolithographic techniques. The copper phthalocyanine (CuPc) layer was protected with a passivation layer, through photolithographic and etching processes; parts of the passivation layer were etched off to form S/D electrodes patterns. Then, using conventional evaporation and lift-off techniques, TC OFETs were proposed. The mobility is 3.51×10^{-3} $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$, 1.36×10^{-3}, and 1.41×10^{-4} $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$, on/off ratio 2×10^4, 10^5, and 10^4 for TC OFETs prepared by the shadow method, and TC OFETs and BC OFETs were fabricated by using photolithographic process, respectively.

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2. Experimental details

Figures 1(a)–1(d) illustrate the fabrication process of TC OFETs. The devices were made on Si substrates, where highly doped Si and 300-nm thermal oxides SiO_2 served as the gate electrode and the insulator, respectively. The surface of the substrates was ultrasonically cleaned in acetone, alcohol and deionized water, and then modified by octadecyltrichlorosilane (OTS). The 50-nm thick CuPc films were then thermally evaporated at a deposition rate of 0.3 Å/s (1 Å = 0.1 nm) with a typical background pressure of 4×10^{-4} Pa, and the substrates were kept at 120 °C. Then 280-nm thick poly-4-vinylphenol (PVP) were spin coated onto CuPc films and the samples were cured on top of a hot plate at 180 °C for 10 min to remove propylene glycol monomethyl ether acetate from the PVP film. Subsequently, 2.3-μm thick photoresist was spun on the PVP surface and was patterned by a photolithographic process. The defined patterns were the areas for S/D electrodes. Using this resist layer as a mask, we etched off the PVP layer by reaction ion etching (RIE) to form the patterns. Finally, 50-nm gold with 10-nm Cr as the adhesion layer was deposited by a Johnsen e-beam evaporation system and then used in a lift-off process to form S/D electrodes. For comparison, ordinary BC OFETs fabricated by using a photolithographic process and TC OFETs with the shadow method were also proposed under the same conditions as described above. The defined channel lengths (L) and channel widths (W) were 500 μm and 45 μm, respectively. The electrical characteristics were measured in air at room temperature using a Keithley 4200 semiconductor characterization system. The morphologies of the CuPc surface were observed by atomic force microscopy (AFM).

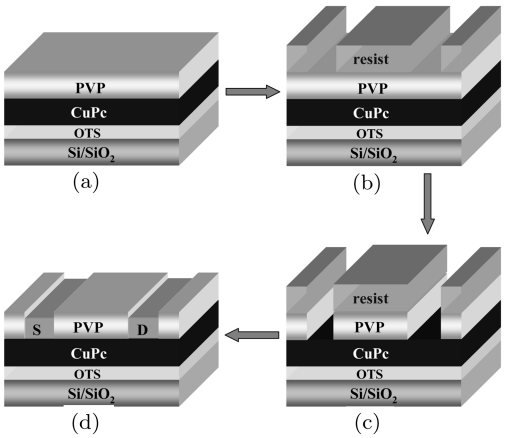


Fig. 1. Fabrication processes of a TC OFET by using a photolithographic and etching process. Panel (d) illustrates the final structure of thes device.

3. Results and discussion

Using photolithographic technique, two kinds of OFETs (TC and BC) were fabricated. Figures 2(a) and 2(b) show the transfer and output characteristics of the CuPc TC OFETs, respectively. These curves show typical p-type field effect transistor behaviours. The electric parameters were extracted from the saturation region using a classical method based on

$$I = \frac{\mu_{\rm FET} W C_0}{2L}(V_{\rm GS} - V_{\rm T})^2.$$

Here, $\mu_{\rm FET}$ is the field effect mobility, C_0 is the capacitance per unit area of the gate insulator (11 nF/cm^2 for the 300-nm thick SiO_2 insulator layer), and $V_{\rm T}$ is the threshold voltage. The calculated $\mu_{\rm FET}, V_{\rm T}$, and $I_{\rm on}/I_{\rm off}$ obtained from the transfer characteristic curve are 1.36×10^{-3} cm$^2 \cdot$V$^{-1} \cdot$s^{-1}, –18 V, and 10^5, respectively. The transfer and output characteristics of BC OFETs are shown in Figs. 2(c) and 2(d), respectively. The BC OFETs show $\mu_{\rm FET}, V_{\rm T}$, and $I_{\rm on}/I_{\rm off}$ of 1.41×10^{-4} cm$^2 \cdot$V$^{-1} \cdot$s^{-1}, 6.6 V, and 10^4 respectively. From the above results, we can see that the field effect mobility of the TC devices is one order of magnitude higher than that of the BC ones. To clarify the reason for the high performance of the TC devices, we investigated the morphologies of the CuPc films for both BC and TC devices, as shown in Figs. 3(a) and 3(b), respectively. From the images, we can see that CuPc films of TC devices have better molecular ordering and larger grain sizes than those of BC ones. In addition, the contact areas for TC devices are much larger than those of BC devices because the contact areas for TC devices are determined by the planar size of the top electrodes and the contact area for BC devices are determined by the side area of the bottom electrodes. The big contact area implied small contact resistance, so the contact resistances for TC devices are much smaller than those of BC devices.[15] For the above reasons, the TC devices offer better performance,[6,14–16] and they demonstrate that our method is a valuable method for TC OFETs fabricated by using a photolithographic technique.

Studying the effect of the PVP passivation layer, we propose TC OFETs fabricated by using a photolithographic process without a PVP layer. At the same time, we also prepare TC OFETs fabricated by using the conventional shadow method with a PVP passivation layer.

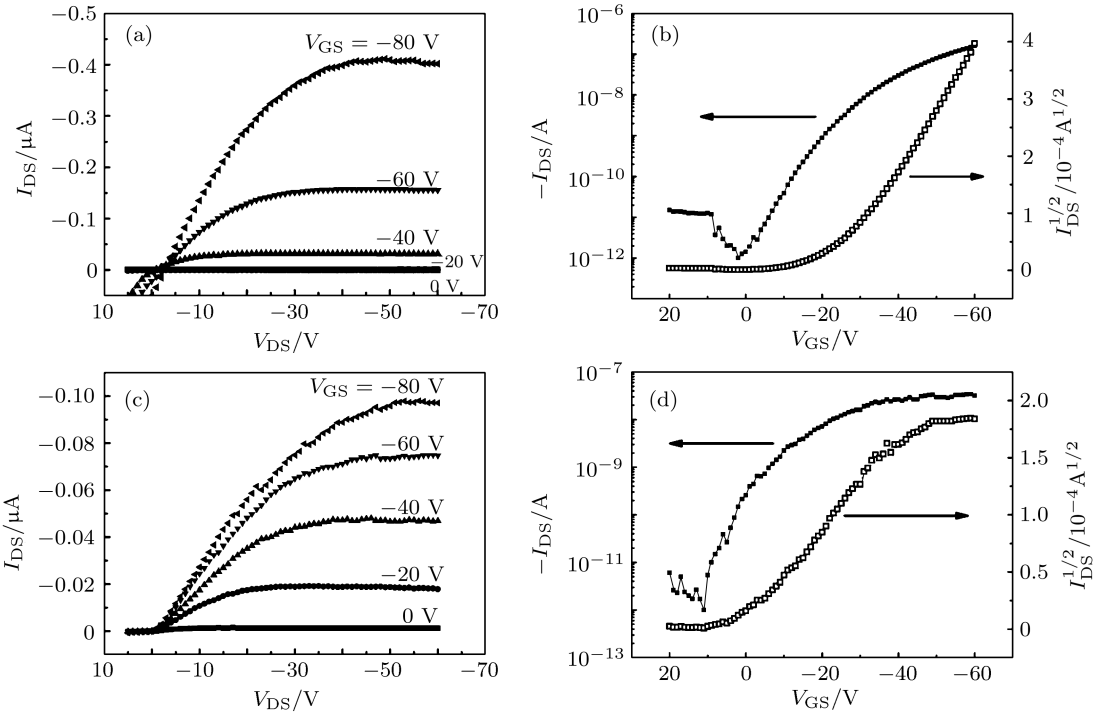


Fig. 2. Typical current voltage curves of OFETs fabricated by using a photolithographic process: (a) the output characteristic and (b) the transfer characteristic of the TC OFETs, (c) the output characteristic, and (d) the transfer characteristic of the BC OFETs.

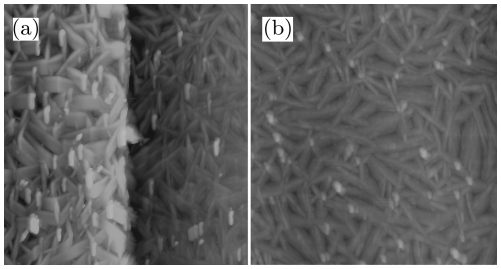


Fig. 3. The AFM images of CuPc films (scan size is 5 μm × 5 μm) on (a) the interface of S/D electrodes and channel (the right part is channel) and (b) OTS modified SiO_2.

Figure 4 shows the transfer and output characteristics of the TC OFETs fabricated by using a photolithographic process without a PVP passivation layer. The devices exhibit low mobility (3.34×10^{-5} $cm^2 \cdot V^{-1} \cdot s^{-1}$) and low I_{on}/I_{off} ratio (8×10^2) due to the destruction of the organic semiconductor layer by a photo resist.[24] Figure 5 shows the transfer characteristics of TC OFETs fabricated by using the shadow method with and without a PVP passivation layer. The mobility decreased from 3.51×10^{-3} $cm^2 \cdot V^{-1} \cdot s^{-1}$ to 1.49×10^{-3} $cm^2 \cdot V^{-1} \cdot s^{-1}$ when the devices were protected by a PVP layer, but the I_{on}/I_{off} ratio increased from 2×10^4 to 1×10^5 due to the reduction in off-state current of the devices with a PVP passivation layer. From these results we can see that the PVP has little negative effect, so it can be used as an efficiency passivation layer, and when the CuPc film was protected by a PVP layer, the influence of the photo resist could be reduced dramatically.

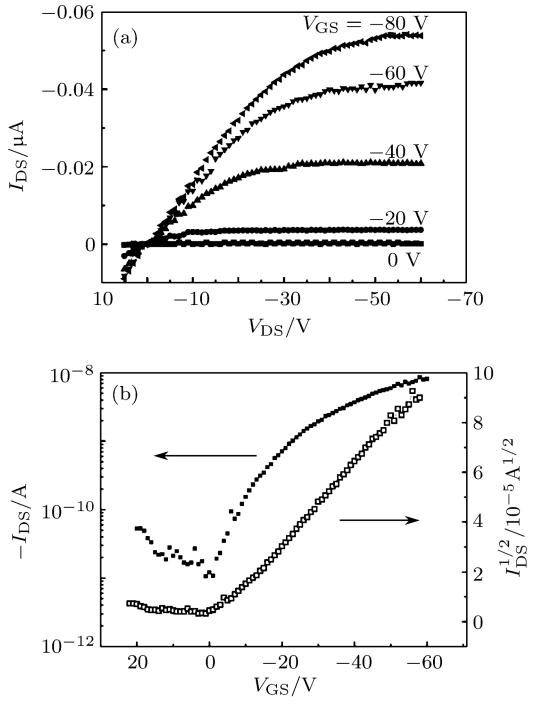


Fig. 4. (a) The output characteristic and (b) the transfer characteristic of TC OFETs fabricated by using a photolithographic process without a PVP passivation layer.

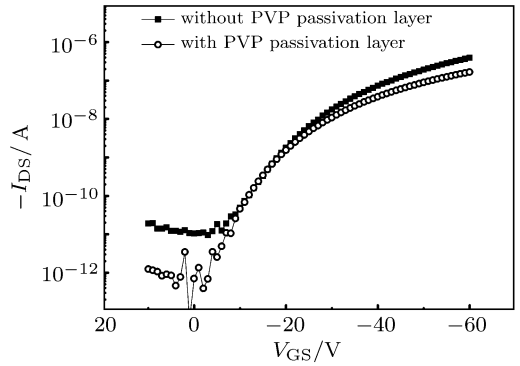


Fig. 5. The transfer characteristic TC OFETs fabricated by using the shadow method with and without a PVP passivation layer.

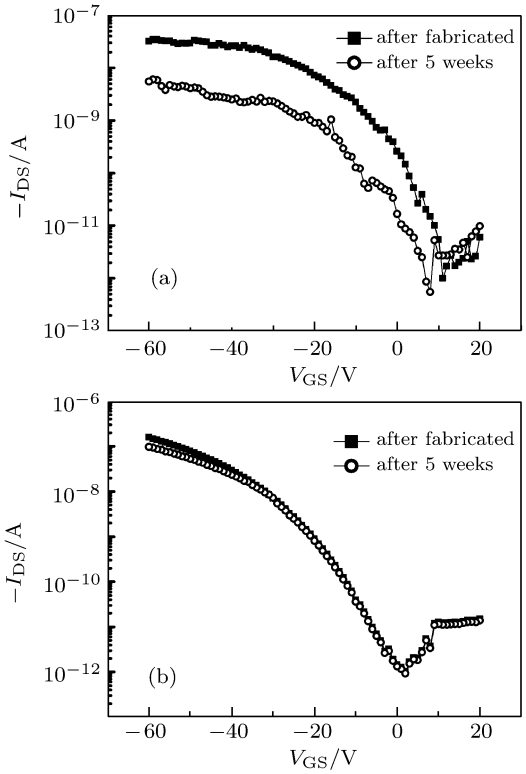


Fig. 6. The stability of OFETs fabricated by using a photolithographic process: (a) transfer characteristics measurement after fabricated and after 5 weeks of BC OFETs and (b) TC OFETs.

Figure 6 shows the stability of OFETs fabricated by using a photolithographic process. To explore the device stability, the electrical characteristics were measured immediately when fabricated and stored in air without any encapsulation for 5 weeks, respectively. The mobility of BC OFETs decreased from 1.41×10^{-4} $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$ to 2.49×10^{-5} $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$ due to the doping of oxygen and water in CuPc films in air.[25,26] The performance of TC OFETs shows no significant decrease, the mobility is 1.36×10^{-3} $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$ and 1.02×10^{-3} $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$ when fabricated and after 5 weeks, respectively. The better stability of TC OFETs is thanks to protection of the PVP dielectric layer. Therefore, with a passivation layer, using a photolithographic process is an effective way to fabricate TC OFETs.

4. Conclusion

In conclusion, a photolithographic process is demonstrated for the fabrication of TC OFETs. Compared with the traditional shadow mask method, we find that this process is more convenient for applications in organic circuits. To avoid the impact of a photolithographic process, the CuPc films were protected with PVP, through a photolithographic and RIE process, S/D electrodes patterns could be formed and TC OFETs could be carried out when the electrode materials were deposited. The mobility of TC OFETs fabricated using this method is comparable to that prepared by the shadow method and one order of magnitude higher than conventional BC OFETs, which were usually used in organic integrated circuits. From these results, we can conclude that the photolithographic process for fabricating TC OFETs is attractive.

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