A −188 V 7.2 Ω · mm^2, P-channel high voltage device formed on an epitaxy-SIMOX substrate*

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This paper proposes a new n$^+$-charge island (NCI) P-channel lateral double diffused metal–oxide semiconductor (LDMOS) based on silicon epitaxial separation by implantation oxygen (E-SIMOX) substrate. Higher concentration self-adapted holes resulting from a vertical electric field are located in the spacing of two neighbouring n$^+$-regions on the interface of a buried oxide layer, and therefore the electric field of a dielectric buried layer ($E_{\rm I}$) is enhanced by these holes effectively, leading to an improved breakdown voltage (BV). The $V_{\rm B}$ and $E_{\rm I}$ of the NCI P-channel LDMOS increase to –188 V and 502.3 V/μm from −75 V and 82.2 V/μm of the conventional P-channel LDMOS with the same thicknesses SOI layer and the buried oxide layer, respectively. The influences of structure parameters on the proposed device characteristics are investigated by simulation. Moreover, compared with the conventional device, the proposed device exhibits low special on-resistance.

Keywords: dielectric buried layer, breakdown voltage, self-adapted holes, epitaxy-SIMOX

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1. Introduction

Silicon on insulator (SOI) high voltage integrated circuit technology for plasma display panel (PDP) drivers is competitive.[1−5] (E-SIMOX) technology is one of the most ordinary and promising methods and is quite suitable for competitive PDP product.[6,7] A high-voltage P-channel SOI lateral double diffused metal–oxide semiconductor (LDMOS) is applied to the PDP scan driver chip.[8,9] The breakdown voltage (BV) of the SOI high voltage device is limited by the low vertical BV ($V_{\rm B}$) due to the presence of the buried oxide layer. Many SOI device structures have been proposed to improve $V_{\rm B}$.[10−18] In this paper, a novel P-channel high voltage LDMOS built on E-SIMOX is proposed, which introduces interface charges to enhance $E_{\rm I}$ and increase the $V_{\rm B}$. The effect of structure parameters on the BV are investigated by MEDICI[19] and special on-resistance is calculated.

2. Structure and mechanism

A new n$^+$-charge islands (NCI) P-channel LDMOS and its physical mechanism are shown in Fig. 1. Equidistant high concentration n$^+$-regions are made on the interface of a top dielectric buried layer (SiO_2). When a high negative voltage $V_{\rm d}$ is applied to the drain and substrate, while the source and gate are grounded, the accumulation holes are formed in the spacing of equidistant n$^+$-regions by the compositive operation of a vertical electric field ($E_{\rm V}$), Coulomb's forces with the ionized donors in the undepleted n$^+$-regions and lateral electric field ($E_{\rm L}$), electrons are induced and located on the interface of bottom dielectric buried layer (SiO_2).

The BV of a high voltage device fabricated on SOI, the field plate (FP) and reduced surface field (RESURF) are adopted in order to optimize the lateral BV, and thus the BV is determined by the vertical breakdown. $E_{\rm I} = q\sigma_{\rm acc}/\varepsilon_{\rm I} + (\varepsilon_{\rm S}/\varepsilon_{\rm I})E_{\rm S}$,[20−22] then the

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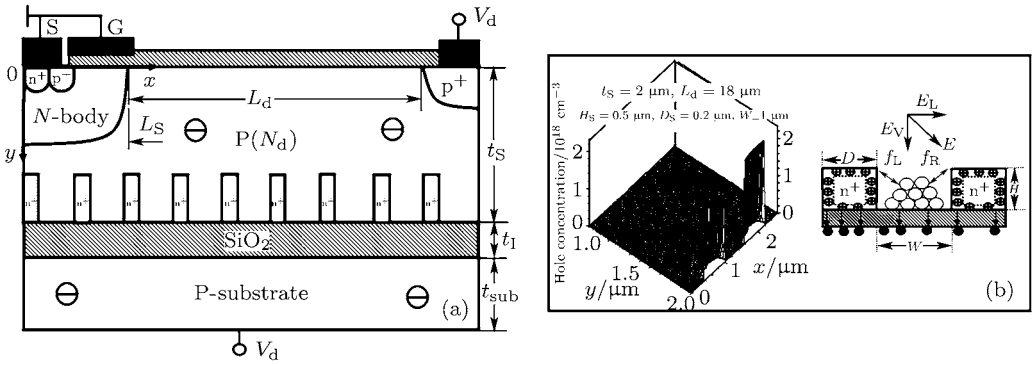


Fig. 1. Cross-sectional structure of NCI P-channel LDMOS and its physical mechanism: (a) device structure, (b) an NCI cell and three-dimensional holes distribution under the source. t_S, t_I, t_{sub}, and H are respectively the thicknesses of top silicon layer, dielectric buried layer, substrate layer and interface n^+-regions, L_d, L_s, D, and W are respectively the lengths of drift region, source (n-body), interface n^+-regions, and the spacing of two neighbouring n^+-regions, N_d are impurity concentrations of the drift region, f_L and f_R are respectively the Coulomb's forces from the left and right ionizing n-type ions in the undepleted n^+-regions.

V_B of SOI is obtained as

$$\begin{aligned} V_B &= t_I E_I + 0.5 t_S E_S \\ &= \frac{q\sigma_{acc} t_I}{\varepsilon_I} + \left(0.5 t_S + \frac{\varepsilon_S}{\varepsilon_I} t_I\right) E_S, \end{aligned} \tag{1}$$

where E_S, E_I are the electric fields of the top silicon layer and the buried dielectric layer, respectively, q is the electron charge, σ_{acc} is the interface accumulated charge, ε_S and ε_I are the permittivities of the silicon and dielectric buried layer, respectively, and t_S and t_I are the thicknesses of the top silicon layer and dielectric buried layer, respectively.

When the drift region is fully depleted, the depleted region potential $\varphi(x,y)$ satisfies the 2D Poisson equation:

$$\begin{aligned} &\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_S}, \\ &0 \le x \le L_d + L_s, \quad 0 \le y \le t_S. \end{aligned} \tag{2}$$

The boundary conditions can be written as

$$\left.\frac{\partial \varphi(x,y)}{\partial y}\right|_{y=0} = 0, \tag{2a}$$

$$\left.\frac{\partial \varphi(x,y)}{\partial y}\right|_{y=t_S} = \frac{q\sigma_{acc}(x)}{\varepsilon_S} - \frac{\varepsilon_I \varphi(x,t_S)}{\varepsilon_S t_I}, \tag{2b}$$

$$\varphi(0,0) = 0, \quad \varphi(L_d + L_s, 0) = V_d, \tag{2c}$$

$$0 \le x \le L_d + L_s, \quad 0 \le y \le t_S,$$

$\varphi(x,y)$ can be expressed as a combination of two parts

$$\begin{aligned} &\varphi(x,y) = \omega(x,y) + \psi(x,y), \\ &0 \le x \le L_d + L_s, \quad 0 \le y \le t_S, \end{aligned} \tag{3}$$

where $\omega(x,y)$ and $\psi(x,y)$ are the contributions of V_d and depleted charge, respectively. So, equations of two parts of the electric potential can be obtained as follows,

$$\begin{aligned} &\frac{\partial^2 \omega(x,y)}{\partial x^2} + \frac{\partial^2 \omega(x,y)}{\partial y^2} = 0, \\ &\omega(0,0) = 0, \quad \omega(L_d + L_s, 0) = V_d, \\ &\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_S}, \\ &\psi(0,0) = 0, \quad \psi(L_d + L_s, 0) = 0, \end{aligned} \tag{4}$$

with $0 \le x \le L_d + L_s, 0 \le y \le t_S$. To make $\omega(x,y)$ as a Taylor series along the y direction

$$\begin{aligned} \omega(x,y) \cong\ & \omega(x,0) + \left.\frac{\partial \omega(x,y)}{\partial y}\right|_{y=0} \cdot y \\ &+ \left.\frac{\partial^2 \omega(x,y)}{\partial y^2}\right|_{y=0} \cdot \frac{y^2}{2} \cdots\cdots \end{aligned} \tag{5}$$

Simplify Eq. (5) with the boundary condition (2a) yields[23]

$$\begin{aligned} &\omega(x,y) = \omega(x,0) + \left.\frac{\partial^2 \omega(x,y)}{\partial y^2}\right|_{y=0} \cdot \frac{y^2}{2}, \\ &0 \le x \le L_d + L_s, \quad 0 \le y \le t_S, \end{aligned} \tag{6}$$

$$\left.\frac{\partial \omega(x,y)}{\partial y}\right. = \left.\frac{\partial^2 \omega(x,y)}{\partial y^2}\right|_{y=0} \cdot y,$$

$$\left.\frac{\partial \omega(x,y)}{\partial y}\right|_{y=t_S} = \left.\frac{\partial^2 \omega(x,y)}{\partial y^2}\right|_{y=0} \cdot t_S. \tag{7}$$

Solving Eq. (7) with the boundary condition (2b) yields

$$\begin{aligned} &\left.\frac{\partial^2 \omega(x,y)}{\partial y^2}\right|_{y=0} \cdot t_S = -\frac{\varepsilon_I \omega(x,t_S)}{\varepsilon_S t_I}, \\ &0 \le x \le L_d + L_s, \quad 0 \le y \le t_S, \end{aligned} \tag{8}$$

then, making $y = t_S$ for Eq. (7), then equation (8) can be simplified as

$$\left.\frac{\partial^2 \omega(x,y)}{\partial y^2}\right|_{y=0} = -\frac{\omega(x,0)}{t^2},$$

$$0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}, \tag{9}$$

where $t = \sqrt{t_{\rm S}^2/2 + (\varepsilon_{\rm S}/\varepsilon_{\rm I})t_{\rm S}t_{\rm I}}$ is the characteristic thickness of SOI devices.

From Eqs. (4) and (9), we obtain the following equation and the boundary conditions

$$\begin{aligned} &\frac{\partial^2\omega(x,0)}{\partial x^2} - \frac{\omega(x,0)}{t^2} = 0, \\ &\omega(0,0) = 0, \quad \omega(L_{\rm d}+L_{\rm s},0) = V_{\rm d}. \end{aligned} \tag{10}$$

Solving Eqs. (6) and (10), the equation of electric potential $\omega(x,y)$ is

$$\begin{aligned} &\omega(x,y) = \left(1 - \frac{y^2}{2t^2}\right)\omega(x,0), \\ &0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}. \end{aligned} \tag{11}$$

Solving Eqs. (10) and (11), the electric potential $\omega(x,0)$ can be obtained,

$$\omega(x,0) = \frac{\sinh(x/t)V_{\rm d}}{\sinh((L_{\rm d}+L_{\rm s})/t)}, \ 0 \le x \le L_{\rm d} + L_{\rm s}. \tag{12}$$

Using the same method as presented above, the electric potential $\psi(x,y)$ distribution can be obtained as

$$\begin{aligned} &\frac{\partial^2\psi(x,y)}{\partial x^2} - \frac{\psi(x,0)}{t^2} = -\frac{qN_{\rm d}}{\varepsilon_{\rm S}} - \frac{t_{\rm I}q\sigma_{\rm acc}(x)}{\varepsilon_{\rm I}t^2} \\ &\psi(0,0) = 0, \quad \psi(L_{\rm d}+L_{\rm s},0) = 0, \\ &0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}. \end{aligned} \tag{13}$$

Then, solving Eq. (13), the electric potential $\psi(x,y)$ can be expressed,

$$\begin{aligned} &\psi(x,y) = \left(1 - \frac{y^2}{2t^2}\right)\psi(x,0) + \frac{y^2}{2}\frac{t_{\rm I}q\sigma_{\rm acc}(x)}{\varepsilon_{\rm I}t^2}, \\ &0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}. \end{aligned} \tag{14}$$

Making $\sigma_{\rm acc}(x) = \sigma_{\rm acc}$, solving Eq. (14) with the boundary conditions yields

$$\psi(x,0) = \frac{t^2qN_{\rm d}/\varepsilon_{\rm S} + t_{\rm I}q\sigma_{\rm acc}/\varepsilon_{\rm I}}{\sinh((L_{\rm d}+L_{\rm s})/t)}\left[1 + \sinh\left[\frac{(x - L_{\rm d} - L_{\rm s})}{t}\right] - \sinh\left(\frac{x}{t}\right)\right]. \tag{15}$$

From Eq. (3), the surface electric potential distribution $\varphi(x,0)$ can be obtained as

$$\varphi(x,0) = \frac{(V_{\rm d} - \beta - t_{\rm I}q\sigma_{\rm acc}/\varepsilon_{\rm I})\sinh(x/t) + (\beta + t_{\rm I}q\sigma_{\rm acc}/\varepsilon_{\rm I})\sinh[(x - L_{\rm d} - L_{\rm s})/t]}{\sinh((L_{\rm d}+L_{\rm s})/t)} + \beta + \frac{t_{\rm I}q\sigma_{\rm acc}}{\varepsilon_{\rm I}}, \tag{16}$$

where $\beta = t^2qN_{\rm d}/\varepsilon_{\rm S}$.

From Eqs. (11) and (14), the electric potential distribution $\varphi(x,y)$ can be denoted as

$$\varphi(x,y) = \left(1 - \frac{y^2}{2t^2}\right)\varphi(x,0) + \frac{y^2}{2}\cdot\frac{t_{\rm I}q\sigma_{\rm acc}}{t^2\varepsilon_{\rm I}}, \quad 0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}. \tag{17}$$

Then, according to the relationship between electric potential and electric field, from Eq. (16), $E_x(x,0)$ can be written as

$$E_x(x,0) = -\frac{\partial\varphi(x,0)}{\partial x} = -\frac{(V_{\rm d} - \beta - t_{\rm I}q\sigma_{\rm acc}/\varepsilon_{\rm I})\cosh(x/t) + (\beta + t_{\rm I}q\sigma_{\rm acc}/\varepsilon_{\rm I})\cosh[(x - L_{\rm d} - L_{\rm s})/t]}{t\sinh((L_{\rm d}+L_{\rm s})/t)}. \tag{18}$$

From Eq. (17), according to the relationship between the electric potential and the electric field, $E_x(x,y)$ can be written as

$$\begin{aligned} &E_x(x,y) = -\frac{\partial\varphi(x,y)}{\partial x} = \left(1 - \frac{y^2}{2t^2}\right)E_x(x,0), \\ &0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}. \end{aligned} \tag{19}$$

For the fully depleted drift region, the vertical electric field in the top silicon layer satisfies

$$\begin{aligned} &E_y(x,y) = -\frac{\partial\varphi(x,y)}{\partial y} = \frac{y}{t^2}\varphi(x,0) - \frac{yt_{\rm I}q\sigma_{\rm acc}}{t^2\varepsilon_{\rm I}}, \\ &0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}. \end{aligned} \tag{20}$$

So, the surface electric field and total electric field can be shown as

$$\begin{aligned} &|E(x,0)| = |E_x(x,0)|, \\ &|E(x,y)| = \sqrt{E_x^2(x,y) + E_y^2(x,y)}, \\ &0 \le x \le L_{\rm d} + L_{\rm s}, \quad 0 \le y \le t_{\rm S}. \end{aligned} \tag{21}$$

With Eq. (21) and Gauss theory on the interface, the vertical electric fields in the silicon and dielectric buried layer (under the source) $E_{\rm S}$ and $E_{\rm I}$ are approximately obtained as

$$\begin{aligned} E_{\rm S} = &\frac{t_{\rm S}}{t^2}\left[V_{\rm d} - \varphi(L_{\rm d}+L_{\rm s}, t_{\rm S}+t_{\rm I})\right] \\ &- \frac{t_{\rm S}t_{\rm I}q\sigma_{\rm acc}}{t^2\varepsilon_{\rm I}}, \end{aligned} \tag{22}$$

$$E_{\rm I} = \frac{\varepsilon_{\rm S} t_{\rm S}}{\varepsilon_{\rm I} t^2} \left[V_{\rm d} - \varphi(L_{\rm d} + L_{\rm s}, t_{\rm S} + t_{\rm I}) \right] + \frac{q\sigma_{\rm acc}}{\varepsilon_{\rm I}} \left(1 - \frac{t_{\rm S} t_{\rm I} \varepsilon_{\rm S}}{t^2 \varepsilon_{\rm I}} \right). \quad (23)$$

From Eqs. (22) and (23), the enhancement of BV introduced by charges $\sigma_{\rm acc}$ for NCI SOI, $E_{\rm I}$ can be increased in comparison with the conventional SOI ($\sigma_{\rm acc} = 0$) by the additional charges, and $E_{\rm S}$ can be reduced at a given $V_{\rm d}$, shielding the Si layer from a high electric field and avoiding Si-layer premature breakdown. Both of them result in an enhanced BV, as indicated in Eq. (1). Moreover, when $\sigma_{\rm acc} = 0$, equations (22) and (23) can be used for the conventional SOI.

3. Results and discussion

The simulated device parameters using device simulator MEDICI are listed in Table 1.

Table 1. Simulated device parameters.

Parameters	NCI SOI	Conv. SOI
Drift length $L_{\rm d}$	15 μm–30 μm	15 μm–30 μm
SOI thickness $t_{\rm S}$	2 μm	2 μm
BOX thickness $t_{\rm I}$	0.375 μm	0.375 μm
P-substrate thickness $t_{\rm sub}$	1 μm	1 μm
P-substrate concentration $N_{\rm sub}$	(1–10)×10^{14} cm^{-3}	(1–10)×10^{14} cm^{-3}
NCI thickness H	0 μm–1 μm	
n^+-region length D	0 μm–1 μm	
Spacing of two neighboring n^+-region W	1 μm–2 μm	
n^+-region concentration N_{n+}	(0.1–1)×10^{19} cm^{-3}	

The changes to $E_{\rm S}$ (y = 1.999 μm) and $E_{\rm I}$ (y = 2.001 μm) at x = 0.2 μm for NCI SOI and the conventional SOI with an augment of the applied voltage $V_{\rm d}$ are shown in Fig. 2. From Eqs. (22) and (23), $E_{\rm S}$ and $E_{\rm I}$ at breakdown ($V_{\rm d} = V_{\rm B}$ = BV) for NCI SOI are reduced and enhanced by the interface holes in comparison with the conventional SOI as

$$\Delta E_{\rm S} = \frac{t_{\rm S}}{t^2} \left[V_{\rm d} - \Delta\varphi(L_{\rm d} + L_{\rm s}, t_{\rm S} + t_{\rm I}) \right] - \frac{t_{\rm S} t_{\rm I} q\sigma_{\rm acc}}{t^2 \varepsilon_{\rm I}}, \quad (24)$$

$$\Delta E_{\rm I} = \frac{\varepsilon_{\rm S} t_{\rm S}}{\varepsilon_{\rm I} t^2} \left[V_{\rm d} - \Delta\varphi(L_{\rm d} + L_{\rm s}, t_{\rm S} + t_{\rm I}) \right] + \frac{q\sigma_{\rm acc}}{\varepsilon_{\rm I}} \left(1 - \frac{t_{\rm S} t_{\rm I} \varepsilon_{\rm S}}{t^2 \varepsilon_{\rm I}} \right), \quad (25)$$

Figure 2 shows that due to the self-adapted increasing of the accumulated holes with the $V_{\rm d}$, $E_{\rm I}$ is linearly enhanced, and simultaneously, $E_{\rm S}$ is reduced to less than 3.13 V/μm. However, because of no n^+-region preventing the extraction of interface charges by the electric field in the drift region, $E_{\rm I}$ of the conventional SOI is always limited by the dependence of $E_{\rm I} = \varepsilon_{\rm S} E_{\rm S}/\varepsilon_{\rm I}$ from Eqs. (22) and (23), and $E_{\rm S}$ rapidly reaches the silicon critical electric field. When $V_{\rm d} = V_{\rm B}$ = BV, $E_{\rm I}$ of NCI SOI reaches to 502.3 V/μm from 82.2 V/μm ($\Delta E_{\rm I}$ = 402.1 V/μm) of the conventional SOI, and $E_{\rm S}$ of NCI SOI decreases to 3.13 V/μm from 38.6 V/μm ($\Delta E_{\rm S}$ = 35.47 V/μm) of the conventional SOI, because of which, NCI SOI has a higher $V_{\rm B}$ (–188 V) than –75 V of the conventional SOI. It is shown that equations (24) and (25) agree with the simulations illustrated in Fig. 2.

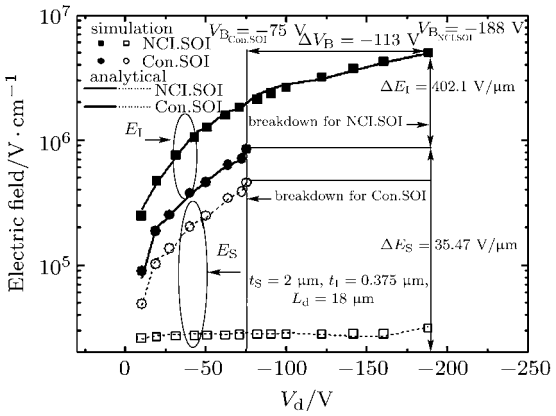


Fig. 2. Dependences of the applied voltages $V_{\rm d}$ on the interface electric fields (at 0.2-μm point) under the source in the silicon layer $E_{\rm S}$ (y = 1.999 μm) and dielectric buried layer $E_{\rm I}$ (y = 2.001 μm) for the NCI.SOI and the conventional SOI ($t_{\rm S}$ = 2 μm, $t_{\rm I}$ = 0.375 μm, $t_{\rm sub}$ = 1 μm, $L_{\rm d}$ = 18 μm, D = 0.2 μm, H = 0.5 μm, W = 1 μm, $N_{n+} = 1 \times 10^{19}$ cm^{-3}, and $N_{\rm sub} = 8 \times 10^{14}$ cm^{-3}).

The equipotential contours and surface electric field (y = 0.001 μm) for NCI P-channel LDMOS and the conventional SOI at breakdown are compared in Fig. 3. A more uniform equal-potential line distribution in the SOI layer for NCI SOI is obtained due to

the modulation effect of the high concentration holes ($> 2 \times 10^{18}$ cm^{-3}) on the interface. However, that of the conventional SOI is concentrated on the end of the drift region. Due to the fact that the equipotential contours of the conventional SOI cannot spread into the whole drift region, the conventional SOI has a low BV. Moreover, owing to the modulation effect of holes increasing from the drain to the source, the surface field in the middle of the drift region for the NCI SOI is higher than that of the conventional SOI and the surface electric field has two electric field peaks at the source- and drain-ends of the NCI SOI, avoiding premature breakdown. Compared with the conventional SOI, one has only one electric field peak at the source-end.

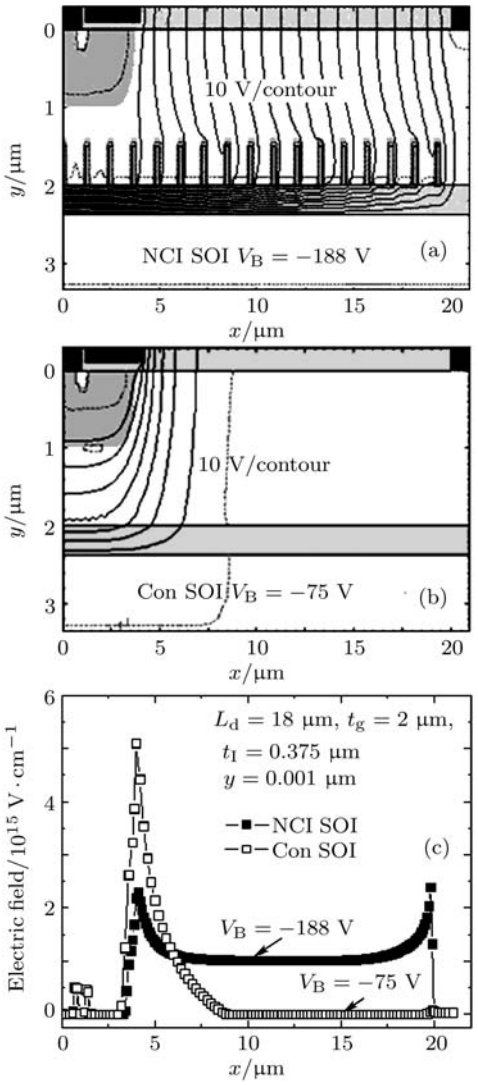


Fig. 3. Equipotential contours and surface electric field profiles for NCI SOI and conventional SOI devices: (a) NCI SOI, (b) conventional SOI, (c) distribution of surface electric field ($y = 0.001$ μm) for NCI SOI and conventional SOI.

The charge distribution for the NCI SOI LDMOS along the top ($y = 1.999$ μm) and the bottom ($y = 2.375$ μm) interface of the SiO_2 layer at $V_d =$ BV is shown in Fig. 4. Figure 4(a) is the hole and electron concentration on both the top and bottom interfaces of the buried dielectric layer for the NCI SOI LDMOS at breakdown. Plentiful holes are located on the top interface, whose concentration increases from the drain to the source with interface potential. Moreover, there are 10^{17} cm^{-3}-level electrons existing on the bottom interface. Figure 4(b) gives the hole distribution in a NCI cell, in which the highest hole concentration is at the middle point (centre of two n^+-regions) due to the maximal Coulomb force at that point. From Fig. 4(b), the accumulated layer is about 90 nm. Based on Eqs. (1), (22) and (23), the interface accumulated holes should not only enhance E_I but also modulate the electric field in the drift region, leading to the enhancement of the lateral and vertical BVs.

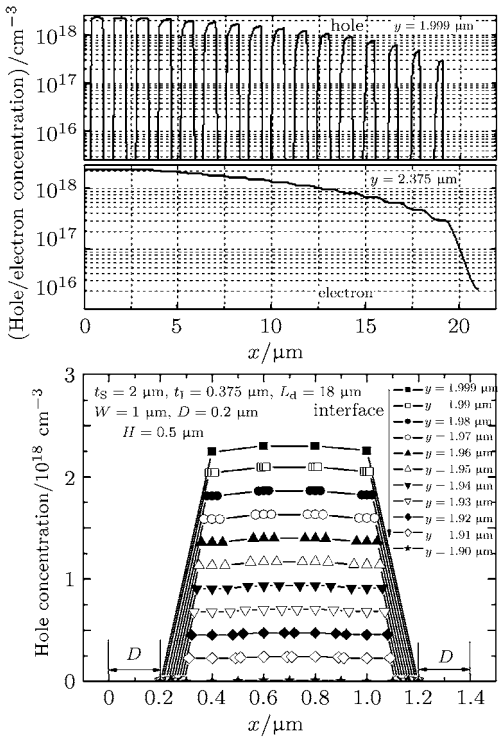


Fig. 4. Charge distribution for the NCI SOI LDMOS at breakdown voltage ($t_S = 2$ μm, $t_I = 0.375$ μm, $L_d = 18$ μm, $D = 0.2$ μm, $H = 0.5$ μm, $W = 1$ μm): (a) hole/electron concentrations on both the top ($y = 1.999$ μm) and bottom ($y = 2.375$ μm) interfaces of the buried dielectric layer, (b) hole distribution in an NCI cell with different vertical distance.

From Eq. (1) and Fig. 1(b), interface charges can effectively enhance E_I from the conventional $\varepsilon_S E_S/\varepsilon_I$ (about $3E_S$) to $\varepsilon_S Es/\varepsilon_I + q\sigma_{in}/\varepsilon_I$, and each adding interface charges to 1×10^{12} cm^{-2} can enhance E_I of

41.3 V/μm. Figure 5 depicts the vertical electric field and potential distributions at breakdown under the source. The modulation effect of holes on the electric fields can not only reduce E_S but also increase E_I. In two of n^+-regions, based on Eqs. (22) and (23), we find the results that E_I and E_S are from E_I = 82.2 V/μm and E_S = 38.6 V/μm of conventional SOI to E_I = 502.3 V/μm and E_S = 3.13 V/μm of NCI SOI. A larger portion of the applied voltage is sustained by bury oxide (BOX) for p-channel NCI SOI, thus $V_B = -188$ V is achieved with t_S = 2 μm and t_I = 0.375 μm by simulation, while V_B is only −75 V for the conventional SOI.

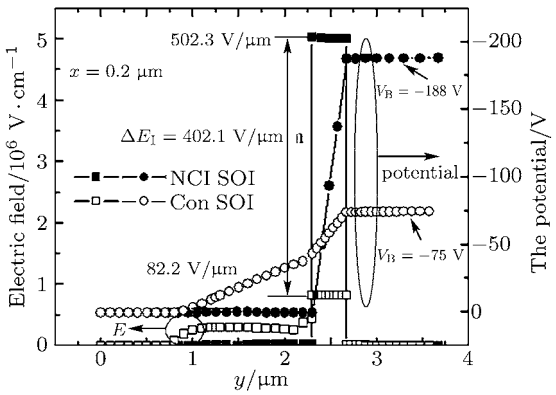


Fig. 5. Electric field and potential distributions at breakdown for the NCI P-channel LDMOS, the conventional SOI (t_S = 2 μm, t_I = 0.375 μm, t_{sub} = 1 μm, L_d = 18 μm, and $N_{sub} = 8 \times 10^{14}$ cm^{-3} for all). The N_d are 5.7×10^{15} cm^{-3} and 2×10^{15} cm^{-3} for the two structures, respectively.

In order to obtain a maximum BV, the total charges in the drift regions should satisfy the reduced surface field (RESURF). The influence of the structure parameters on the BV for the NCI P-channel LDMOS is simulated in Fig. 6. It can be seen from Fig. 6 that the optimal structure parameters are H = 0.5 μm, D = 0.2 μm, and W = 1 μm, there is a maximum BV = −188 V, and BV almost keeps improving linearly with increasing L_d just shown in Fig. 6, too. Moreover, when H or D is 0 μm, NCI P-channel LDMOS will become a conventional SOI (BV = −75 V).

Figure 7(a) shows vertical electric fields in Si (E_{SV}) and in SiO_2 (E_{IV}) on the top interface at the x axis. For NCI SOI, $\Delta E_I(x)$ increases with the hole concentration of Fig. 7 from drain to source and E_{IV} is much larger than $3E_{SV}$ under the source in comparison with the conventional dependence of $E_{IV} = 3E_{SV}$. The $E_{SV}(x)$ for each point is almost invariable because of a series of $n^+p^-n^+$-structures (NCI cell) with a sustained applied voltage of 10 V, as shown in Fig. 3, and $E_{SV}(x)$ is low under 30 V/μm due to the avoidance effect of the holes, whereas those of a conventional SOI increase from drain to source with the potential and reach to 30 V/μm under the source where breakdown occurs (x = 2.2 μm). The breakdown point for NCI SOI is at x = 4.53 μm because of a high lateral electric field. The enhancement of holes on E_I can be clearly seen from the 3D distribution of electric field, as shown in Fig. 7(b).

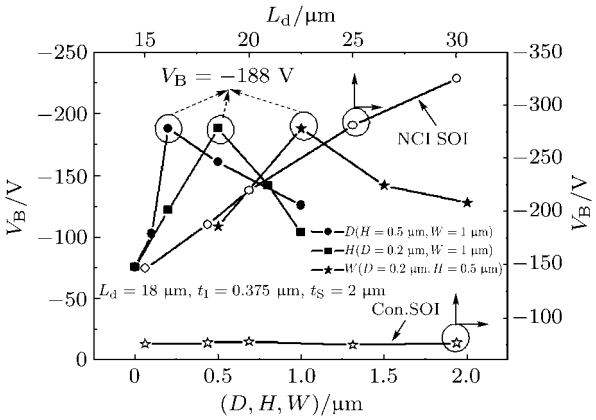


Fig. 6. Influence of device parameters on breakdown voltage. t_S = 2 μm, t_I = 0.375 μm, t_{sub} = 1 μm for all.

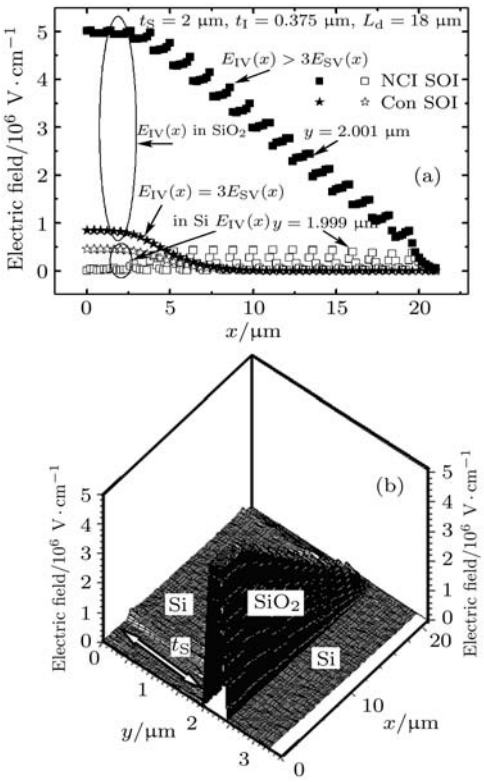


Fig. 7. Electric field distribution at breakdown (t_S = 2 μm, t_I = 0.375 μm, L_d = 18 μm, D = 0.2 μm, H = 0.5 μm, W = 1 μm), (a) vertical electric fields in Si (E_{SV}) and in SiO_2 (E_{IV}) on the top interface; (b) 3D distribution of electric fields.

The influence of N_{n+} (concentration of n^+-regions) on BV, E_I and the maximal hole concentration under source $N_{h,m}$ are shown in Fig. 8. When N_{n+} is larger than 1.85×10^{18} cm^{-3}, BV, E_I, and $N_{h,m}$ are invariable. However, N_{n+} is less than 1.85×10^{18} cm^{-3}, BV decreases with the decreasing N_{n+}, the reason of that when N_{n+} is larger than 1.85×10^{18} cm^{-3}, the n^+-regions under the source are undepleted and the ionized donors are invariable, then BV, E_I, and $N_{h,m}$ are independent of N_{n+}.

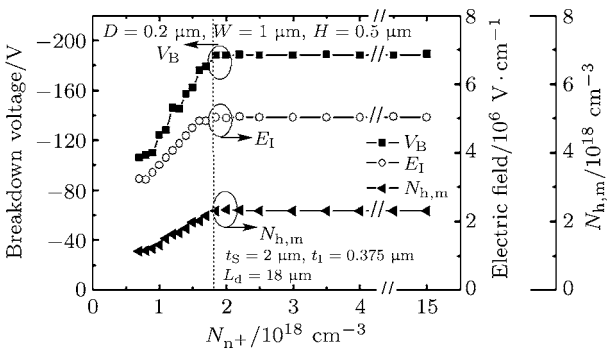


Fig. 8. Influence of interface n^+-region concentration N_{n+} on breakdown voltage, E_I and the maximal hole concentration $N_{h,m}$.

The on-state characteristics between the NCI SOI and the conventional SOI have been compared. The simulation results are tabulated in Table 2. The simulated NCI SOI has an $R_{on,sp}$ of 72 m$\Omega \cdot$cm^2 at $V_{gs} = -25$ V, $V_{ds} = -20$ V while the corresponding values in the conventional SOI are 90 m$\Omega \cdot$cm^2 for the same bias condition. It is calculated to be 20% lower in comparison with that of its counterpart. The improvement in the on-state characteristics must be due to the fact that a higher concentration n^+-implanted layer implemented in the drift region results in the heavy dopant in the drift region, which reduces the on-resistance of the NCI SOI.

Table 2. TDC performance comparison between the NCI SOI and a conventional SOI.

Device		V_B/V	$R_{on,sp}$/m$\Omega \cdot$cm^2
NCI SOI	$V_{gs} = -25$ V	−188	72
	$V_{gs} = -20$ V		87.8
Conventional SOI	$V_{gs} = -25$ V	−75	90
	$V_{gs} = -20$ V		120

The major nodes of the process flow are depicted in Fig. 9, and the associated device cross sections are shown in Fig. 10 for the NCI SOI LDMOS. The NCI SOI LDMOS was fabricated on a SIMOX substrate. The n^+-regions can form by implanting 2×10^{14} cm^{-2} arsenic at 150 keV, followed by annealing with the same conditions. The thickness of the n^+-regions after masked implantation processing was estimated as 200 nm. Then the 2-μm silicon layer could be achieved by using epitaxy technology at 1100 °C with 1×10^{15} cm^{-2} for 1.8-μm thickness. The n-body uses the phosphorus ion beam implantation process, followed by a high temperature drive to create regions (shown in Fig. 9). So only an additional process of arsenic implantation before bonding is needed to form an NCI SOI. Other fabrication processes are fully compatible with conventional CMOS/SOI technology.

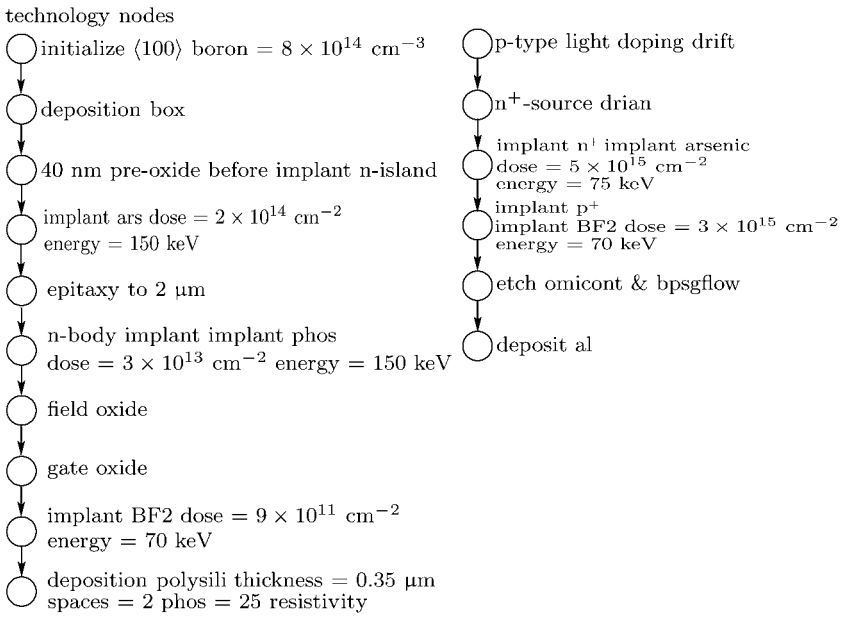


Fig. 9. Summary of process flow nodes (the node data are simulated by TSUPREM4).

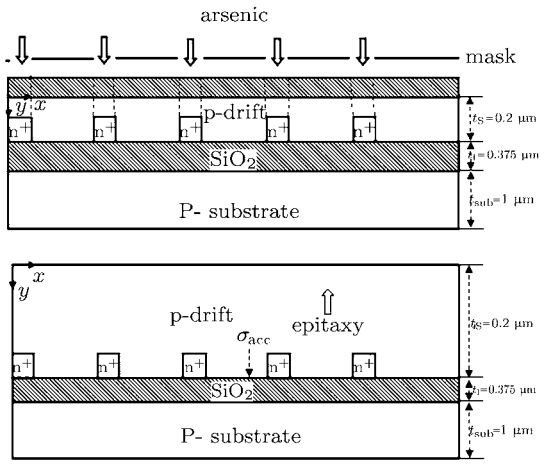


Fig. 10. Schematic principle of E-SIMOX NCI SOI technology: (a) arsenic implantation forms n^+-regions; (b) silicon layer epitaxy to 2 μm.

4. Conclusion

A −188 V P-channel LDMOS is proposed. The NCI SOI effectively utilizes the enhancement effect of the additional self-adapted positive charges on the electric field of the dielectric buried layer to increase the breakdown voltage. Compared with the conventional SOI with the same t_S, t_I, and L_d, V_B increases by 150.67%. The $E_I = 502.3$ V/μm is obtained on a 2-μm-thick SOI over a 0.375-μm-thick buried layer, and $R_{on,sp}$ is reduced by 20% in comparison with those of the conventional SOI LDMOS. This result, coupled with the CMOS-compatible fabrication process, makes the NCI SOI-LDMOS a competitive device for SPIC applications.

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