Compound buried layer SOI high voltage device with a step buried oxide*

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A silicon-on-insulator (SOI) high performance lateral double-diffusion metal oxide semiconductor (LDMOS) on a compound buried layer (CBL) with a step buried oxide (SBO CBL SOI) is proposed. The step buried oxide locates holes in the top interface of the upper buried oxide (UBO) layer. Furthermore, holes with high density are collected in the interface between the polysilicon layer and the lower buried oxide (LBO) layer. Consequently, the electric fields in both the thin LBO and the thick UBO are enhanced by these holes, leading to an improved breakdown voltage. The breakdown voltage of the SBO CBL SOI LDMOS increases to 847 V from the 477 V of a conventional SOI with the same thicknesses of SOI layer and the buried oxide layer. Moreover, SBO CBL SOI can also reduce the self-heating effect.

Keywords: breakdown voltage, step buried oxide, compound buried layer, self-heating effect

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1. Introduction

Silicon-on-insulator (SOI) technology suffers from a low vertical breakdown voltage and the self-heating effect (SHE) due to the presence of the buried oxide layer. Many SOI device structures have been proposed to improve the vertical breakdown voltage by enhancing the electric field in the buried dielectric layer (called $E_{\rm I}$).[1−13] One of the effective methods for increasing $E_{\rm I}$ is by introducing interface charges.[3−8] The compound buried layer (CBL) SOI device structure has been proposed and fabricated by Luo *et al.*[3] Its breakdown voltage is improved because the voltage sustained by the lower buried oxide layer (LBO) is enhanced by the holes collected in the interface between the polysilicon layer and the LBO. A step buried oxide (SBO) SOI structure has also been proposed by our group to enhance the breakdown voltage by locating holes at the steps of the buried oxide.[6]

Combining the SBO SOI structure and the CBL SOI structure, an SBO CBL SOI structure is proposed and its breakdown mechanism is investigated by MEDICI. The structure not only further improves the breakdown voltage, but also maintains a reduced self-heating effect.

2. Structure and mechanism

Figure 1(a) shows the schematic cross section of an SBO CBL SOI LDMOS. The CBL of the SBO CBL SOI consists of the upper buried oxide (UBO) layer and LBO layer, as well as a polysilicon layer between them, with a window and a SBO on the UBO.

Field plates and double RESURF technology are used to improve the lateral breakdown voltage. When a high positive voltage $V_{\rm d}$ is biased to the drain while the source, gate and substrate are grounded, inverse hole layers are formed and are located in the top interfaces of the UBO and the LBO. The SBO prevents the extraction of holes in the UBO top interface and the UBO prevents extraction in the LBO top interface by the lateral electric field in the drift region, as shown in Fig. 1(b). So the breakdown voltage of a CBL SOI LDMOS can be approximately expressed as

$$\begin{aligned} V_{\rm b} = {} & 0.5E_{\rm S}\varepsilon_{\rm S} + t_{\rm I1}(E_{\rm S}\varepsilon_{\rm S} + qQ_{\rm I1})/\varepsilon_{\rm I} \\ & + t_{\rm I2}(E_{\rm P}\varepsilon_{\rm S} + qQ_{\rm I2})/\varepsilon_{\rm I}, \end{aligned} \tag{1}$$

where $Q_{\rm I1}$ and $Q_{\rm I2}$ are the hole density on the top interfaces of the UBO and LBO. $E_{\rm S}$ and $E_{\rm P}$ are the bottom interface electric fields of the SOI layer and the polysilicon layer, respectively; $\varepsilon_{\rm S}$ and $\varepsilon_{\rm I}$ are the permittivity of Si and SiO_2.

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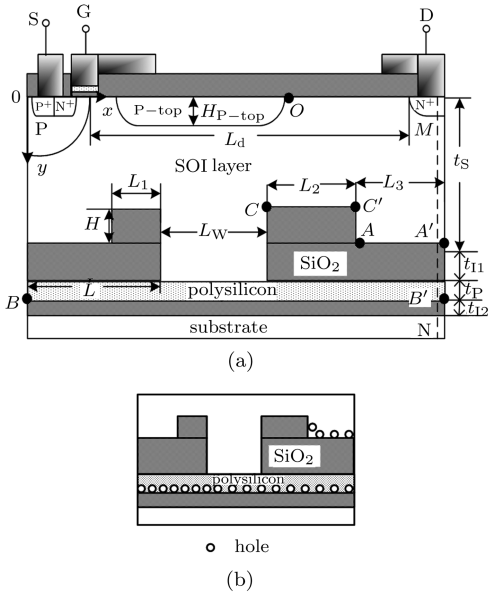


Fig. 1. Schematic cross sections of an SBO CBL SOI LDMOS and the holes on the interface of the UBO and LBO: (a) device structure, (b) holes distribution. H is the height of the SBO; L_1 and L_2 are the lengths of the left SBO and right SBO, respectively; L_d and L_W are the lengths of the drift region and window, respectively; L is the length of the left UBO; t_S, t_{I1}, t_{I2}, t_P and H_{P-top} are the thicknesses of the SOI layer, UBO, LBO and P-top, respectively.

Figure 2 shows the hole concentration distributions in y-direction in the top surfaces of the UBO and LBO at the drain end ($x = 79$ μm). From Fig. 2, it can be calculated that

$$Q_{I1} = (0.05 \times 10^{-4} N_{I1})\ \mathrm{cm}^{-2}, \tag{2}$$

$$Q_{I2} = (0.05 \times 10^{-4} N_{I2})\ \mathrm{cm}^{-2}, \tag{3}$$

where N_{11} and N_{12} (in units of cm^{-3}) are the hole concentrations in the top interface of the UBO and LBO, respectively.

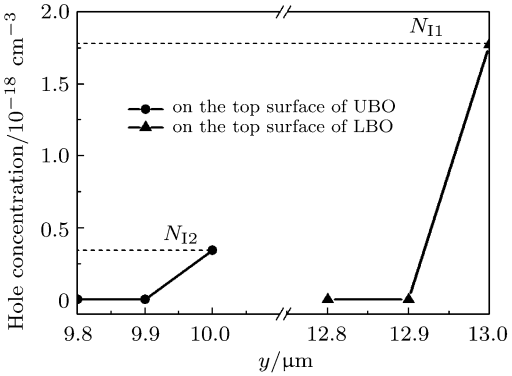


Fig. 2. Hole concentration distribution in y-direction at the drain end ($x = 79$ μm, $t_S = 10$ μm).

The breakdown voltage of the CBL SOI LDMOS can be approximately written as

$$V_b = 0.5E_S\varepsilon_S + t_{I1}E_S\varepsilon_S/\varepsilon_I + t_{I2}(E_P\varepsilon_S + qQ_{I2})/\varepsilon_I, \tag{4}$$

while the breakdown voltage of a conventional SOI LDMOS can be approximately expressed as

$$V_b = 0.5E_S\varepsilon_S + t_{ox}E_S\varepsilon_S/\varepsilon_I. \tag{5}$$

Comparing Eq. (1) with Eq. (5), we see that the breakdown voltage of the SBO CBL SOI is increased owing to the additional holes Q_{I1} and Q_{I2} on the top interfaces of the UBO and LBO, while the breakdown voltage of the CBL SOI device is enhanced just by the Q_{I2} on the UBO.

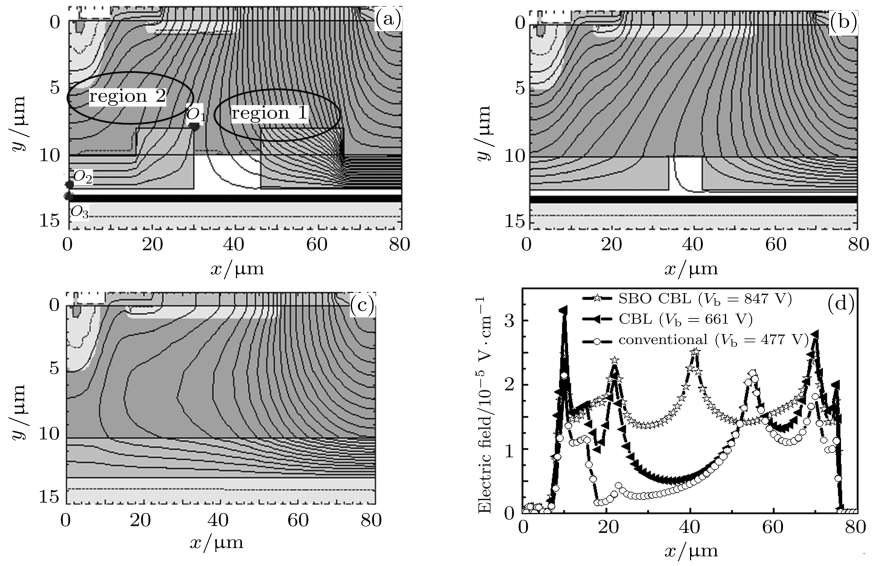


Fig. 3. Equi-potential contours and surface electric fields distributions ($y = 0.01$ μm) at breakdown for SBO CBL, CBL and conventional SOIs, respectively. ($L_d = 70$ μm, $t_S = 10$ μm, $t_{I1} = 2.5$ μm, $t_P = 0.5$ μm, $t_{I2} = 0.5$ μm, $H_{P-top} = 1$ μm, 20 V/contour). Equi-potential contours: (a) SBO CBL, (b) CBL, (c) conventional SOI; (d) surface electric field distribution for the three structures (with the optimal structure parameters, P-top and doping concentration of drift region (N_d) for each device).

Figure 3(a) shows the equi-potential contours for an SBO CBL SOI LDMOS. The equi-potential contours located in the right step oxide and region 1 are more (in Fig. 3(a)) than those of the CBL SOI LDMOS (in Fig. 3 (b)). Moreover, the equi-potential contours located in t region 2 (in Fig. 3(a)) become more than those of the conventional SOI LDMOS (in Fig. 3(c)). Therefore, the equi-potential contour distribution and the surface electric field of the SBO CBL SOI are more uniform than those of the CBL and the conventional SOI, as shown in Fig. 3(d). The potentials at O_1, O_2 and O_3 in Fig. 3(a) are almost the same and the potential at O_3 is equal to $V_{\rm I2}$. $Q_{\rm I2}$ is determined by $V_{\rm I2}$, therefore $Q_{\rm I2}$ is determined by the location of O_1. The breakdown voltages for the conventional SOI, CBL and SBO CBL SOI are 477, 661, and 847 V, respectively.

3. Results and discussion

Figure 4 shows the electric field distributions in y-direction for SBO CBL, CBL, and conventional SOI LDMOS, respectively. The field in the UBO increases to 163 V/μm from about 90 V/μm of the CBL SOI and conventional SOI. The electric displacement continuity on the top interface of the UBO is written as

$$E_{\rm I1}\varepsilon_{\rm I} = E_{\rm S}\varepsilon_{\rm S} + 0.05\times10^{-4}qN_{\rm I1}, \qquad (6)$$

where $E_{\rm S}\varepsilon_{\rm S} \approx 3.16\times10^{-7}({\rm cm}^{-2}\cdot{\rm C})$ at $V_{\rm d} = V_{\rm b}$. Therefore, $E_{\rm I}$ can increase significantly only if $N_{\rm I1} > 10^{17}$ cm^{-3}. For the SBO CBL LDMOS, the SBO prevents the extraction of holes: $N_{\rm I1} = 3.4\times10^{17}$ cm^{-3}, as illustrated in Fig. 5(a). The $E_{\rm S}$ of the SBO CBL is 30.6 V/μm, and the $E_{\rm I1}$ should be 173 V/μm according to Eq. (6). However, the $E_{\rm I1}$ of the SBO CBL is actually 163 V/μm in Fig. 4. There is only 6% error between the actual and theoretical values of $E_{\rm I1}$. The hole concentrations on the top interface of the UBO for the conventional SOI and the CBL SOI are much less than 10^{17} cm^{-3} (in Fig. 5(a), e.g. in order of magnitude 10^{14}), so both of their $E_{\rm I1}$ are just about 90 V/μm.

The electric displacement continuity on the top interface of the LBO is expressed as

$$E_{\rm I2}\varepsilon_{\rm I} = E_{\rm p}\varepsilon_{\rm S} + 0.05\times10^{-4}qN_{\rm I2}. \qquad (7)$$

The location of the black vertical dotted line is $x =$ 79 μm, as illustrated in Fig. 5(b). For the SBO CBL SOI, $E_{\rm P} = 1.05\times10^5$ V/cm, $N_{\rm I2} = 1.77\times10^{18}$ cm^{-3} at $x = 79$ μm as illustrated in Fig. 5(b). $E_{\rm I2}$ should be 442 V/μm according to Eq. (7). However, the $E_{\rm I2}$ of SBO CBL is actually 460 V/μm by simulation, as illustrated in Fig. 4. For the CBL SOI, the actual and the theoretical values of $E_{\rm I2}$ are 476 V/μm and 475 V/μm, respectively. In Fig. 5(b), the hole concentration at the source side on the bottom of the polysilicon layer is higher than that at the drain side while $E_{\rm P}$ is higher at the drain side, which maintains a constant $E_{\rm I2}$ from Eq. (7). From Fig. 5(b), it can be also seen that the hole concentration on the LBO for CBL SOI is higher than that of the SBO CBL SOI, because of the higher $E_{\rm I2}$ and lower $E_{\rm P}$ for the CBL SOI in Fig. 5(b) and Fig. 4. All of them satisfy Eqs. (6) and (7), ignoring the errors caused by simulation and calculation.

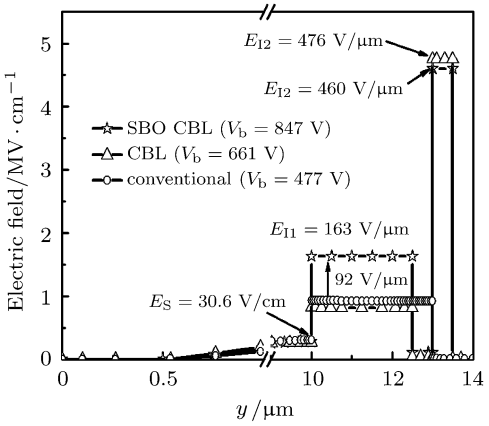


Fig. 4. Electric field distributions in y-direction at the drain end ($x = 79$ μm).

More holes (i.e. large $N_{\rm I1}$ and $Q_{\rm I1}$ values) are located at the top interface of the UBO for a higher oxide step (i.e. a large H value) in Fig. 6(a). Figure 6(b) shows the influences of H on the breakdown voltage and specific on-resistance ($R_{\rm on,sp}$). $E_{\rm I1}$, $V_{\rm I1}$ and $V_{\rm b}$ firstly increase with increasing H according to Eq. (1), as shown in Fig. 6(b). As H increases, more potential contours are located within the right step oxide and the UBO, while the voltage sustained by the SOI layer ($V_{\rm S}$) and by the LBO ($V_{\rm I2}$) decrease. Consequently, the breakdown voltage firstly increases and then decreases with increasing H in Fig. 6(b). Moreover, the current path decreases with increasing H, so $R_{\rm on,sp}$ increases steadily with increasing H in Fig. 6(b). The optimal H value is 2 μm, which is given by taking into account the trade-off between the breakdown voltage and the specific on-resistance.

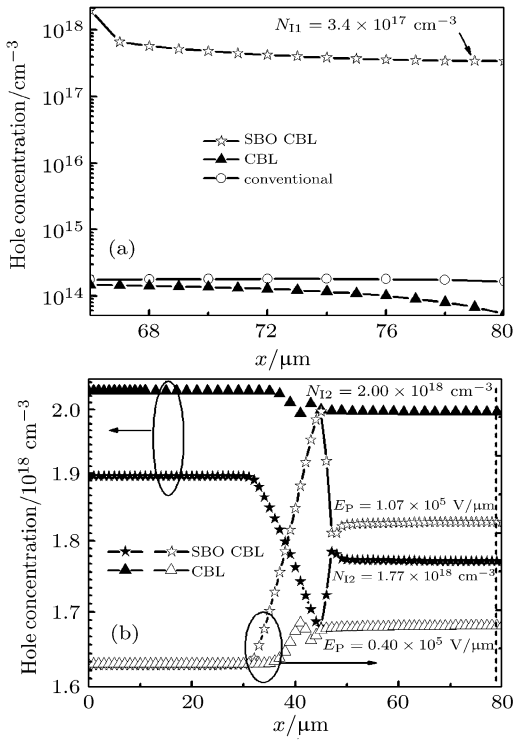


Fig. 5. Electric field and Hole concentration distributions for SBO CBL, CBL and conventional SOI in x-direction: (a) along the bottom SOI layer at the drain (AA' line in Fig. 1), (b) along the bottom of the polysilicon layer (BB' line in Fig. 1).

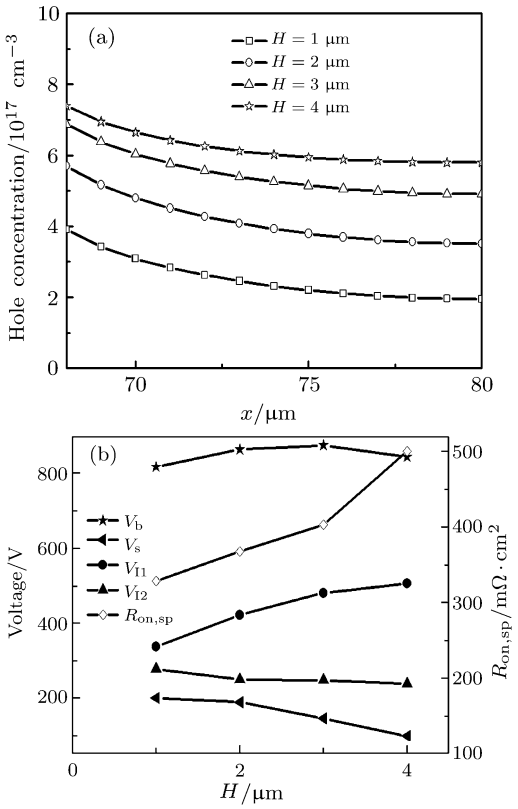


Fig. 6. (a) Hole concentration distribution for SBO CBL along the bottom SOI layer at the drain (AA' line in Fig. 1) under different H, (b) influences of H on $R_{on,sp}$ and V_b ($V_b = V_{I1} + V_{I2} + V_S$).

Figure 7 shows V_b, V_{I1}, V_{I2} and V_S against the structural parameters of L_1, L_2, L_W and L for the SBO CBL. L_3 (in Fig. 1(a)) decreases with increasing L_W, L_2 and L. The increase of L_3 leads to the increase of N_{I1} and Q_{I1}. Therefore, E_{I1} and V_{I1} increase with the increase of L_W, L_2 and L. However, V_S decreases rapidly for large L_W, L_2 and L, because the decrease of L_3 reduces the space to include potential contours for the SOI layer. The potentials at O_1 and O_3 (in Fig. 2(a)) are almost the same and the potential at O_3 is equal to V_{I2}. V_{I2} increases with O_1 moving to the drain side, and thus V_{I2} increases with increasing L. In addition, large L_W, L_2 and L values cause local high electric fields, which lead to premature breakdown. The electric fields at the points C and C' (in Fig. 1(a)) become higher with increasing L_W (in Fig. 8), which limits the breakdown voltage. In short, the breakdown voltage firstly increases and then decreases with increasing L_W, L_2 and L. However, the breakdown voltage almost keeps constant with the increase of L_1. The optimal structural parameters are $L_1 = 14$ μm, $L_2 = 20$ μm, $L_W = 16$ μm and $L = 30$ μm. It can be concluded that the location of O_1 and the length of L_3 affect the breakdown voltage significantly.

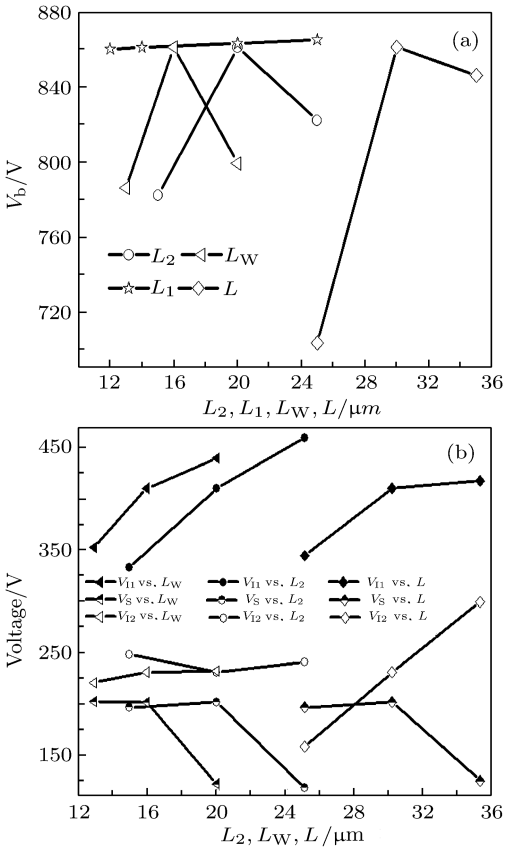


Fig. 7. (a) Dependences of V_b on L_1, L_2, L_W and L for SBO CBL, (b) influences of L_1, L_2, L_W and L on V_{I1}, V_{I2} and V_S.

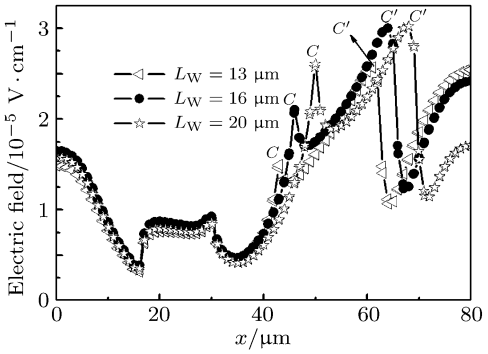


Fig. 8. Electric field distributions for SBO CBL in x-direction at different L_W.

Figure 9 shows the dependences of V_b and $R_{on,sp}$ on H_{P-top} for an SBO CBL. The optimal concentration of the P-top (N_{P-top}) and the curve effect of the P-top increase with decreasing H_{P-top}. This results in a high electric field at the point O (in Fig. 1(a)), which causes premature breakdown and thus limits the breakdown voltage. The current path increases with decreasing H_{P-top}, so $R_{on,sp}$ decreases with decreasing H_{P-top} for $H_{P-top} > 1$ μm. The curve effect of the P-top is so serious that the optimal N_d is very low at $H_{P-top} = 0.5$ μm, and thus $R_{on,sp}$ increases rapidly.

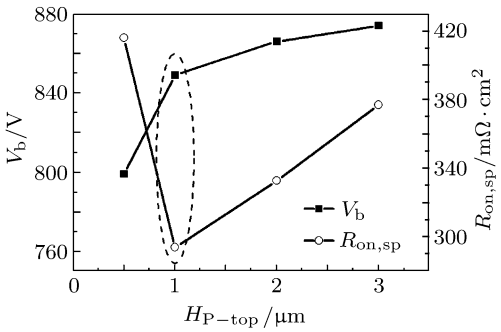


Fig. 9. Dependences of V_b and $R_{on,sp}$ on H_{P-top} for an SBO CBL.

Figure 10(a) shows the surface temperature profiles for the SBO CBL, the CBL and the conventional SOI in the on-state with applied voltage $V_d = 10$ V or $V_d = 20$ V and $V_g = 15$ V (V_g is the gate voltage). Owing to the Si windows, the surface temperatures of the CBL and the SBO CBL SOI are lower than for conventional SOIs. Figure 10(b) shows the influences of t_{I1} or the buried oxide thickness (t_{ox}) on the breakdown voltage and the maximum temperature (T_{max}). The breakdown voltage of the SBO CBL and the conventional SOI increases with increasing t_{I1} or t_{ox}, but T_{max} (at $V_d = 10$ V and $V_g = 15$ V) increases much more slowly for the SBO CBL SOI, as illustrated in Fig. 10(b). Therefore, the SBO CBL SOI is more suitable for high voltage power applications. It can be concluded that the proposed SBO CBL SOI can not only enhance the breakdown voltage but also reduce the self-heating effect.

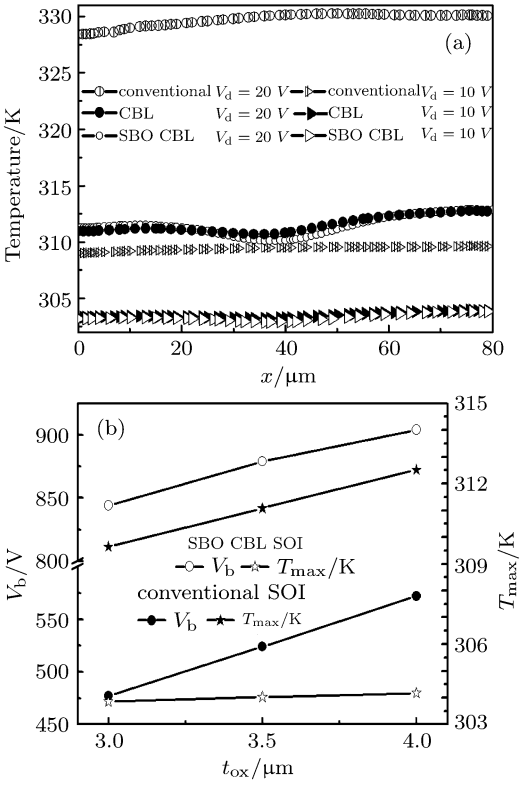


Fig. 10. Thermal characteristics: (a) surface temperature profiles, (b) T_{max} as a function of T_{ox} for CBL and SBO CBL SOI LDMOS ($t_{ox} = t_{I1} + t_{I2}$, $t_{I2} = 0.5$ μm, t_{I1} is variable, for the SBO CBL SOI).

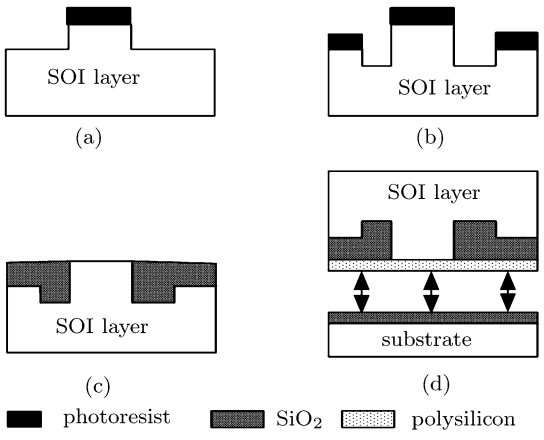


Fig. 11. Key fabrication steps of the SBO CBL SOI wafer.

Figures 11(a)–11(d) show the key fabrication steps for an SBO CBL SOI wafer: (a) etching Si to form the pattern of the UBO on the SOI layer; (b)

etching Si again to form the pattern of the SBO on the SOI layer; (c) thermally growing 0.1 μm oxide and CVD growing more than 4.5 μm SiO_2, then chemical mechanical polishing (CMP) SiO_2 to form UBO and SBO; (d) continuing to deposit polysilicon and then to 0.5 μm on the SOI layer, and thermally growing 0.5 μm oxide on the substrate Si wafer, then bonding the SOI layer and substrate together. Our team has taped out the CBL SOI, and the experimental results have been published.[1] Compared with the fabrication for CBL SOIs, only one mask for the step groove are increased (as illustrated in Fig. 11(b)), but the breakdown avoltage increases from 661 V to 847 V.

4. Conclusion

A new high-voltage device structure for SBO CBL SOI LDMOSs has been proposed. The breakdown voltage of 847 V is obtained on a 10 μm-thick SOI over a 3 μm-thick buried layer. The breakdown voltage of the SBO CBL SOI increases by 28% and 78% compared with the CBL and the conventional SOI, respectively. The maximum temperature is equal to that of the CBL SOI but 5.77 K lower than that of the conventional SOI. An SBO CBL SOI device can not only enhance the breakdown voltage but also reduce the self-heating effect.

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