Bias dependence of a deep submicron NMOSFET response to total dose irradiation

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Deep submicron n-channel metal-oxide-semiconductor field-effect transistors (NMOSFETs) with shallow trench isolation (STI) are exposed to ionizing dose radiation under different bias conditions. The total ionizing dose radiation induced subthreshold leakage current increase and the hump effect under four different irradiation bias conditions including the worst case (ON bias) for the transistors are discussed. The high electric fields at the corners are partly responsible for the subthreshold hump effect. Charge trapped in the isolation oxide, particularly at the Si/SiO_2 interface along the sidewalls of the trench oxide creates a leakage path, which becomes a dominant contributor to the off-state drain-to-source leakage current in the NMOSFET. Non-uniform charge distribution is introduced into a three-dimensional (3D) simulation. Good agreement between experimental and simulation results is demonstrated. We find that the electric field distribution along with the STI sidewall is important for the radiation effect under different bias conditions.

Keywords: bias condition, oxide trapped charge, shallow trench isolation, total ionizing dose

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1. Introduction

In modern submicron bulk complementary metal oxide semiconductor (CMOS) technologies, the radiation induced gate threshold voltage shift is not a major factor limiting the total dose hardness, since the charge trapped in the ultra thin gate oxides is very small.[1−3] For sub 0.25 μm technologies, shallow trench isolation (STI) is the only viable scheme for achieving the required packing density and the required speed performance by using tight active area pitches and improved planarity.[4] Typical STI dimensions for CMOS technologies smaller than 180 nm are in the range from 300 nm to 450 nm in depth and about 280 nm in width.[5,6] Although the gate oxide becomes thinner, the STI oxide does not scale down correspondently. As a consequence, the radiation induced charge trapping in the STI oxide still leads to macroscopic effects, such as the drain-to-source leakage current and ultimately limits the radiation tolerance of CMOS circuits.[7,8]

If an electric field exists across the oxide of a MOSFET, once generated, electrons in the conduction band and holes in the valence band will immediately begin to transport in opposite directions. Electrons are extremely mobile in the silicon oxide and are normally swept out of the silicon dioxide in picoseconds.[9,10] Holes generated in the oxide transport much slower through the lattice than electrons. As the electric field increases, the probability that a hole will recombine with an electron decreases and the fraction of un-recombined holes increases. The electric field extends into the trench region and plays a pivotal role in both the initial separation of electron–hole (e–h) pairs and the charge migration. The electric field distribution in the trench is complicated.[11] There are a few papers dealing with this subject. The non-uniform total dose induced charge distribution in STI oxide is discussed in detail,[12] however it cannot explain the hump effect caused by the total ionizing dose (TID).

The investigations of TID responses of enclosed gate devices,[13] 0.25 μm[14] and 3 μm[15] devices and the simulation of 0.18 μm[16] devices have been performed. In this paper, we fabricate samples using 0.18 μm process. Different bias conditions are used

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to investigate the total ionizing dose effect of NMOSFETs. Though the threshold voltages of the devices show negligible shift, the subthreshold leakage currents suffer a significant change. A three-dimensional (3D) simulation is introduced to understand the mechanism of radiation effects under different bias conditions.

2. Experiment details

All devices were fabricated in a 180 nm process. Shallow trench isolation is introduced for isolation and the trench oxide thickness is about 400 nm. The transistors with gate oxide of 6 nm were used for the input/output (I/O) circuit of the flash memory. Devices with channel width (W) 10 μm and channel length (L) 0.35 μm were used. All the samples were ceramics packaged. The operating voltage was 3.3 V.

Irradiations experiments were carried out at the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences using ^{60}Co γ source, typically at a dose rate of 80 rad(Si)/s. During radiation exposure, the bias conditions were consistent with the usual bias of transistors in digital circuits (Table 1). They corresponded to on-state (ON) and off-state (OFF) in inverters, transmission-gate (PASS) like access transistors in memory cells and the floating condition. The temperature was monitored and kept at room temperature. Electrical measurements were obtained prior to and after step stress irradiations up to 50 krad(Si), 80 krad(Si), 100 krad(Si), 150 krad(Si), 200 krad(Si) and 500 krad(Si). Transfer (I_{ds}–V_{gs}) characteristics were measured in ohmic region (V_{ds} = 50 mV) for all devices. These I–V curves were taken within half an hour following the exposure. All the current components from four terminals were measured and checked.

Table 1. Bias condition definition.

Type	Gate/V	Source/V	Drain/V	Substrate/V
ON	3.3	0	0	0
OFF	0	0	3.3	0
PASS	0	3.3	3.3	0
FLOAT	float	float	float	float

3. Experimental results

Figure 1 shows a series of transfer I–V curves measured on W/L = 10 μm/0.35 μm n-channel transistor irradiated in steps up to 500 krad(Si) under different bias conditions. As shown in Fig. 1, for ON bias condition and after a total dose radiation of 50 krad(Si), the subthreshold leakage current slightly increases and the subthreshold hump effects are observed. At 150 krad(Si), the leakage current curve is nearly flat. When the total ionizing dose accumulates to 500 krad(Si), the drain current at V_{gs} = 0 V is approximately 6 orders of magnitude higher than the corresponding pre-irradiation value. Positive charge trapped in the lateral STI

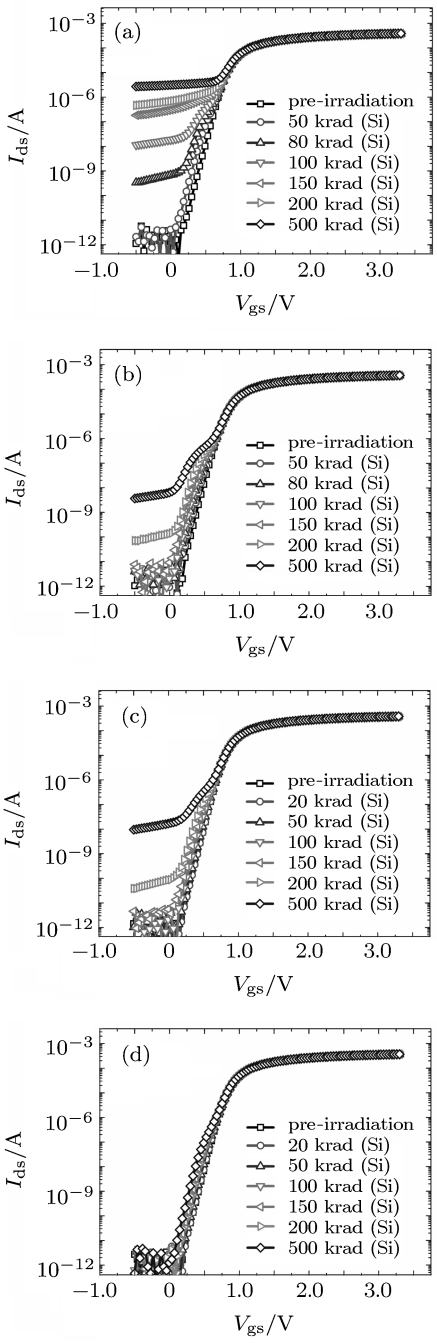


Fig. 1. Radiation response of NMOSFET (W/L = 10 μm/0.35 μm) under different bias conditions: (a) ON, (b) OFF, (c) PASS and (d) FLOAT. The drain-source voltage V_{ds} = 0.05 V.

oxide forms a conductive channel, through which leakage current can flow between the source and the drain and the parasitic lateral transistor turns on. The hump disappears gradually as the leakage current of the parasitic transistor increases. The degradation of the input/output device after the ionizing irradiation will lead to large leakage current and incorrect output voltage. For OFF and PASS bias conditions, as shown in Fig. 1, the radiation induced leakage current is insignificant. The off-state leakage current is 10^{-10} A until the radiation dose reaches 200 krad(Si). At a lower total dose, each of them has a subthreshold hump. That is to say, the total ionizing effect of the device under PASS bias condition is comparable to that under OFF bias condition. For FLOAT bias condition, only hump effect is observed, there is no off-state leakage current that increases with the radiation dose. We extract the off-state leakage current corresponding to $V_{\rm gs} = 0$ V and the response to the total dose under four different biases. The results are shown in Fig. 2. It is clear that the largest leakage current degradation occurs under ON bias condition. The OFF bias condition has a similar effect to that of the PASS bias condition up to 500 krad(Si).

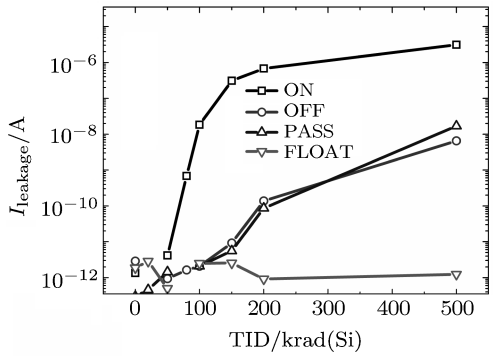


Fig. 2. Off-state leakage current each as a function of total dose under different bias conditions.

4. Discussion

4.1. High electric field region of STI corner

As is well known, high electric fields presented in trench corner regions reduce the gate oxide integrity and cause anomalous humps in the subthreshold I–V characteristics of non-irradiated devices with STI.[17] This problem turns serious if the trench isolation is recessed below the trench corner, where the gate oxide becomes thinner as it wraps around the corner.

At a low dose, the high electric fields at the corners of the STI are partly responsible for the increased transistor leakage current.[18] The trench insulator is recessed for our device. The peak electric fields at the trench corners are further enhanced. Subthreshold hump effects are observed for ON, OFF, PASS bias conditions. Under FLOAT bias condition, although there is no electric field, there are a large number of oxygen vacancies close to the silicon/oxide interface due to the out diffusion of oxygen near the oxide and the lattice mismatch at the surface. These oxygen vacancies can act as trapping centres. During γ ray irradiation, a few generated holes can approach the interface. Some fraction of the holes will be trapped there.

4.2. Parasitic transistor threshold voltage shift

As shown in Fig. 1, at a high dose level, the leakage current becomes more flat, which means that the parasitic transistors play an important role for the leakage current. Figure 3 shows the drain-to-source leakage current versus the gate–source voltage for an n-channel main transistor with (combined curve) and without the field-oxide leakage and for a parasitic field oxide transistor.[19] Because of the large thickness of the shallow trench isolation oxide, the pre-irradiation threshold voltage of the parasitic field oxide transistor is relatively large and it can cause a very large negative threshold-voltage shift, as positive radiation-induced charge builds up in the field oxide. If the threshold voltage shift of the parasitic field oxide transistor is large enough, it will cause an off-state leakage current, which can significantly change the drain-to-source current of the main transistor.

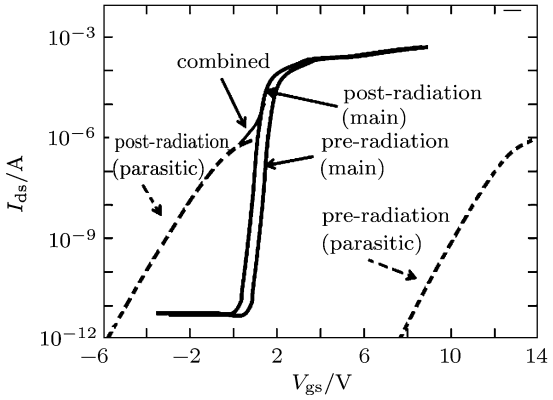


Fig. 3. The I–V curves for a main transistor and a parasitic transistor pre- and post- irradiation.

4.3. 3D simulation

To gain an understanding of the experimental results in Figs. 1 and 2, a 3D simulation is introduced. Since the radiation induced charge in the thin gate oxide is much smaller than that in the STI, interface charge is neglected for the gate oxide/substrate silicon. The post-irradiation simulations are performed by placing sheet charge with non-uniform distribution at the trench sidewall interface. Cross section through the centre of the channel is shown in Fig. 4, in which the STI corner is especially indicated. The trench is 400 nm deep and the doping level of the p well is obtained by using a process simulation. The gate oxide is 6 nm. The models used include the conventional drift diffusion model for transport and the Shockley–Read–Hall (SRH) model for generation recombination. The parallel electric field dependence (FLDMOB) is required to model the velocity saturation effect.

As shown in Fig. 4, the arrow direction (d) is along the STI sidewall towards the substrate. The simulation of $I_{\rm ds}$–$V_{\rm gs}$ curve is calibrated by the pre-irradiation. The simulation results for different bias conditions are shown in Fig. 5. Good agreement between experimental and simulation results is demonstrated. In our study, the non-uniform charge distribution is used along with the STI sidewall. The charge density is shown in Table 2. In general, Table 2 indicates that (1) charge increases with the TID, while the scenario is different in detail for different bias conditions; (2) at low dose, charge trapped in the top 20 nm of the STI sidewall induces the hump effect; (3) at high dose, large off-state leakage current is caused by charge trapped in the deeper STI oxide; (4) ON bias is the worst bias condition, OFF and PASS biases have a similar radiation effect up to 500 krad(Si) and FLOAT bias only exhibits the hump effect.

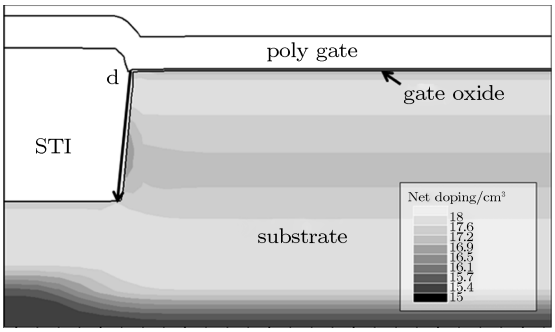


Fig. 4. Cross section of the simulation model.

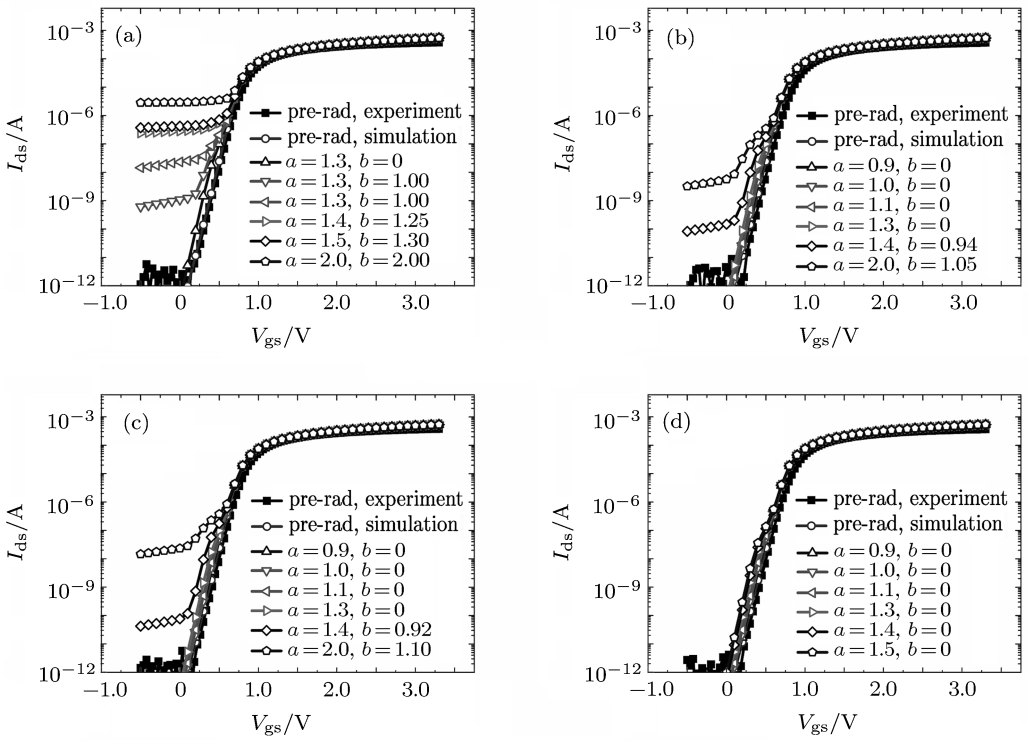


Fig. 5. The $I_{\rm ds}$–$V_{\rm gs}$ characteristics for TID simulated with the 3D model under different bias conditions: (a) ON, (b) OFF, (c) PASS and (d) FLOAT. The drain–source voltage $V_{\rm ds}$ = 0.05 V, W/L = 10 μm/0.35 μm. The a and b denote charge densities along the STI sidewall in units of $10^{12}\cdot$ cm^{-2} for top 20 nm and for 20 nm to 400 nm, respectively.

Table 2. Non-uniform charge distribution in simulation. The a and b denote charge densities along the STI sidewall in units of $10^{12}\cdot$ cm^{-2} for top 20 nm and for 20 nm to 400 nm, respectively.

TID/krad(Si)	ON		OFF		PASS		FLOAT	
	a	b	a	b	a	b	a	b
0	0	0	0	0	0	0	0	0
20	–	–	0.9	0	0.9	0	0.9	0
50	1.3	0	1	0	1	0	1	0
80	1.3	1	–	–	–	–	–	–
100	1.3	1.1	1.1	0	1.1	0	1.1	0
150	1.4	1.25	1.3	0	1.3	0	1.3	0
200	1.5	1.3	1.4	0.94	1.4	0.92	1.4	0
500	2	2	2	1.05	2	1.1	1.5	0

The electric field extending into the trench region is important for the separation of electron–hole pairs and the charge migration. Three processes are involved, i.e., (1) charge yield, which is the fraction of the electron–hole pairs that do not immediately recombine; (2) charge transport by drift and diffusion; and (3) hole trapping at the interface between the STI and the substrate silicon.[11] As shown in Fig. 4, the arrow along the STI sidewall is 5 nm away from the oxide/silicon interface. The electric field distributions in the centre of the channel along the STI sidewall for different bias conditions are shown in Fig. 6(a). For ON bias condition, the electric field near the STI corner is larger than that for PASS/OFF bias condition, which is 2.5×10^6 V/cm. The fraction of unrecombined holes is 90%,[20] and the charge yield is relatively high. As shown in the figure, the electric field for OFF bias condition nearly equals that for PASS bias condition. Electric fields under 100 nm of the STI along the length direction of the device for ON, OFF, PASS bias conditions are shown in Fig. 6(b). The minimum and the maximum electric fields for PASS and OFF bias conditions are equal and smaller than that for ON bias condition.

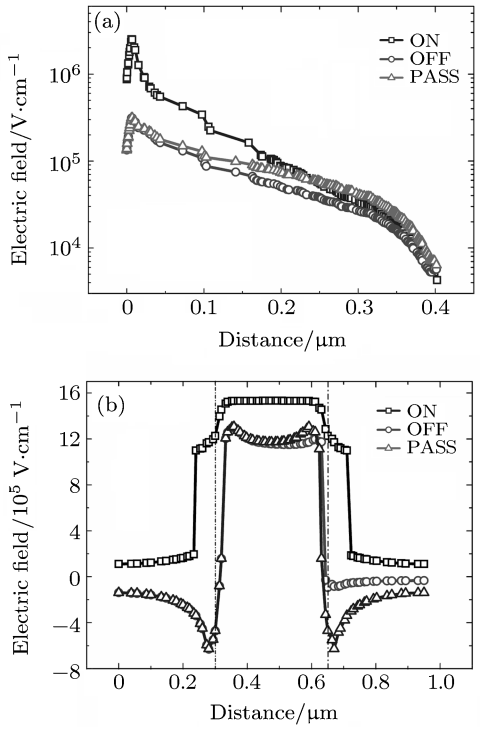


Fig. 6. (a) Electric fields in the centre of the channel along STI sidewall for ON, OFF, PASS bias conditions. (b) Electric fields under 100 nm of the STI along the device's length for ON, OFF, PASS bias conditions.

5. Conclusion

We show that the worst total dose radiation response of I/O transistor occurs under the ON bias condition. We also show that under PASS and OFF bias conditions the radiation effects are similar up to 500 krad(Si). The total ionizing dose effect of I/O transistor is attributed to the high electric field of the recessed STI corner and the threshold voltage shift of the parasitic STI transistors. Degradation of the I/O transistor after ionizing radiation will lead to large leakage current and large power consumption. The electric field distribution along the STI sidewall influences the trapped charge in the STI oxide, which induces a leakage current path. The simulation results, which are consistent well with the experimental results, show the mechanism of the bias dependence of the total dose effect. The non-uniform charge distribution is a simple and effective method for analysing radiation response.

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