First principles simulation technique for characterizing single event effects

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This paper develops a new simulation technique to characterize single event effects on semiconductor devices. The technique used to calculate the single event effects is developed according to the physical interaction mechanism of a single event effect. An application of the first principles simulation technique is performed to predict the ground-test single event upset effect on field-programmable gate arrays based on 0.25 μm advanced complementary metal–oxide–semiconductor technology. The agreement between the single event upset cross section accessed from a broad-beam heavy ion experiment and simulation shows that the simulation technique could be used to characterize the single event effects induced by heavy ions on a semiconductor device.

Keywords: single event effect, static random access memory, cross section, simulation

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1. Introduction

Space radiation effects are among the greatest environmental threats to the safety of manned and robotic missions. Radiation effects in electronics range from loss of data to catastrophic failure. Effects caused by the passage of a single energetic particle (such as a proton, neutron or heavy ion) through a sensitive device are one of the most serious problems.[1] The phenomena are collectively described as single event effects (SEEs). Ground-based particle testing for SEEs is often used to study the physical mechanisms contributing to SEE, estimate on-orbit error rates and qualify parts for use in space-based systems.[2−4]

The energy of heavy ions in an actual space environment could reach hundreds of GeV/u. Unfortunately, most facilities used for such an SEE testing provide particles with energy on the order of tens of MeV/u.[5] Increasing computer power and using new numerical methods now make it possible to routinely deploy exact radiation effect numerical simulation. Moreover, the numerical simulation could be performed in the initial design phase of integrated circuit (IC) to improve the radiation hardening method.[6]

The rectangular parallelepiped (RPP) model used to evaluate for SEEs has been asserted to be inadequate for the advanced IC, because the current semiconductor devices has been scaled so that the basic simplifying assumptions for the RPP model are no longer suitable.[7,8] A new simulation technique is developed to characterize the SEEs on a semiconductor device in this work.

2. The concept of the first principles simulation

The physical process of SEEs on a semiconductor device can be divided into two steps. Firstly, the particle interacts with the semiconductor device and deposits electron–hole pairs within the device. Secondly, the charge carriers transport in the device and induces the device response.[9] The particle can cause digital logic upset (single event upset, SEU), latch-up (single event latch-up, SEL), and so on.

The first segment is corresponds to the simulation of particle transport in semiconductor. The calculation in this segment is accomplished using Geant 4, which is a library of C++ routines for describing radiation interaction with matter.[10] The metal on the top of a semiconductor device could have a

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strong influence on the deposited energy in sensitive regions.[11−13]

The second segment corresponds to the simulation of the physical device to calculate the device response to a radiation event. DESSIS from ISE and Sentaurous from Synopsys are both applicable technology of computer-aided-design (TCAD) tools for this work.[8] A three-dimensional TCAD full-structure will be made in order to calculate the electrical response.

The simulation technique integrates the Geant 4 and TCAD tools according to the SEE physical mechanism, so it is called the first principles simulation technique.[14] In the next two sections, the application of the first principles simulation technique to predict the ground-test SEU response of a 0.25-μm process technology is presented with the analysis of the SEU.

3. FPGA memory cell modeling simulation

The simulation and experiment object is the field-programmable gate arrays (FPGA) XCV300PQ240 produced by Xilinx. It is manufactured by 0.25-μm complementary metal–oxide–semiconductor (MOS) technology. The usual static SEU testing on the FPGA is to determine the cross section of upsets on the configurable logic blocks (CLBs), which provides functional elements for combinatorial or synchronous logic.[15] Values stored in the static memory cells control CLBs. So the characterization of single event upsets in the CLBs could be achieved from the simulation of the static memory cell. This paper demonstrates the simulation technique by applying it to characterize the static SEU on the FPGA in the next several subsections.

3.1. Material structure

There always is a worry about the influence of a device's multi-layer metal structure on the effective linear energy transfer (LET).[12,16] Heavy ions can lose much more energy when penetrating into the multi-layer metal structure than into the semiconductor materials.[17] So the top layers may change the heavy ion's penetration depth and LET considerably. The key is that at different positions on the semiconductor material structure the longitudinal materials are not uniform (e.g., tungsten, a structure used to connect different layers of metal in a multi-layer interconnect system, only fills the contact hole), so it is impossible to correct the influence of multi-layer metal structures using a simple parameter event for normal heavy ion strike.

Recently, the nuclear interaction between heavy ions and semiconductor materials has attracted much attention.[18] This nuclear interaction mechanism was proposed to explain the phenomenon that the particles with the same LET but different energy could induce different cross sections of SEU and SEL.[2,19] Dodd's research suggested that secondary particles produced by nuclear interactions play a role in determining the SEU and SEL hardness of integrated circuits, especially at a low LET.[19] The high-Z material would have greater cross section of nuclear reaction with heavy ions than a low-Z material (e.g., silicon). High-Z material may lead to extreme charge collection events through nuclear reactions.

Therefore, it is necessary to calibrate the quasi-device structure especially for the advanced integrated circuits with five or more layers of metal on the top. The thickness of over layers of the FPGA could be tens of micrometers, which includes the silicon-nitride layer, aluminum, tungsten layers, and so on. The heavy ions which strike the semiconductor device must penetrate the top layers before reaching the sensitive silicon regions.

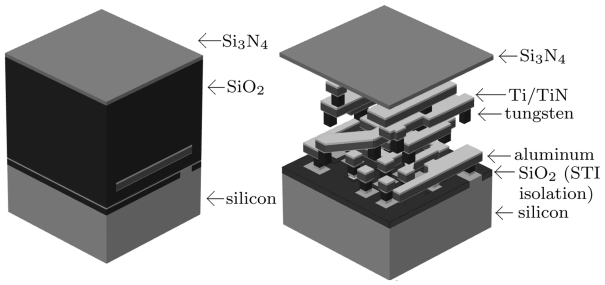


Fig. 1. The memory cell structure calibrated using TCAD. The left figure is the exterior view, the right one shows the metal layers on top of the silicon material.

Figure 1 shows the FPGA memory cell structure calibrated using TCAD. The cell structure is defined from the TCAD layout and technology process steps achieved from the device producer. The top material in the simulations is consistent with the over layers used to fabricate the SRAM cell. The left is the exterior view of the cell structure and the right is the multi-layer interconnect systems. The device has five aluminum layers, which are fixed by the semiconductor technology. The right figure shows that high-Z metals such as tungsten and titanium have an important role in the multi-layer top structure. The influence on the energy of the heavy ion energy can not be ignored.

The material structure of the SRAM cell fabrication utilizing TCAD process tools is the first stage of the first principles simulation. The structure is meshed into a suitable and computer-saving grid for semiconductor device simulation using the ISE-TCAD mesh tool. The meshed material structure is be translated into the Geant 4 program to calculate the transport of heavy ions within the device.

3.2. Geant 4 calculation

The transport of heavy ions within the device is accomplished using the Geant 4 program. The transport calculation has advantages over traditional Monte Carlo calculations.[20−22] Figure 2 shows the device structure in Geant 4 translated from the TCAD process tool.

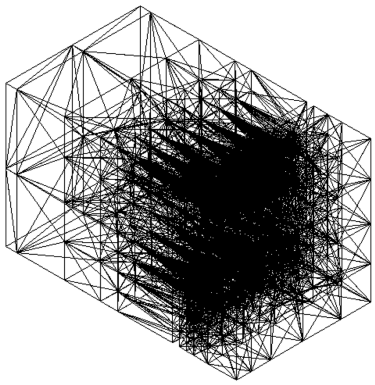


Fig. 2. The device structure in Geant 4 translated from the TCAD process tool.

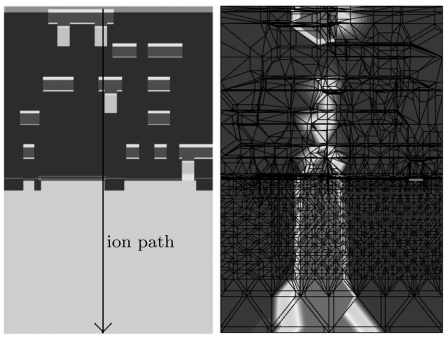


Fig. 3. The distribution of free charge by the 140-MeV ^{35}Cl in the memory cell. (a) The diagram of the pass of ^{35}Cl in the device model; (b) the charge distribution calculated using the first principles simulation technique.

The structure of the initial free charge deposited by heavy ions is a necessary condition for semiconductor simulations.[18,23,24] Figure 3 shows the distribution of free charge by the 140-MeV ^{35}Cl in the memory cell.

The scalar values of the charge deposited by the particle are appended to the vertex of the meshed device structure. The union of the charge distribution and the meshed device structure is a necessary condition in the next device simulation. This approach can reduce the error induced by the analytical radial distribution (such as Gaussian distribution) of the free charge.

3.3. Device modeling

Figure 4 shows the three-dimensional (3D) device model of the memory cell, including the accordant doping concentration with the actual device.

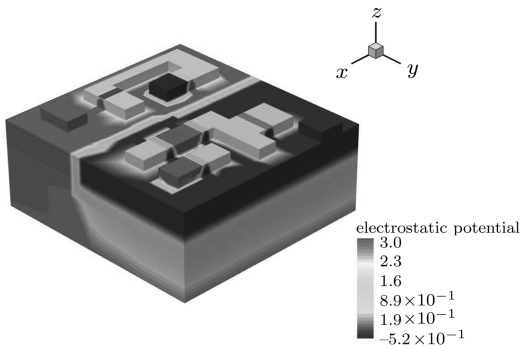


Fig. 4. The doping diagram in a 3D model of the memory cell.

The validity of the basic physical models is the basis of accurate device simulation. In addition to standard drift-diffusion laws, other physical models (such as concentration and field-dependent mobility, velocity saturation of carriers, concentration dependent Shockley-Read-Hall and Auger recombination, band-gap narrowing model, and so on) must be considered. To verify the 3D memory cell model, it is necessary to compare the electrical characterization of the device model with that of the compact Spice model offered by the device producer.

The memory cell is composed of two cross-coupled inverter pairs, as shown in Fig. 5. When an energetic particle strikes the sensitive location on the memory cell (typically the reverse-biased drain junction of a transistor biased in the "off" state,[25]) charge collected by the junction results in a transient current in the struck transistor. Whether an observable SEU occurs depends on which one is faster: the feedback of the voltage transient through the opposite inverter, or recovery of the struck node voltage through the restoring transistor, as shown in Fig. 5.[26] So the verification of the device model is divided into two parts: the recovery time verification and the feedback time.

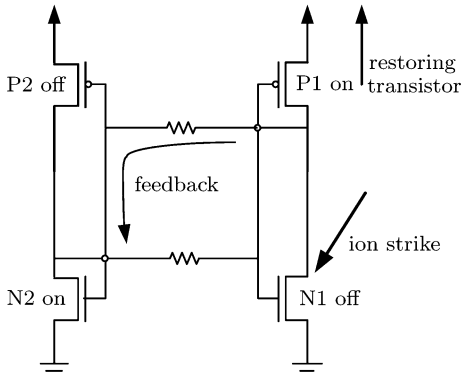


Fig. 5. Comparison between the feedback process and the recovery process governs the SEU response of the memory cells.

3.3.1. The verification of the recovery time

The recovery time depends largely on the restoring transistor current drive and the lifetime of the minority carrier in the semiconductor substrate.[27] The drive current of the restoring transistor is a critical criterion for checking the recovery time of the device model. The transfer curves in Fig. 6 show a good agreement between the vendor's Spice model and the 3D model of the memory cell.

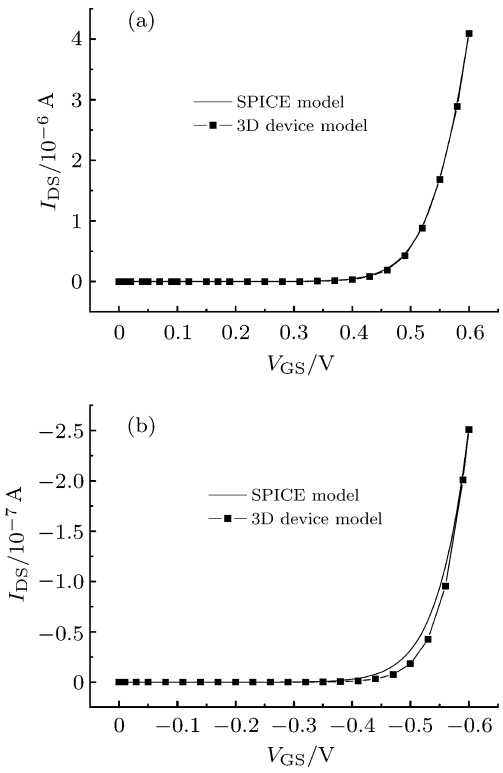


Fig. 6. Comparison between the transfer curves of the 3D device model and the Spice model. Panel (a) is the N-type MOS field-effect transistor (NMOSFET), and panel (b) is the P-type MOS field-effect transistor (PMOSFET).

3.3.2. Verification of the feedback time

The feedback time of the memory cell is defined as the time required for the disturbed node voltage to propagate through the cross-coupled inverter.[27] When a piecewise linear (PWL) signal is forced on the stroked node, the response of the gate voltage of the stroked transistor represents the feedback time. Figure 7 shows the response of the gate voltage of the stroked transistor. The consistence between the feedback time of compact Spice model and 3D device model, as shown in Fig. 7, illustrates that the device model is suitable for characterizing SEU on the memory cell.

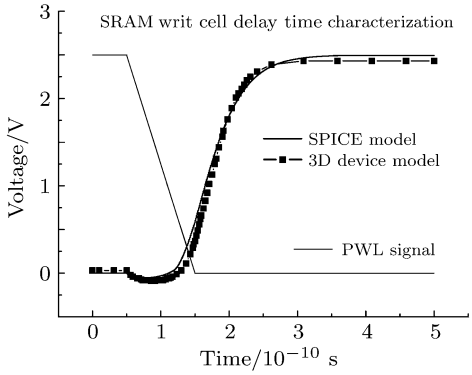


Fig. 7. Comparison between the responses of the gate voltage of the stroked transistor when a PWL signal is forced onto the stroked node.

The first principles simulation technique unites Geant 4 and TCAD tools. The next section is the analysis of the simulation result and an experiment for the characterizing single event effect induced by a heavy ion.

4. Analysis of simulation and experimental results

The static single event effects of the XCV300PQ240 FPGA were tested on the tandem accelerator at Beijing, China. The cross section of SEU on CLB was measured using the measurement system for radiation effects developed by the Northwest Institute of Nuclear Techniques, China.

Heavy ions struck the FPGA device at normal incidence. The upset error on CLB was limited up to 2% (and usually much lower) of the memory array size to reduce the probability of upset more than once at the same cell during one irradiation cycle. The power supply and function of the device on test were monitored. Once the abnormality of the power supply and

function happens, the measurement system reboots. If the power supply current exceeds a predetermined value (usually just above the dynamic current), one SEL was counted.

The SEU simulation was performed by sweeping particles at normal incidence over the memory cell. The several heavy ions used in the SEU accelerator experiment are shown in Table 1.

Table 1. Heavy ions used in the heavy ion experiment.

Species	^{12}C	^{19}F	^{35}Cl	^{48}Ti	^{63}Cu	^{79}Br
Energy/(MeV/u)	80	110	140	170	190	210

Figure 8 shows the layout of the memory cell. "N+doping" in the figure indicates the source and drain regions of the NMOSFET. "P+doping" indicates the source and drain regions of the PMOSFET. Figure 9 shows the SEU sensitive area of the memory cell achieved from the numerical simulation. Figure 9(a) shows the SEU sensitive area induced by ^{19}F. Figure 9(b) shows the SEU sensitive area induced by ^{35}Cl. The area and location of the SEU sensitive are the function of heavy ion species and energy. The sensitive region for the ^{19}F is the reverse-biased PMOSFET drain. The sensitive area for the ^{35}Cl around the PMOSFET drain is larger than that for the ^{19}F.

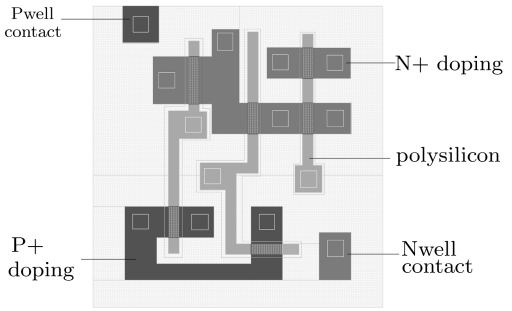


Fig. 8. The layout of the memory cell.

It is obvious that the ^{19}F with a linear energy transfer (LET) of MeV $\cdot$ mg/cm^2 deposits less energy in the memory cell than the ^{35}Cl with the LET of 13.6 MeV $\cdot$ mg/cm^2. The SEU images shown in Fig. 9 could be used for the quantitative analysis of the influence of layout, material and technology of the semiconductor device on SEEs.[28] So the first principles simulation technique can be used to analyse SEEs and to design SEE hardened devices.

The broad beam heavy ion irradiation experiment has been explored to characterize the SEEs on the XCV300PQ240 FPGA. The SEU cross section of the CLB has been achieved. Figure 10 shows the upset cross sections of the FPGA CLB achieved from heavy ion irradiation experiment and the first principles simulation.

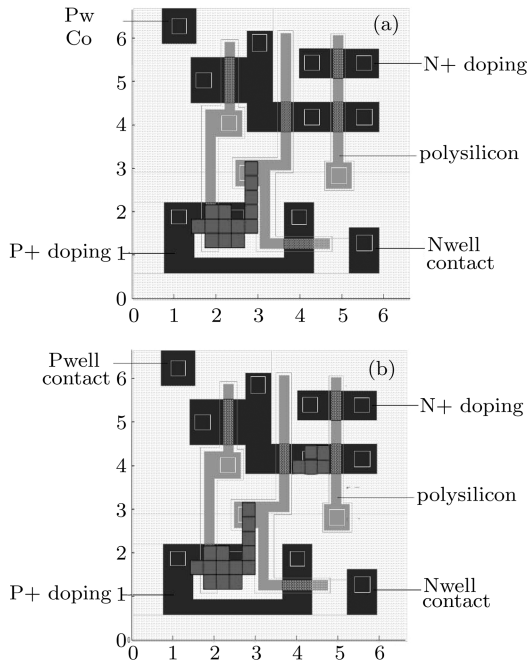


Fig. 9. The single event upset sensitive region (the grey) of the memory cell. Panel (a) is SEU sensitive region induced by ^{19}F. Panel (b) is SEU sensitive region induced by ^{35}Cl.

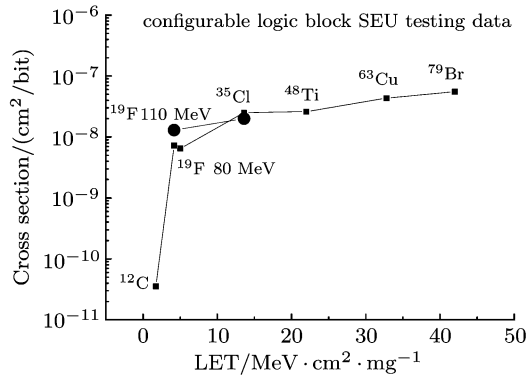


Fig. 10. The SEU cross sections of the FPGA CLB achieved from heavy ion irradiation experiment and the first principles simulation. The circle points are upset cross sections induced by 110-MeV ^{19}F and ^{35}Cl, which were achieved from the first principles simulation. The square ones were achieved from the heavy ion irradiation experiment.

The SEU cross section of the memory cell induced by 110-MeV ^{19}F is 1.5×10^{-8} cm^2 in the numerical simulation and 7.7×10^{-9} cm^2 in heavy ion irradiation experiment. The difference is much larger than that of ^{35}Cl. It is a universal problem in SEE de-

vice physical simulations.[17] The uncertainty generated by the Geant 4 tools, TCAD tools and the physical model cause deviations in the simulation results. The SEU cross section of the memory cell induced by ^{35}Cl is 2.0×10^{-8} cm^2 in the numerical simulation and 2.5×10^{-8} cm^2 in heavy ion irradiation experiment. Provided that the measurement uncertainty is in the broad-beam irradiation experiment, the difference within 20% between the two data is acceptable. It proves that the first principles simulation technique is feasible in characterizing SEU on memory-based digital system such as FPGA.

5. Conclusion

This paper developed a first principles simulation technique to characterize SEE. The technique utilizes the Geant 4 tools and TCAD tools to calculate the SEEs according to the actual physical mechanism. The first principles simulation technique is demonstrated by applying it to predict the SEU on an advanced FPGA. The SEU results achieved from the numerical simulation compared with that from heavy ion experiment prove that the first principles simulation technique can be used to characterize SEU induced by heavy ions on a memory-based digital system.

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