An interconnecting bus power optimization method combining interconnect wire spacing with wire ordering*

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On-chip interconnect buses consume tens of percents of dynamic power in a nanometer scale integrated circuit and they will consume more power with the rapid scaling down of technology size and continuously rising clock frequency, therefore it is meaningful to lower the interconnecting bus power in design. In this paper, a simple yet accurate interconnect parasitic capacitance model is presented first and then, based on this model, a novel interconnecting bus optimization method is proposed. Wire spacing is a process for spacing wires for minimum dynamic power, while wire ordering is a process that searches for wire orders that maximally enhance it. The method, i.e., combining wire spacing with wire ordering, focuses on bus dynamic power optimization with a consideration of bus performance requirements. The optimization method is verified based on various nanometer technology parameters, showing that with 50% slack of routing space, 25.71% and 32.65% of power can be saved on average by the proposed optimization method for a global bus and an intermediate bus, respectively, under a 65-nm technology node, compared with 21.78% and 27.68% of power saved on average by uniform spacing technology. The proposed method is especially suitable for computer-aided design of nanometer scale on-chip buses.

Keywords: interconnect bus, dynamic power, wire ordering, wire spacing, nanometer scale process

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1. Introduction

With the rapid scaling down of complementary metal–oxide semiconductor (CMOS) devices and the continuous rise in very large scale integrated (VLSI) circuit working frequencies, more and more functionality modules are integrated on a chip. This leads to the requirement for better communication between subsystems and implies an increase in the use of interconnect buses. Therefore, the on-chip interconnect bus is becoming a bottleneck in the sense of chip performance and power consumption. It has been reported that up to 50% of overall dynamic power consumption can be consumed by interconnects.[1] The reason for this phenomenon is that the total capacitance C in the switching energy of a net $E = \alpha C V_{\rm DD}^2$ is dominated by interconnect capacitance.[2] What is more, with devices scaling down in size, the interconnects become closer and crosstalk capacitance becomes larger, thereby causing this situation to be increasingly serious. Thus the development of nanometer scale integrated circuits will be seriously restricted unless interconnect power can be lowered effectively.

In order to meet the requirements for performance and power caused by rising clock frequency and increasing complexity, many methods, such as optimal repeater insertion (ORI),[3] wire spacing and sizing,[4] low-swing circuit,[5,6] and bus encoding,[7,8] have been proposed. A small delay penalty will save a considerable amount of power. Based on the distributed RLC interconnect model, Zhu *et al.*[3] proposed a method to calculate the repeater size and the interconnect length by which the sum of the power dissipation and the repeater area can be saved while the target delay constraint is satisfied. Using a specified figure of merit (FOM) function, a new method was proposed by Tang and Mao[4] for determining the optimal wire sizing of buffered global interconnects. They also in-

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vestigated the influence of wire width and space on performance. Considering Vdd and Vth in optimization, Chang *et al.*[5] presented an analytical repeater insertion method to optimize the power consumption under the delay constraint for a single net. Being different from the method of repeater insertion, an irredundant bus encoding scheme for on-chip buses was proposed by Wang Feng *et al.*[7] to tackle the thermal issue arising from on-chip interconnects. Using the characteristic of values transmitted over the data bus, an encoding scheme called the FV encoding scheme was developed.[8] Zuber *et al.*[9] developed a new quasilinear algorithm for solving the coupling power optimal wire spacing problem and, later, according to non-uniform wire spacing, they[2] proposed a routing optimization method for low interconnect dynamic power. In addition, optimal ordering was proposed by Zuber *et al.*[10] to enhance the effect of power optimal wire spacing. Recently a method of designing quasi-resonant interconnect networks was described by Rosenfeld and Friedman[11] for low power on-chip interconnects.

Combining wire spacing with wire ordering, in this paper we present an optimization method for low power on-chip interconnect buses. A simple yet accurate interconnect parasitic capacitance model is presented first and then according to this model we propose an interconnect bus dynamic power model. Later, the statistical characteristic of data transmitted on interconnect buses is presented and the optimal wire ordering is verified using this statistical characteristic. Finally, a novel interconnect bus power optimization method is developed and verified.

2. Interconnect bus capacitance model and power model

Consider an interconnect bus consisting of n parallel interconnects buffered by repeaters, as shown in Fig. 1. Inverters are used to maintain performance requirements such as time delay, signal slew rate, etc. At the same time, ground lines are used to weaken the effect of crosstalk between adjacent wires. Wire i denotes the i-th wire in the layout and wire 0 and wire $(n+1)$ denote two shielding lines, e.g., ground lines. Bits can be transmitted through any wire and different transmission orders will lead to different bus powers. The process to find the optimal order is called wire ordering and the process to find the optimal space is called wire spacing.

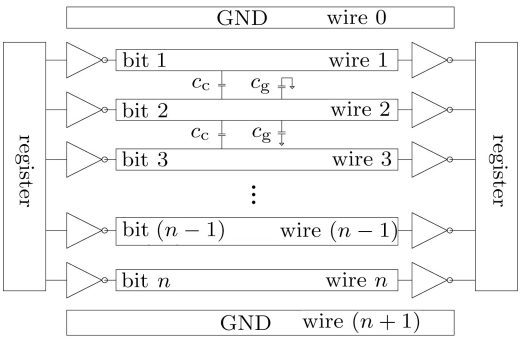


Fig. 1. Buffered interconnect bus structure.

2.1. Interconnect bus capacitance model

Dynamic power is induced by charging and discharging the capacitor and dominates the total chip power. A simple yet accurate capacitance model is needed in order to build an accurate dynamic power model of an acceptable computational complexity. Taking the BPTM (Berkeley Predictive Technology Model)[12] parasitic capacitance model as reference, an interconnect bus capacitance model satisfying these requirements is presented in this section.

In a nanometer scale integrated circuit (IC), the typical wire width and wire space both are on the order of 0.1 μm and the ratio of wire height to wire width is about $2 \sim 3$. Fringing capacitance is becoming more and more significant in nanometer CMOS process technology. Referring to the metrics of the CMOS parasitic capacitance in the BPTM[12] and considering fringing capacitance, the capacitance can be expressed as

$$c_{\mathrm{g}} = \varepsilon\Big[\frac{w}{t_{\mathrm{ins}}} + 2.22\Big(\frac{s}{s+0.70t_{\mathrm{ins}}}\Big)^{3.19} + 1.17\Big(\frac{s}{s+1.51t_{\mathrm{ins}}}\Big)^{0.76}\Big(\frac{t_{\mathrm{m}}}{t_{\mathrm{m}}+4.53t_{\mathrm{ins}}}\Big)^{0.12}\Big], \tag{1}$$

where c_{g} is the self-capacitance per unit length, s denotes the space between adjacent wires, t_{m} is the interconnect thickness, t_{ins} and ε are the thickness and the dielectric constant of the dielectric material. The first part in the bracket denotes the parallel plate capacitance to the metal layer and the last two parts refer to the fringing capacitance of the interconnect. The coupling capacitance is also significant and it can

be written as[12]

$$c_{\rm c} = \varepsilon \cdot \Big[1.44\frac{t_{\rm m}}{s}\Big(\frac{t_{\rm ins}}{t_{\rm ins}+2.06s}\Big)^{0.09} + 0.74\Big(\frac{w}{w+1.59s}\Big)^{1.14} + 1.16\Big(\frac{w}{w+1.87s}\Big)^{0.16}\Big(\frac{t_{\rm ins}}{t_{\rm ins}+0.98s}\Big)^{1.18}\Big], \quad (2)$$

where $c_{\rm c}$ denotes the coupling capacitance per unit length. Due to the existence of coupling capacitance, the conditions of timing and signal integrality are greatly worsened in nanometer scale integrated circuits.

The capacitance model represented by analytical expressions (1) and (2) holds in high accuracy, however its computation is time consuming due to its complex form, therefore it is not suitable for our optimization model. Taking the capacitance model represented by analytical expressions (1) and (2) as a standard, combining the data fitting technique, in this section we present a simplified model expressed as follows:

$$c_{\rm g} = \varepsilon\left(p_0 \cdot w + p_1 \cdot s^3 + p_2 \cdot s^2 + p_3 \cdot s + p_4\right), \quad (3)$$

$$c_{\rm c} = \varepsilon\left(q_0 + q_1 \cdot w + q_2/s\right), \quad (4)$$

where $p_0 = 1/t_{\rm ins}$, and coefficients p_1, p_2, p_3, p_4, q_0, q_1, and q_2 are all constants for a specified technology and can be easily obtained using the data fitting technique.

Adopting the capacitance models provided by BPTM and provided by this paper, the values of capacitances of global interconnect and intermediate interconnect versus normalized wire space under 90-nm CMOS technology are shown respectively in Fig. 2 and Fig. 3, where wire space has been normalized to typical wire space and wire capacitance has been normalized to the self-capacitance of an interconnect of typical width and space. One can see that $cg_{\rm model}$ and $cc_{\rm model}$ (represent model expressed as Eqs. (3) and (4)) fit cg and cc (represent model expressed as Eqs. (1) and (2)) well, which indicates a high accuracy of Eqs. (3) and (4). Obviously self-capacitance is approximately proportional to wire width, and coupling capacitance varies weakly as the wire width increases. One should notice that as wire space increases, the coupling capacitance decreases inversely whereas self-capacitance increases dramatically. A reasonable explanation for this is that as wires turn sparser they become closer to ground than to adjacent wires and thus self-capacitance increases.

Figures 2 and 3 also show that for the adopted typical wire width and wire space, the coupling capacitance of a global interconnect is comparable to its self-capacitance and coupling capacitance of an intermediate interconnect, but much larger than its self-capacitance. Coupling capacitance plays a key role in the total dynamic power, and the dynamic power can be dramatically lowered if the coupling capacitance can be effectively reduced.

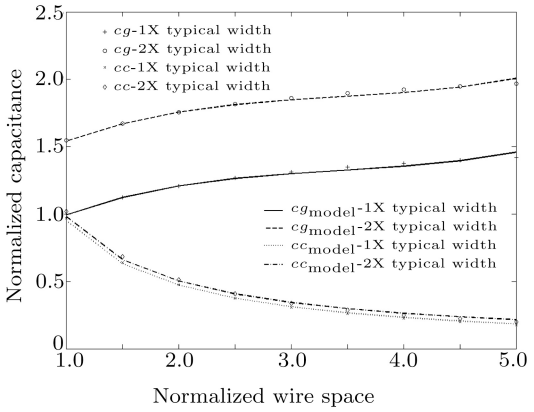


Fig. 2. Sums of normalized self-capacitance and normalized coupling capacitance of global interconnect versus normalized wire space under a 90-nm technology node.

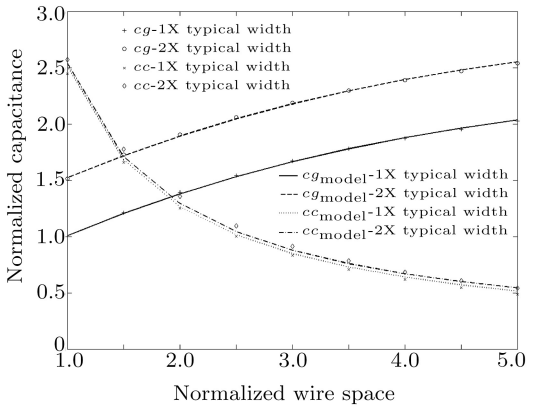


Fig. 3. Sums of normalized self-capacitance and normalized coupling capacitance of intermediate interconnect versus normalized wire space under a 90-nm technology node.

If non-uniform spacing technology is adopted in the routing of an interconnect bus consisting of n parallel interconnects, the self-capacitance for a given wire should be calculated by averaging the contributions from the left and the right wires.[10] Consequently, matrices of self-capacitance and coupling capacitance can be expressed as follows:

$$C_{\rm G} = \begin{bmatrix} c_{\rm g1} \\ c_{\rm g2} \\ \vdots \\ c_{{\rm g}n} \end{bmatrix} = \varepsilon \cdot \left(p_0 \cdot w \cdot \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} + \frac{1}{2} \cdot \begin{bmatrix} 1 & 1 & 0 & \cdots & 0 & 0 \\ 0 & 1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 1 & 1 \end{bmatrix} \cdot \left(\begin{bmatrix} s_0^3 & s_0^2 & s_0 & 1 \\ s_1^3 & s_1^2 & s_1 & 1 \\ \vdots & \vdots & \vdots & \vdots \\ s_n^3 & s_n^2 & s_n & 1 \end{bmatrix} \cdot \begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \end{bmatrix} \right) \right), \tag{5}$$

$$C_{\rm C} = \begin{bmatrix} c_{\rm c0} \\ c_{\rm c1} \\ \vdots \\ c_{{\rm c}n} \end{bmatrix} = \varepsilon \cdot \left((q_0 + q_1 \cdot w) \cdot \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} + q_2 \cdot \begin{bmatrix} 1/s_0 \\ 1/s_1 \\ \vdots \\ 1/s_n \end{bmatrix} \right), \tag{6}$$

where $c_{{\rm g}i}$ denotes the self-capacitance of wire i in Fig. 1, $i = 1, 2, \ldots, n$, and $c_{{\rm c}j}$ and s_j denote the coupling capacitance and the distance between wire $(j-1)$ and wire j respectively, $j = 0, 1, \ldots, n$.

2.2. Interconnect bus power model

The power dissipation of a buffered bus consists of switching power, leakage power and short-circuits power. Compared with the other two parts, short-circuit power is so small that it can be neglected in the power model. Switching power still plays a key role in total power dissipation and dominates total power dissipation, though leakage power increases with technology scaling down. Dynamic power is related not only to capacitance, but also by a bus switching factor. Therefore a switching factor is needed before presenting an analytical dynamic power model.

Table 1. Energy consumed by interconnects in different transmission cases.

c_c	(w_{i+1}, w_i)	
$0 \times c_{\rm c}v^2$	- -, ↑↑, ↓↓	case 1
$1 \times c_{\rm c}v^2$	- ↑, - ↓, ↑ -, ↓ -	case 2
$4 \times c_{\rm c}v^2$	↑↓, ↓↑	case 3

For a specified application, the switching factor can be predicted or obtained statistically by running a typical application. The statistical result can truly reflect the switching factor if the sample is abundant enough. Here, we express bus switching factor matrix as $\alpha = [\alpha_1 \alpha_2 \ldots \alpha_n]$, where α_i denotes the switching probability of data transmitted on wire i, i.e. the switching factor. As shown in Table 1, the energy consumed by the interconnects implies discrete values varying from $0 \times c_{\rm c}v^2$ to $4 \times c_{\rm c}v^2$, where v is the voltage swing of the interconnect bus, for different transmission cases. This fact will lead to the correlation between the power model and concrete data transmitted on the interconnect bus. In order to overcome this problem, a relative switching factor β is proposed in this paper and it is defined as the ratio of expectation of energy consumed by coupling capacitance between two adjacent wires to $c_{\rm c}v^2$ in a single data transmission, that is to say, $\beta = p_{\rm exp}/c_{\rm c}v^2$. Assuming that the data transmitted on wire i and wire $(i+1)$ are independent of each other, according to Table 1 $p_{{\rm exp},i}$ can be expressed as follows:

$$p_{{\rm exp},i} = c_{c,i} \cdot (\alpha_{i+1} + \alpha_i) \cdot v^2. \tag{7}$$

Then we can obtain the following relationship according to the definition of the relative switching factor:

$$\beta_i = \alpha_{i+1} + \alpha_i, \tag{8}$$

where β_i denotes the relative switching factor between wire i and wire $(i+1)$. Specially there is $\beta_0 = \alpha_1$ as wire 0 (ground line) is not used to transmit any data and wire 0 has a switching factor of 0. This condition corresponds to case 2 in Table 1. For an n-bit interconnect bus, as shown in Fig. 1, its relative switching factor matrix can be expressed as $\beta = [\beta_0 \beta_1 \ldots \beta_n]$. As part of the experimental results, the validity of Eq. (8) will be verified in Section 4.

Taking the self-capacitance and the coupling capacitance into account, the dynamic power of an n-bit interconnect bus can be expressed as follows:

$$P = (\alpha \cdot C_{\rm G} + \beta \cdot C_{\rm C})\, v^2 f, \tag{9}$$

where P, v, and f denote the dynamic power, voltage swing and working frequency of the interconnect bus, respectively. The two parts in the brackets denote contributions of self-capacitance and coupling capacitance, respectively.

3. Interconnect bus power optimization method

The interconnect bus power model represented by Eq. (9) indicates that several parameters, such as volt-

age swing, working frequency, switching factor, self-capacitance or coupling capacitance, can be chosen and optimized to reduce the bus power. In this paper, we focus on optimizing the switching factor, self-capacitance and coupling capacitance only, instead of taking all parameters into account. The optimization method presented here consists of two parts: optimal wire ordering and optimal wire spacing.

3.1. Optimal wire ordering

Optimizing wire ordering is regarded as the process for finding a specified wire order that can maximally enhance the effect of optimal wire spacing. All the possible wire orders for an n-bit interconnect bus can be up to $0.5 \times n!$. Taking an 8-bit bus and a 16-bit bus for example, they have possible wire orders of about 2×10^4 and 1×10^{13}, respectively. Searching in such a large solution space is time consuming and nearly impossible.

Fortunately, the existence of a unique power-optimal wire order has been proven in Refs. [10], [13]–[15]. Assuming that the coupling capacitance is inversely proportional to wire space and ignoring the self-capacitance, Zuber *et al.*[10] and Gritzmann *et al.*[13] presented and proved this specific wire order separately. Taking the same assumption and ignoring the relation between self-capacitance and wire space, Moiseev *et al.*[14,15] also constructed and proved this optimal wire order.

However, one can see clearly from Figs. 2 and 3 that self-capacitance is comparable to coupling capacitance and strongly dependent on wire space. Consequently, self-capacitance and its effect on wire space should not be ignored in optimization. As these two factors were not considered in Refs. [10], [13]–[15], whether their conclusions still hold in this condition should be verified first. For the 8-bit interconnect bus with several distinct switching factor matrices in this paper, we search for the optimal wire order (including all possible wire orders) using different searching algorithms. Abundant experimental data show that the conclusions in Refs. [10], [13]–[15] still hold in this paper on condition that the coupling capacitance is comparable to the self-capacitance while this requirement can be easily satisfied in nanometer scale integrated circuits.

Generally, the switching factor rises from 0 to 0.5 gradually from most significant bit (MSB) to least significant bit (LSB). We define bit 1, bit 2 ... bit (n) according to the switching factor order from the smallest to the largest. That is to say, bit 1 is regarded as the wire with the smallest switching factor and bit n is considered as the wire with the largest switching factor. Then the optimal wire order will be {GND, bit 1, bit 3, bit 5 ... bit $(n-1)$, bit (n), ..., bit 6, bit 4, bit 2, GND}[10,13–15] as shown in Fig. 4, and the switching factor rises gradually from two sides to the middle. Relative switching factor is depicted in Fig. 5, where a rising trend of β from two sides to the middle is shown. An intuitive explanation for Figs. 4 and 5 is that such a wire order can minimize $\sum \beta$ as much as possible and help reduce the distance shared by "weak coupling wires" and increase the distance shared by "strong coupling wires" so as to reduce $\sum C_{\mathrm{C}}$ and finally leads to a minimum value of $\beta \cdot C_{\mathrm{C}}$.

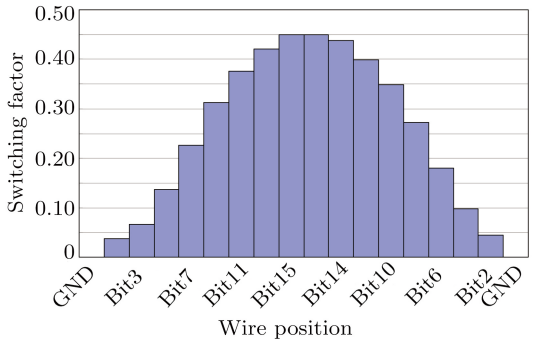


Fig. 4. Optimal wire order and switching factor.

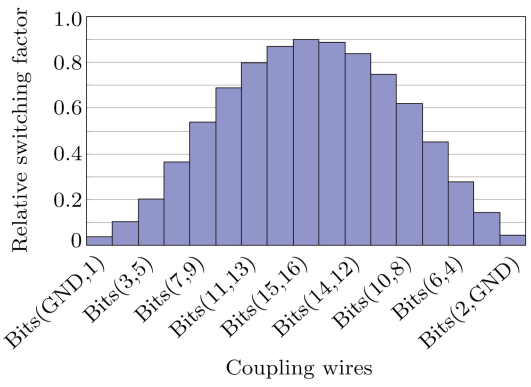


Fig. 5. Optimal wire order and relative switching factor.

3.2. Optimal wire spacing

As the communication mechanism between subsystems is usually realized using a high-speed interconnect bus, the on-chip bus has been a performance and power bottleneck in nanometer scale integrated

circuits. In order to satisfy the performance requirements, such as, for time delay, signal slew rate and crosstalk, some constraints should be introduced in the process of optimization. Assuming that the wire width is constant, the wire space is chosen to be used as the constraint and no wire space is allowed to be smaller than the constraint.

Based on the above analyses, in this section we present an interconnect bus power optimization method with combining wire spacing with wire ordering. Adopting the wire order presented in the last section, the optimization model can be written as the following expression:

$$\begin{aligned} &\min . P \\ &\text{s.t.} \begin{cases} C_{\text{coef}} \cdot S = (1+\delta) \cdot s_{\min}, \\ S \geq s_{\text{c}} \cdot C_{\text{coef}}^{\text{T}}, \end{cases} \\ &C_{\text{coef}} = \left[1 \ 1 \ \cdots \ 1 \right], \\ &S = \left[s_0 \ s_1 \ \cdots \ s_n \right], \end{aligned} \tag{10}$$

where C_{coef} is the coefficient matrix with a size of $1 \times (n+1)$, and its elements are all 1 in value; $C_{\text{coef}}^{\text{T}}$ denotes the transpose of C_{coef}; S represents the matrix of distances between two adjacent wires and it has a size of $1 \times (n+1)$ too; $s_{\min}$ means the minimum space needed to layout an n-bit bus adopting minimum wire width and minimum wire space; δ refers to the slack of routing space (the extra space available can be used for placing wires) and s_{c} is the constraint of wire space. The remaining parameters have the same meanings as those mentioned above. The first equality constraint shows that the routing space can be used and the second inequality indicates the constraint condition that should be satisfied during the optimization. It is a minimum problem of a constrained nonlinear multivariable function and there are many special numerical methods that can be used to handle this problem.

4. Model verification and discussion

Buses can be divided into address buses and data buses according to the type of data transmitted on them. Most of the data transmitted on address buses vary gradually and all show a smaller value of $(\alpha \cdot C_{\text{G}} + \beta \cdot C_{\text{C}})$ compared with the data transmitted on data buses. As will be illustrated at the end of this section, the optimization method should be more effective on an address bus if it is effective on a data bus. Therefore, a data bus is chosen as an optimization object.

The verification is performed on the assumption that only audio and video data are transmitted on interconnect buses, and we refer to the bus only transmitting audio data as an audio bus and the other one as a video bus. In fact, the data transmitted on a bus is a mixture of data of all these types and other types. However, at that time, the weighted average value of the switching factor can be obtained and then this method can be used.

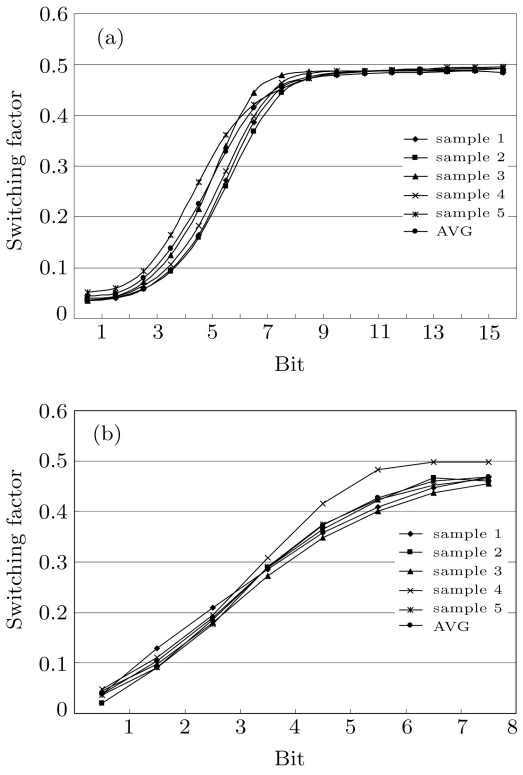


Fig. 6. Statistical results of switching factors for an audio bus (a) and a video bus (b).

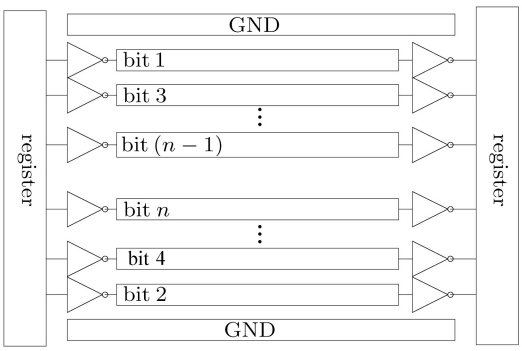


Fig. 7. Layout of an optimal interconnect bus.

Switching factor matrices of an audio bus and a video bus are obtained in this paper by taking statistics over several samples containing abundant data.

As shown in Figs. 6(a) and 6(b), every statistic contains 5 samples and their average value, and all the samples show similar properties. Clearly MSB has a switching factor of about 0 and LSB has a switching factor of nearly 0.5, which indicates the predictability of MSB and the randomicity of LSB.

Under 65-nm, 90-nm and 130-nm technology nodes, intermediate buses and global buses are optimized in this section. All interconnect parameters are provided by the BPTM.[12,16,17] The optimal interconnect bus layout is depicted in Fig. 7 where high bits are distributed on both sides and low bits are distributed in the middle so as to increase the space shared by low bits and consequently reduce the coupling capacitance between low bits. Now the relative switching factors of the audio bus and the video bus are depicted in Figs. 8(a) and 8(b), respectively, where the statistical value and calculated value from Eq. (8) are presented simultaneously. One can observe that the statistical results fit to Eq. (8) nicely, except for two points on both sides. This observation indicates that ignoring the relativity of signals is acceptable.

To compare the dynamic powers of interconnect buses adopting a minimum wire space, Table 2 and Table 3 show the power savings that can be provided by this optimization method and uniform spacing technology for different routing space slacks. For a value of slack of 50% under a 65-nm technology node, 27.68% power of an intermediate audio interconnect bus and 21.78% of power of a global audio interconnect bus can be saved by uniform spacing technology, whereas 32.26% of power of an intermediate audio interconnect bus and 25.39% of power of a global audio interconnect bus can be saved by the proposed optimization methodology, with an average power saving of 4.09%. In addition, under the same conditions 27.68% of power of an intermediate video interconnect bus and 21.78% of power of a global video interconnect bus can be saved by uniform spacing technology, whereas 33.03% of power of an intermediate video interconnect bus and 26.03% of power of a global video interconnect bus can be saved by the proposed optimization methodology, with an average power saving of 4.80%. Considerable results can be obtained by the optimization methodology. It is easy to conclude from Tables 2 and 3 that better results can be obtained for a relatively big value of slack.

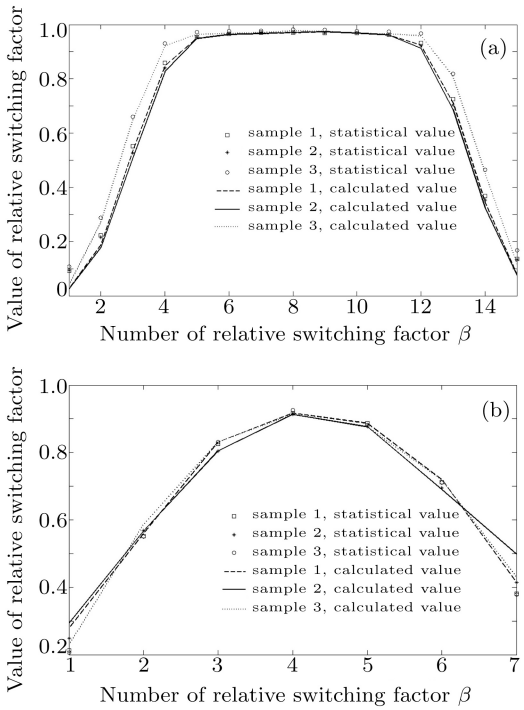


Fig. 8. Relative switching factors of the audio bus (a) and the video bus (b).

Table 2. Power savings provided by the two routing methods, with the audio bus acting as an optimization object.

δ	Wire type	Global			Intermediate		
	Tech. node	65 nm	90 nm	130 nm	65 nm	90 nm	130 nm
10%	Uniform spacing	6.15%	6.15%	5.87%	7.73%	7.48%	6.87%
	Optimization method	8.24%	8.23%	7.84%	10.38%	10.04%	9.19%
	Extra power saving	2.08%	2.08%	1.97%	2.65%	2.55%	2.32%
30%	Uniform spacing	15.32%	15.30%	14.53%	19.38%	18.70%	17.06%
	Optimization method	18.73%	18.68%	17.67%	23.79%	22.89%	20.77%
	Extra power saving	3.41%	3.18%	3.14%	4.40%	4.18%	3.71%
50%	Uniform spacing	21.78%	21.71%	20.52%	27.68%	26.62%	24.13%
	Optimization method	25.39%	25.24%	23.70%	32.26%	30.91%	27.84%
	Extra power saving	3.60%	3.53%	3.18%	4.58%	4.30%	3.71%

A comparison of Table 2 and Table 3 indicates that with switching factor becoming smaller, the uniform spacing provides a constant power saving while the proposed optimization method provides a rising power saving. Consequently better results can be achieved when this optimization method is applied to an address bus due to its smaller switching factor. Additionally, as reported in Ref. [9], that 95% of signals in a high-end microprocessor have switching factors less than 0.2 guarantees the application scope of this optimization method.

Table 3. Power savings provided by the two routing methods, with the video bus acting as an optimization object.

δ	Wire type	Global			Intermediate		
	Tech. node	65 nm	90 nm	130 nm	65 nm	90 nm	130 nm
10%	Uniform spacing	6.15%	6.15%	5.87%	7.73%	7.48%	6.87%
	Optimization method	8.90%	8.90%	8.46%	11.24%	10.86%	9.92%
	Extra power saving	2.75%	2.75%	2.59%	3.51%	3.38%	3.06%
30%	Uniform spacing	15.32%	15.30%	14.53%	19.40%	18.70%	17.06%
	Optimization method	19.46%	19.39%	18.31%	24.72%	23.76%	21.53%
	Extra power saving	4.14%	4.10%	3.78%	5.34%	5.06%	4.47%
50%	Uniform spacing	21.78%	21.71%	20.52%	27.68%	26.62%	24.13%
	Optimization method	26.03%	25.86%	24.22%	33.03%	31.62%	28.42%
	Extra power saving	4.25%	4.15%	3.70%	5.35%	5.00%	4.29%

5. Conclusion

An optimal wire order is verified in this paper and it helps us to avoid searching solution space for the optimal order. Based on this verification, combined with the analytical capacitance model proposed in this paper, a novel interconnect bus power optimization method adopting a no-uniform spacing technology is presented. Being a different form of bus coding, this optimization method does not need an overhead circuit. Optimizations of interconnect buses of different application types, at different interconnect layers, are performed under different technology nodes. The proposed optimization method provides considerable power savings and plays an important guiding role in the design and the optimization of interconnect buses in nanometer scale CMOS integrated circuits.

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