Research on high-voltage 4H–SiC P–i–N diode with planar edge junction termination techniques*

Zhang Fa-Sheng(张发生)[a)b)†] and Li Xin-Ran(李欣然)[b)]

[a)] School of Computer and Information Engineering, Central South University of Forestry and Technology, Changsha 410004, China

[b)] College of Electrical and Information Engineering, Hunan University, Changsha 410082, China

(Received 10 December 2010; revised manuscript received 26 January 2011)

The planar edge termination techniques of junction termination extension (JTE) and offset field plates and field-limiting rings for the 4H–SiC P–i–N diode were investigated and optimized by using a two-dimensional device simulator ISE-TCAD10.0. By experimental verification, a good consistency between simulation and experiment can be observed. The results show that the reverse breakdown voltage for the 4H–SiC P–i–N diode with optimized JTE edge termination can accomplish near ideal breakdown voltage and much lower leakage current. The breakdown voltage can be near 1650 V, which achieves more than 90 percent of ideal parallel plane junction breakdown voltage and the leakage current density can be near 3×10^{-5} A/cm^2.

Keywords: silicon carbide, P–i–N diode, junction termination technique, simulation, breakdown voltage

PACS: 71.20.Nr, 85.30.De, 85.30.Kk, 78.40.Fy **DOI:** 10.1088/1674-1056/20/6/067102

1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor material. Owing to its very good properties such as high breakdown critical electric field, great thermal conductivity and high saturation-electron drift velocity, it has been used to fabricate high-power, high temperature and high-speed devices.[1−5] Based on the advantages mentioned above, 4H–SiC is one of the most promising candidates for power semiconductor devices.

Compared with 4H–SiC Schottky barrier diode (SBD), 4H–SiC P–i–N diode is more attractively used in high voltage field. The 4H–SiC P–i–N diode with breakdown voltage up to 20 kV has been reported.[6] The 4H–SiC P–i–N diodes can obtain high reverse breakdown voltage with thin and low doping level voltage blocking epitaxial layer. But most 4H–SiC P–i–N diodes are in mesa structure, not parallel plane structure so far. As the simple fabrication process, the parallel plane structure is more attractive. Moreover, with the maturation of junction termination technique, parallel plane 4H–SiC P–i–N diode can achieve high breakdown voltage too.

For high power semiconductor devices, in order to improve the breakdown voltage, an adequate edge termination is necessary to reduce the electric field crowding effect at the periphery of P–i–N junction. To date, several techniques have been proposed to reduce the electric field crowding effect. These include field-limiting rings (FLR),[7,9] field plates (FP),[10] offset field plates and field-limiting rings (OFP–FLR),[8,11] junction termination extension (JTE),[8] and other non-planar level structures.[7] Among these techniques, JTE has been used extensively for higher blocking capability devices because of its superior advantages, such as effective termination area utilization, near ideal breakdown voltage achievable and suitability to many device types and coarser photolithography. However, the remarkable variation of breakdown voltage along with JTE implanted dose will cause the process window limited and increase the implementation complexity of JTE technique. For this reason, in this work, JTE edge terminations were studied by a two-dimensional device simulator ISE-TCAD10.0 to optimize the device performance and extract some dependent parameters. In addition, they were also compared with the most commonly used edge termination technique, OFP–FLR. Finally, these optimized structures were performed experimentally to test and verify the feasibility of JTE edge termination technique for 4H–SiC P–i–N diode.

*Project supported by the Science and Technology Foundation of Hunan Province of China (Grant No. 2008FJ3102).

†Corresponding author. E-mail: zhang_fs@126.com

© 2011 Chinese Physical Society and IOP Publishing Ltd

2. Device simulation model

The two-dimensional (2D) numerical device simulator ISE-TCAD10.0 is used to simulate the characteristics of 4H–SiC P–i–N diode with junction termination technique by solving Poisson's equation and carrier continuity equation.[12,13] The models for 4H–SiC P–i–N diode are shown as follows:

$$\varepsilon\nabla^2\psi = -q(p - n + N_{\rm D}^+ - N_{\rm A}^-) - \rho_{\rm s}, \tag{1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla j_n - U_n = F(\psi, n, p), \tag{2}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla j_p - U_p = F(\psi, n, p), \tag{3}$$

$$j_n = -q\mu_n n\nabla\varphi_n, \tag{4}$$

$$j_p = -q\mu_p p\nabla\varphi_p, \tag{5}$$

where ψ is the intrinsic Fermi potential, $N_{\rm D}^+$ and $N_{\rm A}^-$ are the ionized impurity concentration respectively, $\rho_{\rm s}$ is the surface charge density, μ_n and μ_p are the electron and hole mobility respectively, ε is the electrical permittivity, q is the electronic charge, n and p are the electron and hole densities respectively, U_n and U_p are the net electron and hole recombination rate respectively, j_n and j_p are the electron and hole current density respectively, ϕ_n and ϕ_p are the electron and hole quasi-Fermi potential respectively.

As we know, there are two mechanisms including avalance and tunneling breakdown which can be occurred at the P–i–N diode junction. Since the tunneling breakdown mainly occurs in very low-voltage condition, so the avalance breakdown mechanism is considered mainly in the paper. The P–i–N diode avalance breakdown condition is:[14]

$$\int_0^w \alpha_n \exp\left(\int_0^x (\alpha_p - \alpha_n)\,{\rm d}x'\right){\rm d}x = 1, \tag{6}$$

where w is the drift layer thickness of 4H–SiC P–i–N diode, α_n and α_p are the impact ionization coefficients for the electron and hole respectively, which are given by the following equation

$$\alpha_n = a_n \exp\left(\frac{-b_n}{E}\right), \tag{7}$$

$$\alpha_p = a_p \exp\left(\frac{-b_p}{E}\right). \tag{8}$$

The parameter values are taken as follows:[15]

$$a_n({\rm cm}^{-1}) = 1.76\times10^8, \quad b_n({\rm V/cm}) = 3.30\times10^7;$$
$$a_p({\rm cm}^{-1}) = 3.41\times10^8, \quad b_p({\rm V/cm}) = 2.50\times10^7.$$

The critical breakdown field in 4H–SiC P–i–N diode can be approximated by the following equation[16]

$$E_{\rm cr} = \frac{2.49\times10^6}{1 - \frac{1}{4}\log_{10}(N/10^{16}\ {\rm cm}^{-3})}. \tag{9}$$

The critical breakdown field in 4H–SiC appears to be more than 10 times higher than breakdown field in silicon.

The incomplete impurity ionization model is considered, which means that the impurity is not fully ionized at room temperature. Ionization rate is only 75% for 4H–SiC with 10^{17} cm^{-3} n-type doping concentration at 300 K. However, the ionization rate increases with temperature and it is about 95% at 700 K for 4H–SiC with 10^{17} cm^{-3} n-type doping concentration. The concentration of ionized impurity atoms is given by

$$N_{\rm D}^+ = \frac{N_{\rm D}}{1 + G_{\rm D}(T)\exp\left(\dfrac{E_{\rm Fn} - E_{\rm c}}{k_{\rm B}T}\right)}, \tag{10}$$

$$N_{\rm A}^+ = \frac{N_{\rm A}}{1 + G_{\rm A}(T)\exp\left(-\dfrac{E_{\rm Fp} - E_{\rm v}}{k_{\rm B}T}\right)}, \tag{11}$$

where $N_{\rm A}$ and $N_{\rm D}$ are the acceptor and donor concentration respectively, $E_{\rm Fp}$ and $E_{\rm Fn}$ are the quasi-Fermi energies for electrons and holes respectively, $E_{\rm C}$ and $E_{\rm V}$ are the conduction band and valance band energies respectively, $G_{\rm A/T}$ is the degeneracy factor for the impurity level, T is the lattice temperature and $k_{\rm B}$ is the Boltzman's constant.

The following simulations were performed at 300 K by using DESSIS-ISE10.0 software. We define the reverse breakdown voltage as the point where the P–i–N diode reverse leakage current comes to 1×10^{-7} A. This low limiting condition is set to avoid computer long time simulation running because no further change in $V_{\rm P-i-N-breakdown}$ was observed after the reverse leakage current reached this value.

3. Device structure and simulation

To optimize the characteristics of edge terminations for 4H–SiC P–i–N diode, a 2D device simulator ISE-TCAD10.0 is used to analyse the devices. The cross sections of three edge terminations adopted in this work are illustrated in Figs. 1 and 2, respectively. The doping profile concentrations are regarded

as Gaussian distribution and all P–i–N diode junctions are considered to be formed at the same moment. So the p^+ main junction and p^+ field-limiting rings have the same junction depth, however the JTE regions due to its much lightly doping concentration are shallower than others.

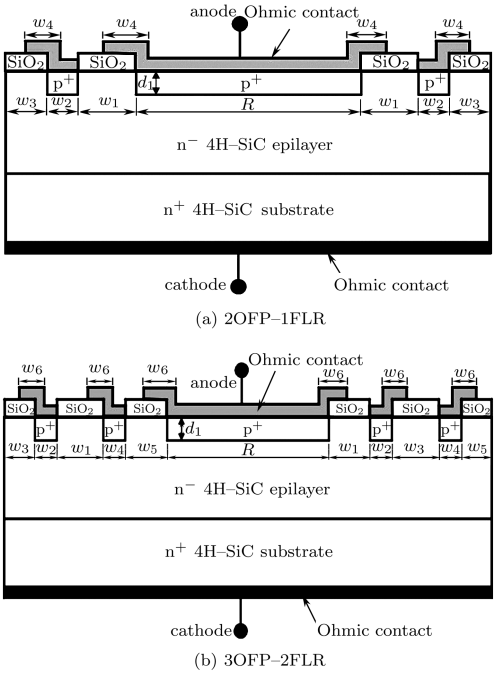


Fig. 1. Schematic cross section: (a) 2OFP–1FLR; (b) 3OFP–2FLR.

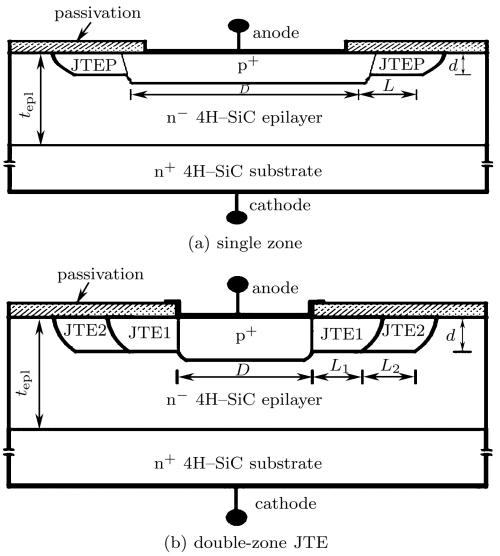


Fig. 2. Schematic cross section: (a) single zone; (b) double-zone JTE edge termination.

3.1. Termination techniques of OFP–FLR

Multiple OFP–FLR are designed to effectively reduce the electric field crowding influence. Figures 1(a) and 1(b) schematize a typical edge termination structure of 2OFP–1FLR and 3OFP–2FLR respectively, in which the first field plate is directly extended from the p^+ main junction electrode, but the others are coupled with their respective floating FLRs. By means of simulation optimization, the electric field distribution along the termination surface for 2OFR–1FLR, 3OFR–2FLR, 4OFP–3FLR and 5OFP–4FLR with a near breakdown voltage can be seen in Figs. 3 and 4.

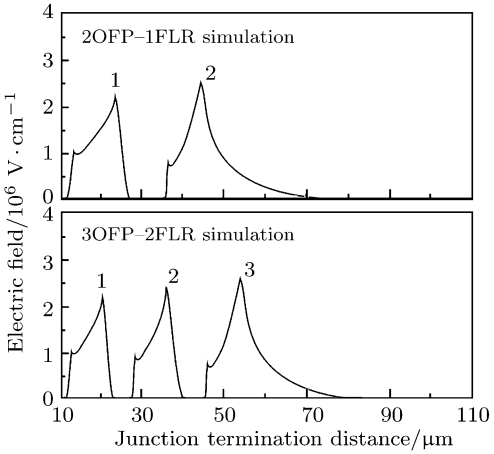


Fig. 3. Electric field distribution along the termination surface for 2OFP–1FLR and 3OFP–2FLR with a near breakdown voltage.

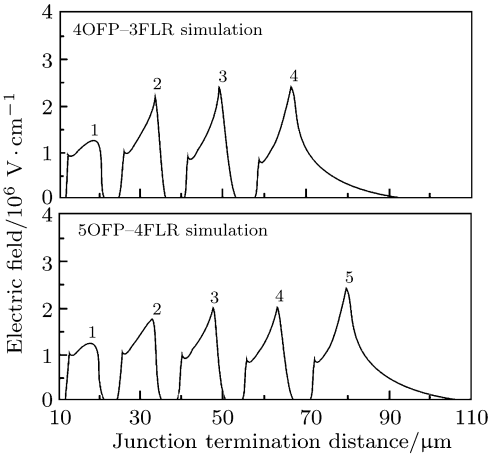


Fig. 4. Electric field distribution along the termination surface for 4OFP–3FLR and 5OFP–4FLR with a near breakdown voltage.

The arabic numerals shown in Figs. 3 and 4 represent the existing electric field peaks, which just correspond to the possible breakdown locations shown in Fig. 1. All these electric field peaks can be found at the silicon carbide surface and beneath the edge of each field plate. The extent of these peaks primarily depends on the spacing between each FLR. Obviously, equal spacing is not the optimum design and the best results can

be obtained by increasing the spacing gradually from the inner to the outer of termination. Besides, because of the voltage supported by the first FLR is higher, so if the first peak can be inhibited effectively, the electric field crowding effect will be improved further.

3.2. Termination techniques of JTE

With regard to JTE, two different structures of single-zone JTE and double-zone JTE are designed as shown in Figs. 2(a) and 2(b).

Usually, two competitive electric field peaks may exist at device edge to determine whether the breakdown will occur. One is bulk electric field peak and the other is surface electric field peak.[12] For single-zone JTE, one lightly JTE doping concentration is formed against the p^+ main junction to control these two electric field peaks simultaneously. This lightly doping must be high enough to suppress the bulk electric field and at the same time it also must be as low as possible to prevent the surface electric field. Thus, this JTE doping concentration is very critical and the implanted dose must be carefully controlled and chosen.

However, double-zone JTE method uses two different kinds of JTE doping (JTE 1 and JTE 2) to control these two electric field peaks independently, so these two peaks can be optimized separately. Therefore, double-zone JTE can be more insensitive to the variation of JTE doping concentration than single-zone JTE, but the drawback is that the extra process must be required.

Figures 5 and 6 disclose the optimized electric field distribution along the termination surface for single-zone JTE and double-zone JTE with a near breakdown bias. As can be seen, single-zone JTE shows two apparent peaks and they are exactly the bulk and surface electric field peak. These electric field peaks can make a well-balanced intensity to enhance its breakdown voltage by precisely controlling the JTE doping. In particular, for double-zone JTE shown in Fig. 6, an extra surface electric field peak at 2 zone exists near the interface between JTE 1 and JTE 2 zones. This extra surface electric field peak is produced by the increase of localized doping concentration due to the overlap of lateral diffusion of two adjacent JTE regions, so the extent is mainly determined by the doping difference between JTE 1 and JTE 2. In addition, figures 5 and 6 also show the electric field distribution with different JTE zone widths. It can be seen that the well-balanced electric field distribution almost keeps unchanged after the JTE zone width is enlarged. However, a broader electric field distribution and higher breakdown voltage can be achieved by increasing the JTE zone width.

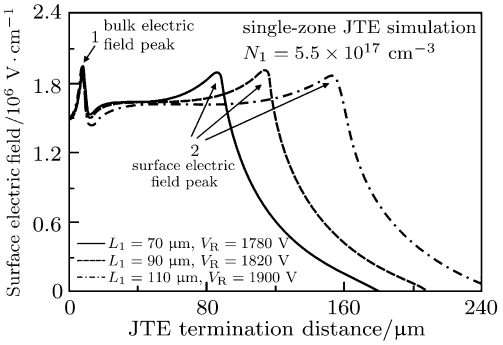


Fig. 5. Electric field distribution along the termination surface for single-zone JTE with different JTE zone widths at a near breakdown voltage.

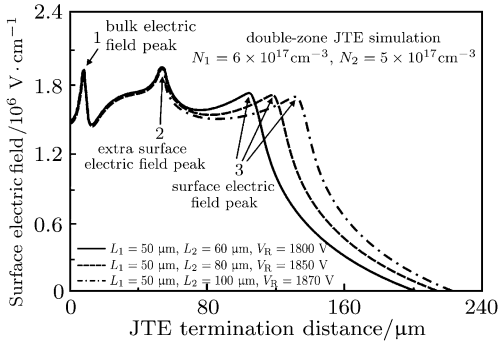


Fig. 6. Electric field distribution along the termination surface for double-zone JTE with different JTE zone widths at a near breakdown voltage.

The simulation outcomes of breakdown voltage for P–i–N diode as a function of termination width for single-zone JTE and OFP–FLR are compared in Fig. 7, where the termination width is defined as the distance from the p^+ main junction edge to the starting point of channel stop. Regardless of JTE or OFP–FLR, the breakdown voltage shows an upward tendency along with the termination width and finally reaches a saturated value. By making a comparison between JTE and OFP–FLR, JTE can not only support higher breakdown voltage but also require less termination area. The results can demonstrate that JTE is a much more effective edge termination technique than OFP–FLR.

In order to obtain the JTE doping concentration effect upon breakdown voltage, the concentration of assumed Gaussian distribution for JTE doping profile is varied. Figure 8 shows the simulation

results of breakdown voltage versus JTE concentration for single-zone JTE. Apparently, the tendencies of breakdown voltage along with concentration are all the same for four devices with different zone widths and they all have an identical optimum concentration of 3.8×10^{17} cm^{-3}. A considerable reduction of breakdown voltage is observed when the concentration deviates from the optimum value. Especially when the concentration is higher than the optimum value, the breakdown voltage will obviously decrease. However, the sharp reduction effect can be slightly compensated by extending the JTE zone width, because the breakdown voltage can be improved as the JTE zone width increases. But, the best design is still to make the doping concentration as close as the optimum value but not more than it.

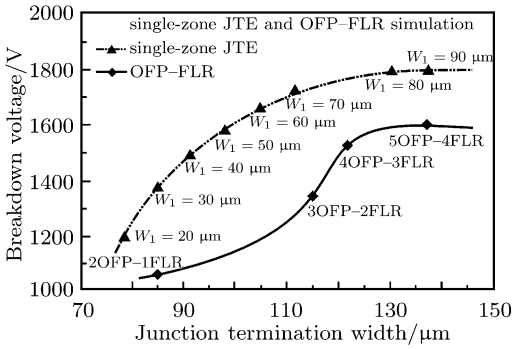


Fig. 7. Simulation results of breakdown voltage as a function of width for single-zone JTE and OFP–FLR.

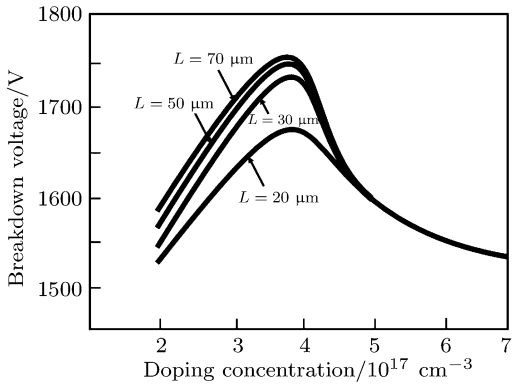


Fig. 8. Simulation results of breakdown voltage versus JTE concentration for single-zone JTE with different JTE zone widths.

Figure 9 indicates the simulation results of breakdown voltage versus JTE 1 and JTE 2 concentration for double-zone JTE. It can be obtained that the variation of breakdown voltage with doping concentration for double-zone JTE is much smoother than single-zone JTE shown in Fig. 8. This characteristics also shows the superior advantage for multi-zone JTE. Besides, an optimum N_1 of 4×10^{17} cm^{-3} can be obtained for all cases of N_2 and the breakdown voltage increases if N_2 can reach as close as 5×10^{17} cm^{-3}.

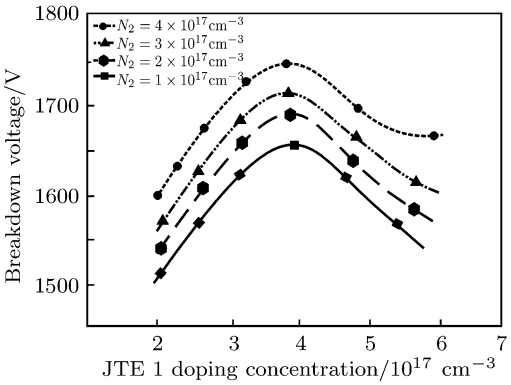


Fig. 9. Simulation results of breakdown voltage versus JTE 1 and JTE 2 concentrations for double-zone JTE.

4. Fabrication and experimental results

Based on the simulation results mentioned above, the high-voltage 4H–SiC P–i–N diode with JTE were fabricated on the epilayer, its schematic cross section is shown in Fig. 2(a). The thickness of p^+ region is 0.4 μm, diameter is 200 μm, the thickness and diameter of substrate are 350 μm and 300 μm respectively, the thickness and n^- concentration of the epilayer were 12 μm and 6×10^{15} cm^{-3} respectively. The boron ions were implanted to fabricate the p^+ anode (1×10^{19} cm^{-3}) and JTE (4.0×10^{17} cm^{-3}) respectively.[17] The depth (d) and total legth (L) of the JTE were 0.3 μm and 60 μm respectively. The Ni was deposited for the anode contact and cathode contact respectively.

The forward I–V characteristic for the 4H–SiC P–i–N diode is shown in Fig. 10. This forward current conduction mechanism follows the thermionic electron emission theory. The reverse I–V characteristic of

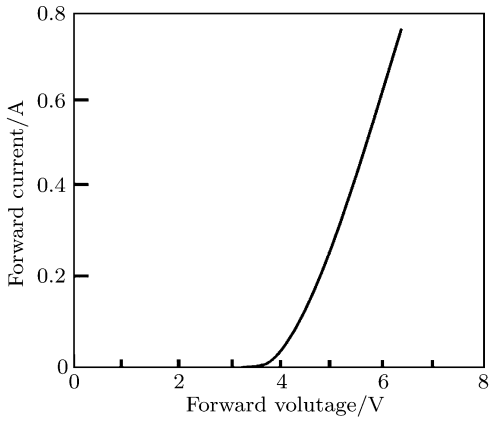


Fig. 10. Forward I–V characteristic of 4H–SiC P–i–N diode.

4H–SiC P–i–N diode is shown in Fig. 11, the avalanche breakdown voltage was observed at 1650 V, above 90% of the ideal V_B. The leakage current density can be estimated as low as 3×10^{-5} A/cm^2. The breakdown voltage of the fabricated device had a little lower than optimization simulation breakdown voltage because of some reasons, such as requiring precise control doping concentration for JTE, some defects for 4H–SiC epilayer etc.[18]

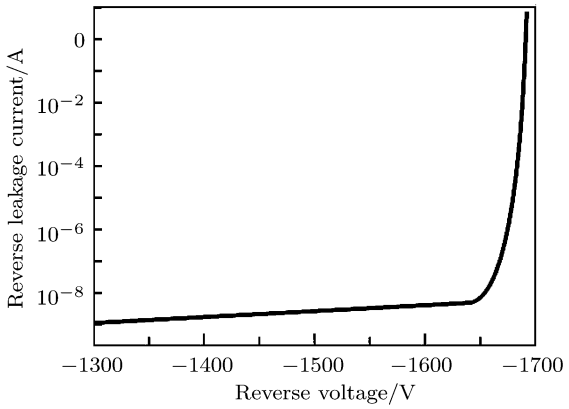


Fig. 11. Reverse I–V characteristic of 4H–SiC P–i–N diode.

5. Conclusions

In this work we have systematically studied the design and optimization of the planar edge termination techniques for high-voltage 4H–SiC P–i–N diode by ISE-TCAD10.0. By making a comparison between JTE and OFP–FLR, JTE can not only support higher breakdown voltage but also requires less termination area. Relatively to OFP–FLR, about 40% of termination area can be economized to achieve the same breakdown voltage for JTE. According to the simulation parameters of 4H–SiC P–i–N diode with single-zone JTE, we have succeeded in fabricating the 4H–SiC P–i–N diode with single-zone JTE. The results are shown to be in good agreement between simulated and experimental data, this fact proves that it is effective and practicable to use the ISE-TCAD10.0 simulator to simulate 4H–SiC P–i–N diode. The results presented in this work confirm that JTE is a feasible edge termination technique for higher blocking capability power 4H–SiC P–i–N diode. The farbrication technique can be also utilized for other high voltage silicon carbide devices, such as Schottky barrier diode, bipolar transistors and metal–oxide semiconductor field effect transistors, etc.

References

[1] Ostling M, Lee H S, Domeij M and Zetterling C M 2006 *Proc. Int. Conf. Mixed Design Ics Systems* (Gdynia, Poland) p. 34

[2] Tang H Z, Caruth D and Becher D 1999 *IEEE Electron. Device Lett.* **20** 245

[3] Saxena V, Su J N and Steckl A J 1999 *IEEE Trans. Electron. Devices* **46** 456

[4] Frey W L and Ryssel H 2001 *Appl. Surf. Sci.* **184** 413

[5] Wang S G, Yang L A, Zhang Y M, Zhang Y M and Yan J F 2003 *Chin. Phys.* **12** 322

[6] Sugawara Y, Takayama D, Asano K, Singh R, Palmour J W and Hayashi T 2001 *Proc. Int. Symp. Power Semicond. Devices Ics* (Osaka: Japan) p. 27

[7] Baliga J 1996 *Power Semiconductor Devices* (Boston: PWS Publishing Company)

[8] Yilmaz H 1991 *IEEE Trans. Electron Devices* **38** 1666

[9] Bose J V S C, Souza M M D, Narayanan E M S, Spulber O and Sweet M 1999 *Proc. Int. Semicond. Conf.* CAS'1 (Sinaia: Romania) p. 63

[10] Basavana Goud C 1991 *IEEE Trans. Electron. Devices* **38** 1497

[11] Basavana Goud C and Bhat K N 1992 *IEEE Trans. Electron. Devices* **39** 1768

[12] Temple V A K and Tantrapom W 1986 *IEEE. Trans. Electron. Devices* **33** 1601

[13] Song Q W, Zhang Y M, Zhang Y M, Lü H L, Chen F P and Zheng Q L 2009 *Chin. Phys.* B **18** 5474

[14] Fulop W 1967 *Solid State Electronics* **10** 39

[15] Hatakeyama T, Watanabe T and Shinohe T 2004 *Appl. Phys. Lett.* **85** 23

[16] Konstantinov A O, Wahab Q, Nordell N and Lindefelt U 1997 *Appl. Phys. Lett.* **70** 90

[17] Wang S G, Zhang Y, Zhang Y M and Zhang Y M 2010 *Chin. Phys.* B **19** 017203

[18] Wang S G, Zhang Y M and Zhang Y M 2003 *Chin. Phys.* **12** 89