A k-band broadband monolithic distributed frequency multiplier based on nonlinear transmission line*

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A fabrication technology of GaAs planar Schottky varactor diode (PSVD) is successfully developed and used to design and manufacture GaAs-based monolithic frequency multiplication based on 23-section nonlinear transmission lines (NLTLs) consisting of a coplanar waveguide transmission line and periodically distributed PSVDs. The throughout design and optimization procedure of 23-section monolithic NLTLs for frequency multiplication in the k-band range is based on a large signal equivalent model of PSVD extracted from small-signal S-parameter measurements. This paper reports that the distributed SPVD exhibits a capacitance ratio of 5.4, a normalized capacitance of 0.86 fF/μm^2 and a breakdown voltage in excess of 22 V. The integrated 23-section NLTLs fed by 20-dBm input power demonstrates a 26-GHz peak second harmonic output power of 14-dBm with 25.3% conversion efficiency in the second harmonic output frequency range of 6 GHz–26 GHz.

Keywords: nonlinear transmission line, frequency multiplication, harmonic generation, planar Schottky varactor diode

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1. Introduction

High frequency multipliers are widely used in microwave signal generators due to the lack of efficient and stable sources at microwave frequencies. Nonlinear transmission lines (NLTLs), consisting of coplanar waveguide (CPW) transmission line (TL) and fully distributed Schottky-barrier varactors used as the basic nonlinear component in microwave frequency multipliers due to their fast switching capability,[1,2] contain voltage-variable nonlinear capacitance and hence can be used for frequency conversion and are very suitable for high frequency harmonic generation.[3–6] The typical application of NLTLs, for instance harmonic generation with broad bandwidth and high efficiency, is feasible since they have an almost real input impedance and can be designed to provide a good matching to a resistive impedance (the input impedance is purely resistive for lossless NLTLs) and have much better phase noise characteristics.[7,8] While implementations using lumped-element Schottky varactor diodes have reactive input and output impedances which lead to narrow bandwidth. Terahertz (THz) cutoff frequency of Schottky diode and extreme high Bragg cutoff frequency from the periodic network of NLTLs push the operating frequency limit of the NLTLs far beyond the needs of today's electronics. Moreover CPW-based NLTLs need no complex processes such as via holes and back-plating, which were needed by microstrip-based NLTLs and cause limited bandwidth (up to 40 GHz) and lower performances.[3,9]

2. Schottky diode structure design and model

The conversion efficiency of second harmonics generated is proportional to the nonlinearity determined by the capacitance ratio of planar Schottky varactor diode (PSVD) over the range of applied voltages. Consequently, we optimize and design the following epilayers on a semi-insulating GaAs wafer: a 0.6 μm-thick n layer doped with Si at a level of 5×10^{16} cm^{-3},

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which was determined by a tradeoff between power handling ability and conversion efficiency and a 1 μm-thick n^+ active layer doped with 5×10^{18} cm^{-3}, which was optimized for good Ohmic contact and lower parasitical resistance.[10,11] A Schottky varactor diode with a 20 μm×8 μm Schottky contact is designed to satisfy the k-band frequency multiplication applications. By using the optimized diode doping profile, a zero-biased cutoff frequency of higher than 1 THz and the breakdown voltage of 22 V was achieved. The schematic of PSVD was shown in Fig. 1(a). Figure 1(b) shows the large signal equivalent circuit model for PSVD. This equivalent circuit model can be divided into two parts: 1) the nonlinear intrinsic elements R_j and C_j, which are dependent on the applied voltage, 2) the extrinsic parasitic elements R_s, C_p, C_i, C_o, and L_s, which are independent of the applied voltage. The R_j and C_j represent nonlinear junction resistance and nonlinear capacitance of the active layer of PSVD, R_s represents series resistance, C_p is the finger-to-Pad capacitance, L_s is the finger inductance from the physical geometry of PSVD, the anode and cathode capacitance to ground is represented by C_i and C_o, respectively.

The measured capacitance–voltage characteristic for 20 μm×8 μm PSVD at 1 MHz by an Agilent 4284A Precision LCR Meter can be seen in Fig. 1(c). The junction capacitance of PSVD can also be given by

$$C_j = \frac{C_{j0}}{\left(1 - \dfrac{V}{V_{bi}}\right)^M}, \tag{1}$$

where C_{j0} is zero-bias junction capacitance of 125 fF, V_{bi} is the barrier potential of 0.65 V and M is index factor of 0.35 depended on the diode doping profile. The capacitance ratio between the maximum capacitance C_{max} and minimum capacitance C_{min} of PSVD over the range of applied voltages (−10 V to 0.6 V) is 5.4 and is usually used to weight the device nonlinearity. The DC I–V characterization of PSVD was measured on an HP4155 Semiconductor Parameter Analyser. The PSVD with active area of 160 μm^2 had an ideality factor of 1.04, series resistance (R_s) of 3.8 Ω and the reverse saturation current of 31.97 fA. The measured breakdown voltage is 22 V. These parameters of large signal model for PSVD with area of 160 μm^2 are shown in Table 1. Finally, the extracted lumped-element model of the PSVD was implemented by using a symbolically defined device (SDD) in Agilent Advanced Design System (ADS) simulator and is used to design the frequency multiplier based on NLTLs.

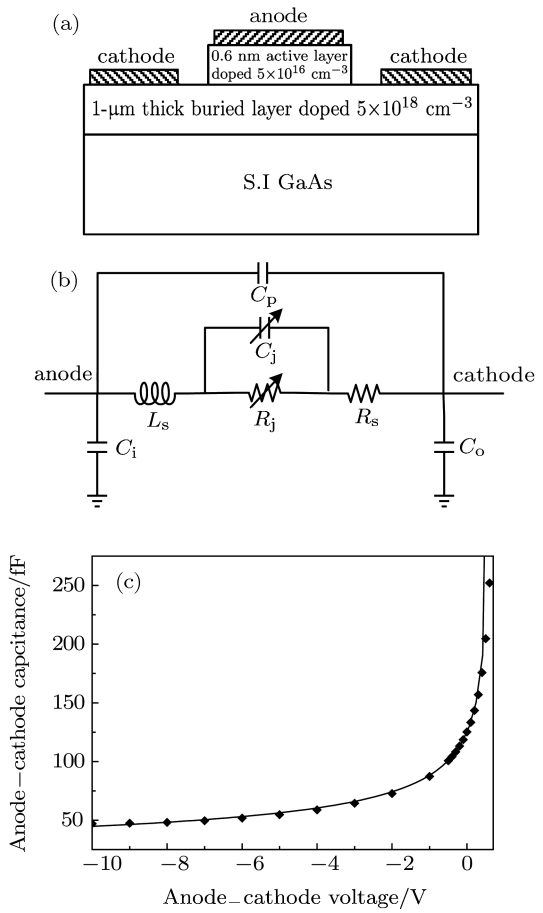


Fig. 1. (a) The schematic diagram of PSVD; (b) equivalent circuit of the PSVD; (c) C–V characteristic measured at 1 MHz (dot: measured value, line: fitted C–V curve).

Table 1. Parameters of equivalent circuit model of the PSVD.

Parameter	Value	Parameter	Value
C_p/fF	1	I_s/fA	31.97
C_i/fF	0.5	N	1.0431
C_o/fF	4	C_{j0}/fF	125
L_s/pH	10	M	0.35
R_s/Ω	3.18	V_{bi}/V	0.65

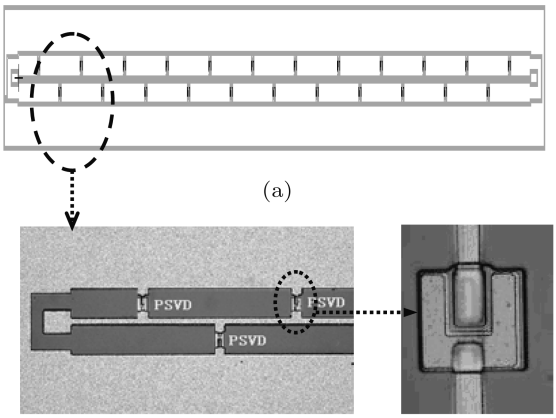
3. The NLTLs circuit design

The GaAs NLTL is a monolithic circuit, consisting of CPW TL with a high characteristic impedance of Z_0 and periodically at spacing L distributed PSVDs with reverse bias and exhibits nonlinearity from voltage-variable capacitance of PSVD and dispersion characterized by Bragg cutoff frequency from the periodic network.[12,13] The NLTLs design procedure, based on the large-signal model of PSVD, is similar to one adopted by Li and is followed as that in Ref. [14]. First input frequency of 13 GHz, input power of 20 dBm and −2 V bias are set and then the

optimal number of NLTLs sections (N) is chosen until the corresponding maximum second harmonic output power from harmonic balance simulation by ADS is obtained. Secondly geometric parameters of CPW TL, which include the central signal line width W, the gap S between centre signal line and the ground planes sitting on each side of the central signal line and the distance L between two adjacent nonlinear elements, are optimized for maximum secondary harmonic conversion efficiency over the input frequency range 4 GHz< $f_{\rm in}$ <15 GHz. It is necessary to optimize the CPW TL to prevent electromagnetic coupling between them, High Frequency Structure Simulator (HFSS) is used to demonstrate the coupling effect between those CPW TL. Finally the corresponding optimal values of W, S, L, and N are 20 μm, 89 μm, 300 μm, and 23, respectively. The effective permittivity $\varepsilon_{\rm eff}$ of 7.57 is dependent on the GaAs substrate thickness h of 350 μm, $\varepsilon_{\rm r}$ of 12.9 and conductor width W of 20 μm.[15] The distributed inductance $L_{\rm R}$ and capacitance $C_{\rm R}$ of one section CPW TL on 350 μm-thickness GaAs substrate ($Z_0 = 108\ \Omega$) is 0.3 nH and 25.5 fF, respectively.[8]

4. Integrated Schottky NLTLs fabrication

The NLTLs were fabricated by using standard GaAs processing techniques, similar to those reported in Ref. [16]. First, the first mesa etching was performed to expose the buried n^+ GaAs contact layer by wet chemical etching with a solution of H_3PO_4:H_2O_2:H_2O=2:3:30. Secondly, the Ohmic metal pattern of cathode was formed by an image reversal process using AZ5214 photoresist for the lift off process. After the pattern lithography, to achieve Ohmic metallization we evapourated Ni/Ge/Au/Ge/Ni/Au (40/40/660/80/30/2200 Å, (1 Å=0.1 nm)) using electron beam evapourator. Then the cathode was annealed at 375 °C for 60 s. The Schottky contacts were defined by evaporating Ti/Pt/Au and lift-off processes, then the second mesa etching was followed to achieve electronic isolation and the PSVD were passivated with 0.3-μm Si_3N_4. Then reactive ion etching was used to open windows over the metal contacts. Finally electroplating was executed to form interconnection between expanded metal pattern and Schottky and Ohmic contacts metal, CPW TL and the circuits. The NLTLs periodically distributed PSVDs shown in Fig. 2 were successfully fabricated on GaAs wafer.



(a)

(b)

Fig. 2. (a) Schematic showing layout of NLTLs; (b) photograph of the 7.16-mm fabricated multiplier based on NLTLs illustrating the details.

5. Measurement and discussion

5.1. Small signal measurements

The small signal measurements are taken on-wafer with a HP8510C network analyser and a Cascade Microtech probe station using a Thru-Reflet-Line calibration. Figure 3 shows the measured S-parameters of a 23-sectin CPW NLTLs, compared with simulated results which are achieved by using the SDD large signal model of PSVD and replacing the ideal models for CPW TL with their corresponding S-parameter files obtained by HFSS. Excellent agreement can be observed and indicates that the circuit model proposed is accurate and can be potentially used in the other microwave circuit application.

The frequency response (S_{21} and S_{11}) shown in Fig. 3 shows the low-pass characteristic characterized by the Bragg cutoff frequency of about 31 GHz and 40 GHz at a reverse voltage of 0- and 4.5-V bias, respectively. Experimentally, we define the corresponding frequency as the Bragg cutoff frequency when the S_{21} is −20 dB. It is observed that the Bragg cutoff frequency decreases with the increase of the reverse bias voltage, which is consistent with the relationship expressed as

$$f_{\rm B} = \frac{1}{\pi\sqrt{L_{\rm R}\left(C_{\rm R} + C_{\rm d}\left(V\right)\right)}}. \qquad (2)$$

Theoretically, the Bragg cutoff frequency is 32.5 GHz and 41.4 GHz for 0- and −4.5-V bias, respectively.

The measured Bragg cutoff frequency is in good agreement with experimental one. Additionally, the difference between the measured and experimental one is due to the fact that theoretical Bragg cutoff frequency is defined when an infinite number of unit cells are cascaded, however our circuit actually consists of 23 unit cells.[17]

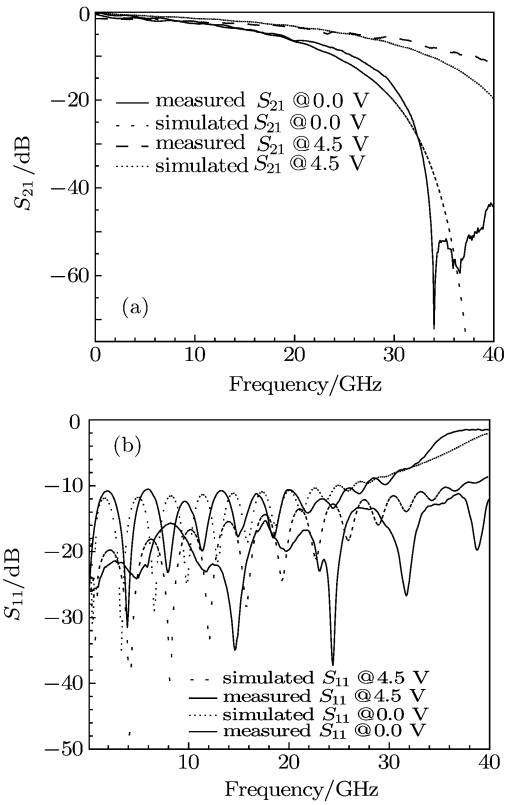


Fig. 3. The simulated and measured S-parameters of 23-section NLTLs multiplier at reverse 0-V and 4.5-V bias: (a) S_{21}; (b) S_{11}.

5.2. Large signal measurements

To investigate the performances of NLTLs such as the variations of the output power versus second harmonic frequency and power, a large signal radio frequency measurement was experimentally performed on-wafer by using HP83752B vector signal generator as synthesized microwave source and a 0–26 GHz HP8563E spectrum analyser and DC-40 GHz bias tees and wafer probes. When a 20-dBm signal of 13 GHz with a reverse bias voltage of 2.0 V was applied to the input port, the measured output spectrum is shown in Fig. 4, where the multiplier exhibited second harmonic output power of 14 dBm (including 3.3-dBm conversion loss) and a corresponding maximum second harmonic conversion efficiency of 25.3%. Moreover, when input frequency varies from 3 GHz to 13 GHz with the fixed 20-dBm power, the pure and stable spectrum of the output wave were also observed. Measured output second harmonic power versus input frequency at different biased voltages is shown in Fig. 5. It can be observed that the second harmonic output power decreases with the increase of the reverse bias voltage in the range of −2.0 V to −4.5 V and that relatively high conversion efficiency for second-harmonics over a broad frequency range of 6 GHz–26 GHz is also obtained experimentally by use of monolithic microwave integrated circuit (MMIC) technology. The optimal impedance match, determined by the capacitance of PSVD at the applied reverse bias voltage, is achieved when the reverse voltage of 2 V is applied, which leads to corresponding peak second harmonic output power. At the same time the output power of second harmonics is above 0 dBm in the fundamental frequency range of 3 GHz–13 GHz because their corresponding second harmonics frequency is below the Bragg cutoff frequency of NLTLs with a reverse bias voltage of 2.0 V and severe attenuation does not occur.

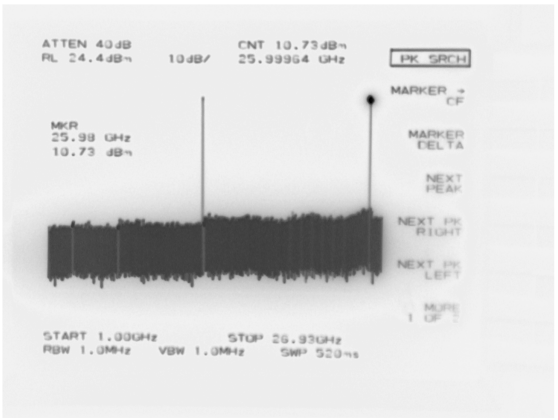


Fig. 4. Spectrum of the output wave form generated by a 23-section NLTLs multiplier fed by 13-GHz, 20-dBm input signal at reverse bias voltage of 2.0 V.

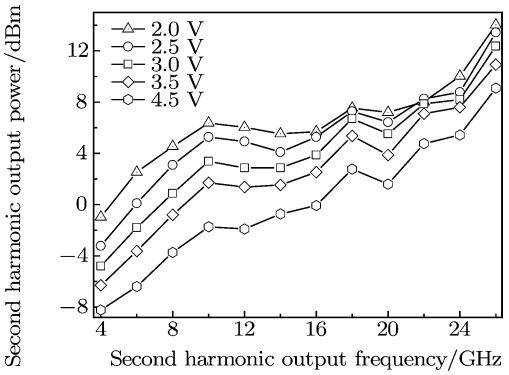


Fig. 5. Measured second harmonic output power versus second harmonic frequency at different reversed bias voltages.

6. Conclusions

The PSVD and corresponding large signal model was successfully developed to design a 23-section NLTLs MMIC for frequency multiplication in the k-band frequency range. It has been demonstrated that second harmonics can be stably obtained and that relatively high conversion efficiency for second-harmonics over a broad frequency range of 6 GHz–26 GHz is also obtained experimentally by use of MMIC technology. At the second harmonic output frequency of 26 GHz, second harmonic output power of 14 dBm with 25.3% conversion efficiency was measured with 20-dBm input power at 13 GHz. The behaviour of the NLTLs MMIC is imposed by the cutoff frequency of PSVD and the Bragg frequency of the NLTLs circuit. By properly designing the Bragg cut-off frequency, a suppression of the higher order harmonics can be obtained. The good performances of frequency multiplication based on NLTLs promise good prospects for microwave and THz applications.

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