# Substrate bias effects on collector resistance in SiGe heterojunction bipolar transistors on thin film silicon-on-insulator*

Xu Xiao-Bo(徐小波)†, Zhang He-Ming(张鹤鸣),
Hu Hui-Yong(胡辉勇), and Qu Jiang-Tao(屈江涛)

*Key Laboratory of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an* 710071*, China*

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An analytical expression for the collector resistance of a novel vertical SiGe heterojunction bipolar transistor (HBT) on thin film silicon-on-insulator (SOI) is obtained with the substrate bias effects being considered. The resistance is found to decrease slowly and then quickly and to have kinks with the increase of the substrate–collector bias, which is quite different from that of a conventional bulk HBT. The model is consistent with the simulation result and the reported data and is useful to the frequency characteristic design of 0.13 μm millimeter-wave SiGe SOI BiCMOS devices.

**Keywords:** collector resistance, substrate bias effect, SiGe heterojunction bipolar transistor, thin film silicon-on-insulator

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## 1. Introduction

In recent years, a novel vertical silicon–germanium heterojunction bipolar transistor (SiGe HBT) fabricated on thin film silicon-on-insulator (SOI) substrate has been proposed and integrated into the latest 0.13 μm millimeter-wave SiGe SOI BiCMOS technology. The devices fabricated with the new technology show decent performances, such as higher Early voltage, better trade-off between the base–collector avalanche breakdown voltage and the characteristic frequency and better proton radiation effect.[1−5] Compared to the HBT on bulk, the HBT on SOI has a thinner collector thickness. The buried layer is also absent in the HBT on SOI, which leads to a vertical and horizontal collector space charge region (SCR). The HBT operation is modeled with electrical characteristics at zero substrate bias.[6−9] To the best of our knowledge, the contribution of the substrate bias to the collector resistance $R_c$ has not been theoretically investigated, whereas the new device features a small collector width and hence a higher $R_c$, which can limit the device performance by internal forward biasing the base–collector junction and can limit the device frequency response by the RC time delay. The main aim of this paper is to show how the substrate bias effects on $R_c$ can be modeled, how $R_c$ can be linked to its physical origin and how the substrate terminal can be used to improve the electrical behaviours, such as device frequency response for partially depleted HBTs.

## 2. Modeling collector resistances for different substrate biases

A structure diagram of an SOI SiGe HBT is shown in Fig. 1. We limit the analysis to the left half side, as the structure is symmetric. The zero point of $x$ axis is located at the base side edge of the base–collector depletion region at zero bias and the zero point of $y$ axis is located at the edge of the base. The $L_E$ is the emitter length, the $W_E$ is the emitter width, the $W_B$ is the base width, the $W_{epi}$ is the collector width and the $L_{epi}$ is the collector length. Electrons injected from the emitter flow vertically down in the collector and make a turn towards the N+ collector contact region on the side. The intrinsic collector space charge extension is lateral at $V_{CiBi} = 0$ V for a fully de-

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†Corresponding author. E-mail: xxb_xidian@163.com

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pleted HBT and vertical at $V_{\rm CiBi} = 0$ V while lateral at higher reverse bias for a partially depleted HBT, where $V_{\rm CiBi}$ is the intrinsic reverse collector–base voltage.

As can be seen from Fig. 1, the collector–oxide–substrate structure is similar to a "back gate" acting as a PIN junction capacitance (MOS capacitance). The electron behaviour of the interface on the collector side depends on the substrate bias. Electrons would accumulate at the interface with a positive substrate acting as a subcollector layer and deplete with a negative substrate. Therefore the collector contact region (N+) links to the electron accumulation layer in the positive substrate case and no horizontal collector resistance occurs; the collector–base SCR expands further in the negative substrate case, which also influences the collector resistance.

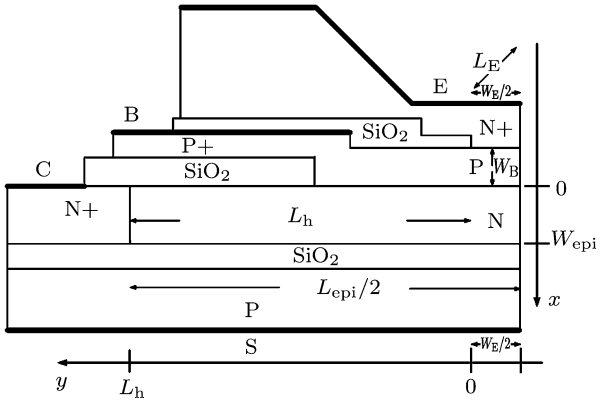



**Fig. 1.** Sketch of an SOI SiGe HBT.

In deriving the model, assumptions including a flat dope in the epilayer and an abrupt base–collector junction are made; the depletion and the low injection approximations are used; the hole drift and diffusion currents and the generation and recombination currents are ignored; the impurity atoms are assumed to be completely ionized.

In the negative substrate–collector bias case, the collector SCR consists of two components, one next to the collector–base interface and the other next to the collector–oxide interface. The former can be easily obtained by applying the one-dimensional Poisson's equation

$$x_1 = \sqrt{\frac{2\varepsilon_{\rm Si}(V_{\rm CB} + V_{\rm dc})}{qN_{\rm epi}}}, \tag{1}$$

where $x_1$ is the depletion width at the collector–base interface, $\varepsilon_{\rm Si}$ is the dielectric coefficient of Si, q is the charge of an electron, $V_{\rm CB}$ is the collector–base voltage, $N_{\rm epi}$ is the collector doping concentration, $V_{\rm dc} = V_T \ln(N_{\rm epi}^2/n_{\rm i}^2)$ is the built in potential with $n_{\rm i}$ the intrinsic concentration of Si and $V_{\rm T}$ the thermodynamic potential. The latter can be obtain according to the ideal MOS capacitance features, in which a flat energy band is assumed at zero bias, carriers exists only in semiconductors and no current exists in the insulator under direct current. The substrate capacitance $C_{\rm ts}$ is the series of oxide capacitance $C_{\rm ox}$ and SCR capacitance $C_{\rm Si}$ at the Si/SiO$_2$ interface on the collector side

$$\frac{1}{C_{\rm ts}} = \frac{1}{C_{\rm ox}} + \frac{1}{C_{\rm Si}}, \tag{2}$$

where $C_{\rm ox} = \varepsilon_{\rm SiO_2}/t_{\rm ox}$ and $C_{\rm Si} = \varepsilon_{\rm Si}/x_2$, $\varepsilon_{\rm SiO_2}$ is the dielectric coefficient of SiO$_2$, $t_{\rm ox}$ and $x_2$ are the oxide width and the SCR width next to the collector–oxide interface, respectively. It should be noted that the SCR capacitance at the Si/SiO$_2$ interface on the substrate side is neglected, as its contribution to $C_{\rm ts}$ is small due to the parallel connection of the capacitances in the circuit. With $-C_{\rm ts}V_{\rm SC} = qN_{\rm epi}x_2$ ($V_{\rm SC} = V_{\rm S} - V_{\rm C}$ is the substrate–collector bias), $x_2$ is obtained as

$$x_2 = \frac{-t_{\rm ox}\varepsilon_{\rm Si}qN_{\rm epi} + \sqrt{(t_{\rm ox}\varepsilon_{\rm Si}qN_{\rm epi})^2 - 4\varepsilon_{\rm Si}\varepsilon_{\rm SiO_2}^2 qN_{\rm epi}V_{\rm SC}}}{2\varepsilon_{\rm SiO_2}qN_{\rm epi}}. \tag{3}$$

Figures 2 and 3 show the sketches of electron flow paths in partially and in fully depleted operation modes respectively. In the partially depleted operation mode, $x_1 + x_2 \le W_{\rm epi}$, the SCR is vertical, the current flow area is $L_{\rm E} \times W_{\rm E}/2$; in the fully depleted operation mode, $W_{\rm epi} < x_1 + x_2 \le L_{\rm h} + W_{\rm epi}$ (where $L_{\rm h} = (L_{\rm epi} - W_{\rm E})/2$ is the collector maximum horizontal depletion width), the SCRs have both vertical and horizontal components, the horizontal current flow is confined in a thin layer of width $W_{\rm DEFP}$, and the vertical and the horizontal current flow areas are $L_{\rm E} \times W_{\rm E}/2$ and $L_{\rm E} \times W_{\rm EFPT}$, respectively. We can write down the following formula directly:

$$R_{\rm C} = \begin{cases} \dfrac{\rho L_{\rm h}}{L_{\rm E} W_{\rm epi}}, & 0 \le x_1 + x_2 \le W_{\rm epi}, \\ \dfrac{\rho(L_{\rm h} - L_{\rm DEFP})}{L_{\rm E} W_{\rm epi}} + \dfrac{\rho L_{\rm DEFP}}{L_{\rm E}(W_{\rm epi} - W_{\rm DEFP})}, & W_{\rm epi} \le x_1 + x_2 \le L_{\rm h} + W_{\rm epi}, \end{cases} \tag{4}$$

where $W_{\rm DEFP}$ depends on the current flow path in the horizontal mode and is considered to be a constant at the first order approximation, because it depends on the extrinsic collector–base SCR in the punch through mode.[7] The $L_{\rm DEFP}$ is the horizontal depletion width. In Eq. (4), we assume the collector–base SCR extension has a first-vertical-later-horizontal behaviour and no horizontal depletion occurs before a full vertical depletion. The $\rho = 1/(q\mu_{\rm n}N_{\rm epi})$ is the resistivity of the collector. We can rewrite $R_{\rm C}$ to make it practical and smooth as

$$R_{\rm C} = \frac{\rho(L_{\rm h} - f(W_{\rm d} - W_{\rm epi}))}{L_{\rm E} W_{\rm epi}} + \frac{f(W_{\rm d} - W_{\rm epi})\rho}{L_{\rm E}(W_{\rm epi} - W_{\rm DEFP})}, \tag{5}$$

where $W_{\rm d} = x_1 + x_2$, $f(W_{\rm d} - W_{\rm epi})$ is a smooth function which evolves from 0 in the vertical mode to $W_{\rm d} - W_{\rm epi}$ $(= L_{\rm DEFP})$ in the horizontal mode. In this paper, we take the following function:

$$f(W_{\rm d} - W_{\rm epi}) = \varepsilon \ln(1 + {\rm e}^{(W_{\rm d} - W_{\rm epi})/\varepsilon}). \tag{6}$$

As shown in Fig. 4, in the positive substrate–collector bias case, the accumulation of electrons next to the collector–oxide interface causes a current flow path to the collector contact region resulting in the disappearance of the horizontal SCR. Therefore the collector resistance is just due to the depletion of the collector–base junction. The depletion width has a maximum value of $W_{\rm epi}$,

$$x_1 = \begin{cases} \sqrt{\dfrac{2\varepsilon_{\rm Si}(V_{\rm CB} + V_{\rm dc})}{qN_{\rm epi}}}, & x_1 \le W_{\rm epi}, \\ W_{\rm epi}, & x_1 > W_{\rm epi}. \end{cases} \tag{7}$$

A smooth and soft transition from $x_1$ to $W_{\rm epi}$ is

$$W_{\rm d} = \begin{cases} \dfrac{x_1 W_{\rm epi}}{\sqrt{x_1^2 + W_{\rm epi}^2}}, & x_1 \le W_{\rm epi}, \\ W_{\rm epi}, & x_1 > W_{\rm epi}. \end{cases} \tag{8}$$

The vertical current flow area is $L_{\rm E} \times W_{\rm E}/2$. The collector resistance can be obtained as

$$R_{\rm C} = \rho(W_{\rm epi} - W_{\rm d})/(0.5 W_{\rm E} L_{\rm E}). \tag{9}$$

It is noted from Eq. (9) that the evolution of the collector resistance from the depletion to the accumulation mode is abrupt, which is not true in practice. We introduce another smooth function

$$R_{\rm C} = f'(V_{\rm SC})\rho(W_{\rm epi} - W_{\rm d})/(0.5 W_{\rm E} L_{\rm E}) + (1 - f'(V_{\rm SC}))\rho L_{\rm h}/(L_{\rm E} W_{\rm epi}), \tag{10}$$

where $f'(V_{\rm SC})$ is a smooth function which evolves from 0 at the bias $V_{\rm SC} = 0$ to 1 at the bias $V_{\rm SC} = 20$. As the collector resistance drops fast initially and slowly later with the increase of $V_{\rm SC}$, the following trigonometric function is used:

$$f'(V_{\rm SC}) = \sin(V_{\rm SC}\pi/40). \tag{11}$$

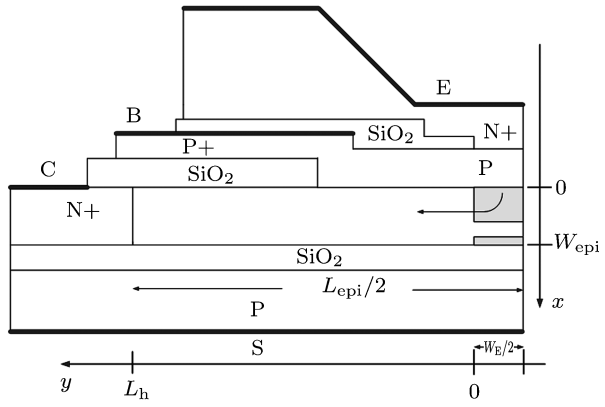



**Fig. 2.** Sketch of electron flow path in partially depleted operation mode.

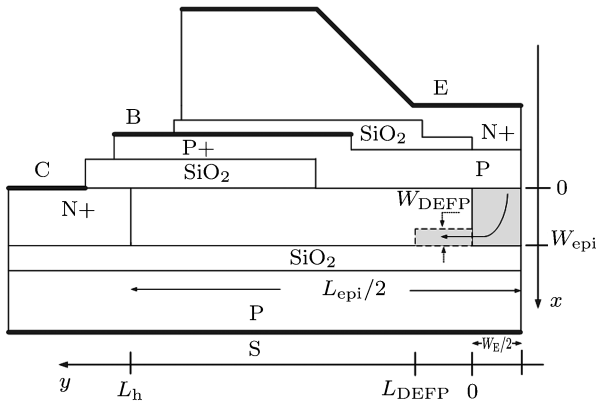



**Fig. 3.** Sketch of electron flow path in fully depleted operation mode.

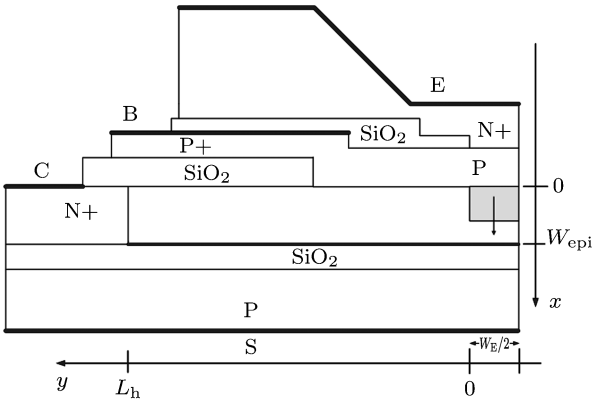



**Fig. 4.** Sketch of electron flow path in accumulation operation mode.

The collector transit time represents excess delay induced by the collector depletion capacitance and the series resistance. Variations of the collector resistance would cause variations of the transit frequency. As the transit frequency is influenced by many other factors, such as the base transit time and the collector capacitance, whereas these factors of an SOI HBT are quite different from those of a bulk counterpart, we just analyze the transit frequency qualitatively.

## 3. Illustrations and discussion

To show the validity of the proposed model, the calculated collector resistance is compared to the result of the two-dimensional simulation tool ISE TCAD, with a collector width $W_{\rm epi} = 160$ nm, a collector length $L_{\rm epi} = 1200$ nm, a collector doping concentration $N_{\rm epi} = 1.0 \times 10^{17}$ cm$^{-3}$, a base width $W_{\rm B} = 50$ nm, a base length $L_{\rm B} = 200$ nm, a base doping concentration $2 \times 10^{18}$ cm$^{-3}$, an oxide width $T_{\rm ox} = 140$ nm and an emitter size of 0.16 μm×0.6 μm. We apply the bias voltages $V_{\rm BE} = 0.8$ V, $V_{\rm CE} = 1.0$ V and get $R_{\rm C}$ values directly from the $I$–$V$ results.

Figure 5 shows the substrate effect by plotting the collector resistance as a function of the substrate collector voltage. The model is applied to the other half side. A kink occurs at zero bias, which is the transition point from the depletion mode to the accumulation mode. The resistance decreases slowly and then rapidly with the increase of the substrate collector voltage. This is due to the depletion of the horizontal collector neural region for negative bias and disappearance of horizontal depletion region and appearance of low impedance current flow path for positive bias. The discrepancy is probably due to parasitic effects and smooth function induced errors. It should be noted that the variation tendency of the collector resistance is the same as that showed by the IBM group.[10]

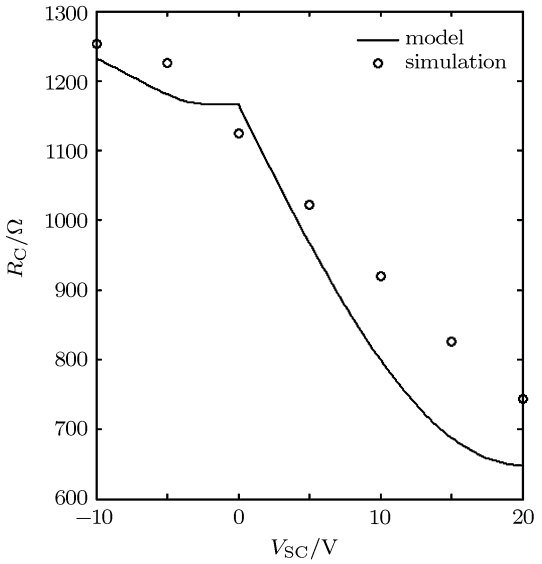



**Fig. 5.** The $R_{\rm C}$ as a function of $V_{\rm SC}$.

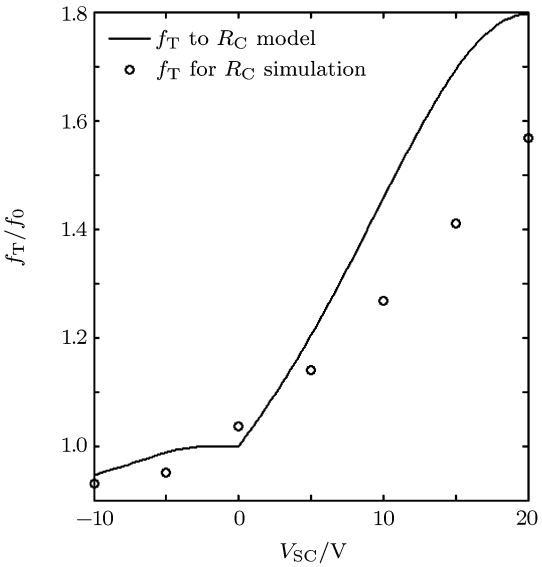



**Fig. 6.** Normalized transit frequency $f_{\rm T}/f_0$ as a function of $V_{\rm SC}$ considering collector resistance reduction effect only.

As the transit frequency is influenced by many factors, such as the base transit time and the collector capacitance, whereas these factors of an SOI HBT are quite different from that of a bulk counterpart, we just consider the effect of $R_{\rm C}$ to $f_{\rm T}$ qualitatively, neglecting other parameter variations. Figure 6 shows the corresponding normalized frequency $f_{\rm T}/f_0$ versus $V_{\rm SC}$, with $f_0$ defined as the corresponding transit frequency for the $R_{\rm C}$ model at zero substrate collector bias. It is found that substrate bias, especially positive bias, is beneficial to collector resistance reduction

and hence to the increase of the transit frequency. In this paper, the resistances are 1124 Ω and 743 Ω at the biases 0 V and 20 V, respectively, resulting in a 51% improvement of the transit frequency.

## 4. Conclusions

An analytical expression for the collector resistance of a novel vertical SiGe partially depleted HBT on thin SOI is obtained, considering both the vertical and the horizontal depletions. The resistance depends on the substrate bias and shows kinks with the increase of the substrate–collector bias from the depletion mode to the accumulation mode, which are quite different from those of a conventional bulk HBT. The model is consistent with the simulation result and the reported data and is useful to the frequency characteristic design of 0.13 μm millimeter-wave SiGe SOI BiCMOS devices.

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