Early effect modeling of silicon-on-insulator SiGe heterojunction bipolar transistors*

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Silicon germanium (SiGe) heterojunction bipolar transistor (HBT) on thin silicon-on-insulator (SOI) has recently been demonstrated and integrated into the latest SOI BiCMOS technology. The Early effect of the SOI SiGe HBT is analysed considering vertical and horizontal collector depletion, which is different from that of a bulk counterpart. A new compact formula of the Early voltage is presented and validated by an ISE TCAD simulation. The Early voltage shows a kink with the increase of the reverse base–collector bias. Large differences are observed between SOI devices and their bulk counterparts. The presented Early effect model can be employed for a fast evaluation of the Early voltage and is useful to the design, the simulation and the fabrication of high performance SOI SiGe devices and circuits.

Keywords: heterojunction bipolar transistor (HBT), SiGe, silicon-on-insulator, Early effect

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1. Introduction

Silicon germanium (SiGe) technology has matured to a stage where a superb state-of-the-art heterojunction bipolar transistor (HBT) with characteristic frequency at room temperature exceeding 400 GHz can be manufactured.[1] SiGe HBTs have emerged as one of the key components for millimeter wave applications, such as high speed communication systems at 60 GHz, automotive radar systems at 77 GHz, millimeter wave imaging systems at 94 GHz or higher, due to the great compatibility with the standard silicon process.[2] Unlike III/V semiconductor technologies, the SiGe exploits the same manufacturing steps as the silicon-based CMOS and allows analog, digital and millimeter wave functionalities to be integrated on a single chip. Silicon-on-Insulator (SOI) devices feature reduced parasitic capacitances, low leakage currents and improved immunities to substrate noise and crosstalk.[3] Therefore combining SiGe HBTs with the SOI technology, especially thin film SOI, is attractive for low power and high speed applications. Recently, a novel SiGe HBT with "folded collector" fabricated on thin CMOS-compatible SOI, first proposed by IBM,[4] has been integrated into the latest 0.13 μm millimeter wave SiGe SOI BiCMOS technology.[5] The devices show decent electrical performances, such as higher Early voltage and better trade-off between the base-collector avalanche breakdown voltage and the characteristic frequency.

As the SOI SiGe HBT has both vertical and horizontal current flow paths,[4] the change of the electrical behaviour makes the conventional model insufficient to describe the forward Early effect. The Early effect has a profound impact on device characteristics. The Early effect is due to variations in the width of the quasi-neutral base, which arise from a modulation of the base–collector depletion width. Changes in the capacitively stored junction charge cause changes in the output current, in the output conductance, in the base transit time, in the current gain and in the collector diffusion capacitance.

The forward Early effect of the device has been analysed qualitatively.[6] The researchers simplify the problem by neglecting the capacitance induced by the horizontal space charge expansion and propose an artificial Early voltage instead. Our investigations focus on understanding the unique features of the horizontal space charge region and their influences on the forward Early voltage. To our knowledge, the forward Early effect has not been theoretically and quantitatively

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studied. The aim of this paper is to develop an accurate yet relatively simple analytical expression for the conventional Early voltage. This paper is organized as follows. Section 2 provides information on the investigated transistor and briefly derives the employed models. In Section 3, device simulation results are compared to the calculation of the model. Furthermore, the observations are discussed. The results are summarized in Section 4.

2. Early voltage model for SOI SiGe HBTs

Figure 1 shows the sketch of a SiGe HBT on thin SOI with the definitions of dimension variables. The width of the collector is about 150 nm,[7] therefore the current flows vertically and makes a turn to the N+ collector contact region. The zero point of x axis is located at the base side edge of the base–emitter depletion region at zero bias and the zero point of y axis is located at the edge of the base. We restrict our analysis to the left half side of the device. A similar discussion applies to the other side.

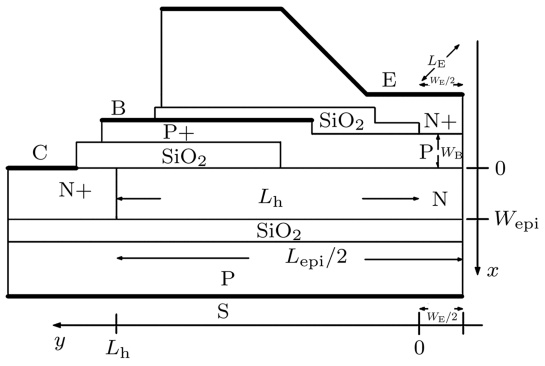


Fig. 1. Schematic diagram of a SiGe HBT on thin SOI.

Define $x' = x - W_{\rm B0}$, where $W_{\rm B0}$ is the quasi-neutral base width at zero bias. The Early voltage expression of a SiGe HBT can be obtained by partitioning the relative Gummel number $G_{\rm B}/G_{\rm B0}$ of the collector current and using the definition of the Early voltage, where $G_{\rm B} = \int_{-x'_{\rm E}}^{x'_{\rm C}} (N_{\rm B}(x')n_{\rm i0}^2/D_{\rm n}(x')n_{\rm i}^2(x'))\,{\rm d}x'$ and $G_{\rm B0} = \int_0^{W_{\rm B0}} (N_{\rm B}(x')n_{\rm i0}^2/D_{\rm n}(x')n_{\rm i}^2(x'))\,{\rm d}x'$ are the base Gummel numbers at arbitrary biases and at zero bias respectively, $D_{\rm n}$ is the minority carrier diffusion coefficient in the SiGe base, $N_{\rm B}$ is the base doping concentration, $n_{\rm i0}$ is the intrinsic carrier concentration of the un-doped Si, $n_{\rm i}(x')$ is the intrinsic doping of Ge. The $x'_{\rm E}$ ($x'_{\rm C}$) is the increase of the quasi-neutral base width due to a change in the emitter–base (collector–base) depletion layer width.[8,9]

$$V_{\rm EF}^{\rm eff} = G_{\rm B0}\left(\frac{\partial G_{\rm C}}{\partial V_{\rm BC}}\right)^{-1}\Bigg|_{V_{\rm BE}=0}, \tag{1}$$

where $G_{\rm C} = \int_{W_{\rm B0}}^{x'_{\rm C}} (N_{\rm B}(x')n_{\rm i0}^2/D_{\rm n}(x')n_{\rm i}^2(x'))\,{\rm d}x'$, $V_{\rm EF}^{\rm eff}$ is the effective forward Early voltage at zero bias, $V_{\rm BC}$ is the base–collector bias. The reverse collector–base bias will be denoted by $V_{\rm CB}$.

The intrinsic carrier concentration of SiGe is $n_{\rm i}^2 = (N_{\rm C}N_{\rm V})_{\rm SiGe}\exp[-E_{\rm g}/(kT)]$, where $(N_{\rm C}N_{\rm V})_{\rm SiGe}$ is the Ge-induced change including both the conduction and the valence band effective density-of-states, k and T are the Boltzmann constant and the absolute temperature, respectively. Neglecting the effect of doping induced bandgap narrowing, we obtain $E_{\rm g}(z,T) = E_0(T) - 0.96z + 0.43z^2 - 0.17z^3$ (eV),[10] where z is the Ge fraction, $E_{\rm g}$ is the energy difference between the lowest conduction band edge and the highest valence band edge for the alloy layer (strained $Si_{1-x}Ge_x$ grows on an unstrained Si layer) and $E_0(T)$ is the bandgap of the bulk Si (1.17 eV at 90 K or 1.12 eV at room temperature). We are looking for a reasonably simple but adequately accurate formula. Hence we assume the Ge doping in the base is linear, the base doping concentration is a constant, the diffusion coefficient is a constant and the third order component of $E_{\rm g}$ is negligible. We can then write

$$n_{\rm i}^2 = A\exp\left(\eta\frac{x'}{W_{\rm B0}} - 0.47kT\eta^2\frac{x'^2}{W_{\rm B0}^2}\right), \tag{2}$$

$$A = (N_{\rm C}N_{\rm V})_{\rm SiGe}\exp\left(-\frac{E_0(T)}{kT}\right), \tag{3}$$

where $\eta = 0.96(z_{W_{\rm B0}} - z_0)/(kT)$, $z_{W_{\rm B0}}$ and z_0 are the Ge fractions at $x' = W_{\rm B0}$ and $x' = 0$, respectively. In practice, the bandgap change within $[W_{\rm B0},\ x'_{\rm C}]$ is negligible. Substituting Eqs. (2) and (3) into Eq. (1) and evaluating the collector–base depletion charge by a capacitance $C_{\rm jC}$, we obtain,

$$V_{\rm EF}^{\rm eff} = \frac{\int_0^1 \exp(-\eta x' + 0.47kT\eta^2 x'^2)\,{\rm d}x'}{\exp(-\eta + 0.47kT\eta^2)}\frac{Q_{\rm B0}}{C_{\rm jC}}, \tag{4}$$

where $Q_{\rm B0} = qW_{\rm E}L_{\rm E}N_{\rm B}W_{\rm B0}$ is the base charge at zero bias. The integral $\int_0^1 \exp(-x'^2)\,{\rm d}x'$ can be evaluated approximately by the trapezoidal method, which is equal to 0.746. If the second order component of $E_{\rm g}$ is also neglected, the forward Early voltage of a bulk HBT is simplified to

$$V_{\rm EF}^{\rm eff} = \frac{1-\exp(-\eta)}{\eta\exp(-\eta)}\frac{Q_{\rm B0}}{C_{\rm jC}}. \tag{5}$$

The "folded collector" of the SOI HBT makes the collector capacitance different from that of a bulk counterpart. The behaviour of the device is analysed

to get a collector depletion width model and hence to obtain a final formula for the collector capacitance.

The base–collector space charge region (SCR) expansion is vertical at $V_{\rm CB} = 0$ V while lateral at higher reverse bias for a partially depleted HBT. The SCR expansion is lateral at $V_{\rm CB} = 0$ V for a fully depleted HBT. We focus on the former case just because the latter case can be described by conventional models.

According to the HICUM model,[11] the effective vertical punch through voltage is expressed as $V_{\rm jPC} = (qN_{\rm epi}/2\varepsilon_{\rm Si})W_{\rm epi}^2 - V_{\rm dc}$, where $V_{\rm dc} = V_{\rm T}\ln(N_{\rm epi}^2/n_{\rm i}^2)$ is the built in potential, $N_{\rm epi}$ and $W_{\rm epi}$ are the collector doping concentration and the collector width, respectively, $\varepsilon_{\rm Si}$ is the dielectric coefficient of Si, $V_{\rm T}$ is the thermodynamic potential. If $V_{\rm CB} \leq V_{\rm jPC}$, the collector SCR extends vertically; if $V_{\rm CB} > V_{\rm jPC}$, the collector SCR reaches the Si/SiO_2 interface and begins to extend horizontally.

In the case $V_{\rm CB} \leq V_{\rm jPC}$, the collector is partially depleted and the depletion is generated in the intrinsic collector region. We solve the one-dimensional Possion's equation and obtain the vertical depletion width $\bar{x}$ with the assumption of an abrupt base–collector junction

$$\bar{x} = \sqrt{\frac{2\varepsilon_{\rm Si}(V_{\rm CB} + V_{\rm dc})}{qN_{\rm epi}}}. \tag{6}$$

In the case $V_{\rm CB} > V_{\rm jPC}$, $\bar{x}$ is equal to $W_{\rm epi}$, the collector is fully depleted and the excess voltage falls on the collector's horizontal depletion region. We apply the Possion's equation horizontally with boundaries $E(\bar{y}) = 0$, where E is the electric field, $\bar{y}$ is the horizontal depletion length and $-\int_0^{\bar{y}} E(\bar{y})\,{\rm d}\bar{y} = V_{\rm CB} - V_{\rm jPC}$ and obtain

$$\bar{y} = \sqrt{\frac{2\varepsilon_{\rm Si}(V_{\rm CBi} - V_{\rm jPCi})}{qN_{\rm epi}}}. \tag{7}$$

In summary, the vertical and the horizontal space charge region widths for a partially depleted HBT are given by

$$\bar{x} = \begin{cases} \sqrt{\dfrac{2\varepsilon_{\rm Si}(V_{\rm CB} + V_{\rm dc})}{qN_{\rm epi}}}, & 0 \leq V_{\rm CB} \leq V_{\rm jPC}, \\ W_{\rm epi}, & V_{\rm CB} > V_{\rm jPC}, \end{cases} \tag{8}$$

$$\bar{y} = \begin{cases} 0, & 0 \leq V_{\rm CB} \leq V_{\rm jPC}, \\ \sqrt{\dfrac{2\varepsilon_{\rm Si}(V_{\rm CB} - V_{\rm jPC})}{qN_{\rm epi}}}, & V_{\rm CB} > V_{\rm jPC}. \end{cases} \tag{9}$$

In practice, the horizontal collector current is confined in a thin film as $V_{\rm CB} > V_{\rm jPC}$, with the width $W_{\rm DEFP}$ smaller than the collector width $W_{\rm epi}$, as shown in Fig. 2. The corresponding vertical and horizontal collector depletion charges are $Q_{\rm jCv} = 0.5qN_{\rm epi}L_{\rm E}W_{\rm E}\bar{x}$ and $Q_{\rm jCh} = qN_{\rm epi}L_{\rm E}W_{\rm DEFP}\bar{y}$, where $0.5L_{\rm E}W_{\rm E}$ and $L_{\rm E}W_{\rm DEFP}$ are the emitter area and the horizontal collector depletion region area of the left half of the device, respectively. Therefore the vertical and the horizontal collector depletion capacitance $C_{\rm jCv}$ and $C_{\rm jCh}$ can be obtained as

$$C_{\rm jCv} = \begin{cases} \dfrac{C_{\rm jC0}}{(V_{\rm CB}/V_{\rm dc} + 1)^{1/2}}, & 0 < V_{\rm CB} \leq V_{\rm jPC}, \\ \varepsilon_{\rm Si}/{\rm W}_{\rm epi}, & V_{\rm jPC} < V_{\rm CB}, \end{cases} \tag{10}$$

$$C_{\rm jCh} = \begin{cases} 0, & 0 < V_{\rm CB} \leq V_{\rm jPC}, \\ \dfrac{\alpha C_{\rm jC0}}{\left(\dfrac{V_{\rm CB}}{V_{\rm dc}} - \dfrac{V_{\rm jPC}}{V_{\rm dc}}\right)^{1/2}}, & V_{\rm jPC} < V_{\rm CB}, \end{cases} \tag{11}$$

where $C_{\rm jC0} = W_{\rm E}L_{\rm E}(qN_{\rm epi}\varepsilon_{\rm Si}/(2V_{\rm dc}))^{1/2}$ is the zero bias collector depletion capacitance. The $\alpha = W_{\rm DEFP}L_{\rm E}/(0.5W_{\rm E}L_{\rm E}) = W_{\rm DEFP}/(0.5W_{\rm E})$ is a weighting factor and can be considered as a constant at the first order approximation since it depends on the extrinsic base–collector SCR in the punch through mode.[12] The vertical capacitance can be regarded as $\varepsilon_{\rm Si}/W_{\rm epi}$ in full depletion cases. From a physical modeling point of view, the whole collector depletion capacitance $C_{\rm jC}$ is the series of vertical and horizontal parts. It should be noted that the collector depletion capacitance of the right half is similar to that of the left half and has the same expressions. Therefore, the $C_{\rm jC}$ is expressed as $2/(1/C_{\rm jCv} + 1/C_{\rm jCh})$, where 2 accounts for both the left half and the right half contributions and is given by

$$C_{\rm jC} = \begin{cases} \dfrac{2C_{\rm jC0}}{(V_{\rm CB}/V_{\rm dc} + 1)^{1/2}}, & 0 < V_{\rm CB} \leq V_{\rm jPC}, \\ \dfrac{2}{\dfrac{W_{\rm epi}}{\varepsilon_{\rm Si}} + \dfrac{(V_{\rm CB}/V_{\rm dc} - V_{\rm jPC}/V_{\rm dc})^{1/2}}{\alpha C_{\rm jC0}}}, & V_{\rm jPC} < V_{\rm CB}. \end{cases} \tag{12}$$

Substituting Eq. (12) to Eq. (5), the final expression for the forward Early voltage of a partially depleted SOI SiGe HBT with an abrupt base–collector junction is obtained

$$V_{\rm EF}^{\rm eff}=\begin{cases}\dfrac{1-\exp(-\eta)}{2\eta\exp(-\eta)}\dfrac{Q_{\rm B0}(V_{\rm CB}/V_{\rm dc}+1)^{1/2}}{C_{\rm jC0}}, & 0<V_{\rm CB}\leq V_{\rm jPC},\\ \dfrac{1-\exp(-\eta)}{2\eta\exp(-\eta)}Q_{\rm B0}\left(\dfrac{W_{\rm epi}}{\varepsilon_{\rm Si}}+\dfrac{(V_{\rm CB}/V_{\rm dc}-V_{\rm jPC}/V_{\rm dc})^{1/2}}{\alpha C_{\rm jC0}}\right), & V_{\rm jPC}<V_{\rm CB}.\end{cases} \tag{13}$$

It is apparent that the Early voltage in the model shows a kink at the transition point.

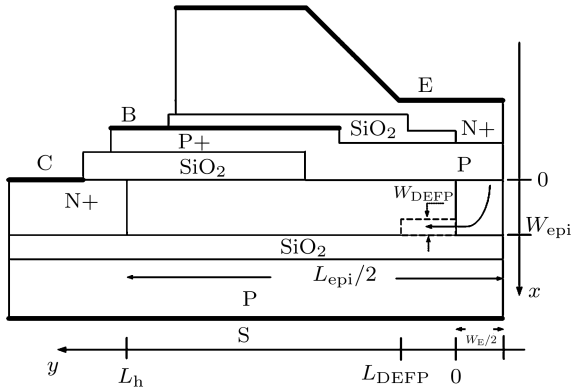


Fig. 2. Schematic diagram of electron flow path for the fully depleted operation mode.

3. Verification and discussion

The model established above is verified by a two-dimensional simulation using ISE TCAD with graded Ge content, while the constant Ge case is a special case with zero gradient. For experimental convenience, the forward Early voltage is normally written as $I_{\rm C}/(\partial I_{\rm C}/\partial V_{\rm CB})$.

First, the forward Early voltage model of a bulk SiGe HBT given by Eq. (4) and the simplified form given by Eq. (5) are compared to the simulation with emitter doping concentration 5×10^{19} cm^{-3}, base doping concentration 2×10^{18} cm^{-3}, collector doping concentration 1×10^{17} cm^{-3}, Ge doping profile linEarly graded up from 10% at the emitter–base junction side to 22% at the collector–base junction side and base width of 40 nm. The Ge induced bandgap narrowing model is implemented and the base–emitter bias is 0.85 V.

Figure 3 shows the forward Early voltage versus $V_{\rm CB}$ for linEarly graded Ge. The forward Early voltage increases with the increase of $V_{\rm CB}$. Discrepancies between the proposed model and the simulation at low biases and large biases are observed. The former is due to weak electron extraction capability of small electric field, the latter is probably due to the high injection effect. It is observed from the figure that the proposed model given by Eq. (4) and the simplified form given in Eq. (5) coincide with each other. In fact, the deviation is less than 1%. The simulation agrees wells with the model given by Eq. (5). The SPICE–Gummel–Poon (SGP) model $Q_{\rm B0}/C_{\rm jC}$ is drawn. Apparently the SGP model is insufficient to describe the SiGe HBT with graded Ge.

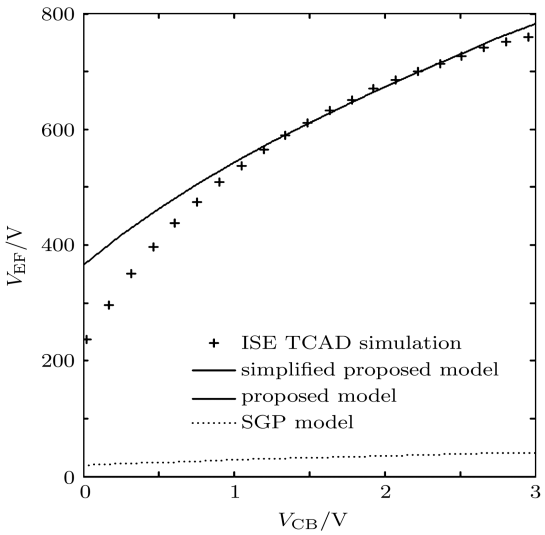


Fig. 3. Relation between the forward Early voltage and the collector–base junction voltage for a bulk SiGe HBT.

Then, the forward Early voltage model of an SOI SiGe HBT is compared to the simulation, where a 0.2 μm × 1 μm transistor with emitter doping concentration 1×10^{20} cm^{-3}, base doping concentration 3×10^{18} cm^{-3}, collector doping concentrations 1×10^{17} cm^{-3} and 2×10^{17} cm^{-3}, 10% (22%) Ge at the emitter (collector) side and base width of 35 nm is modeled and simulated.

Figures 4 and 5 present the results of the base–collector capacitance and the forward Early voltage versus reverse base–collector bias. The symbols repre-

sent results from the simulation and the lines represent results from the numerical calculation. The kink occurs in a transition from the vertical operation mode to the horizontal operation mode. As the collector doping dose increases, the device is harder to deplete, which causes a larger vertical punch through voltage and hence leads to the delay of the kink. In the case $V_{\rm CB} > V_{\rm jPC}$, large differences are observed between the SOI HBT and the corresponding bulk device. This is because the collector SCR of the former extends horizontally and forms the series of vertical and horizontal capacitances. The excess electric field on horizontal depletion region has a limited effect on the collector current, therefore a more stable collector current is generated and a larger Early voltage is predicted. While the latter continues to deplete vertically due to a much thicker collector width. As can be seen,

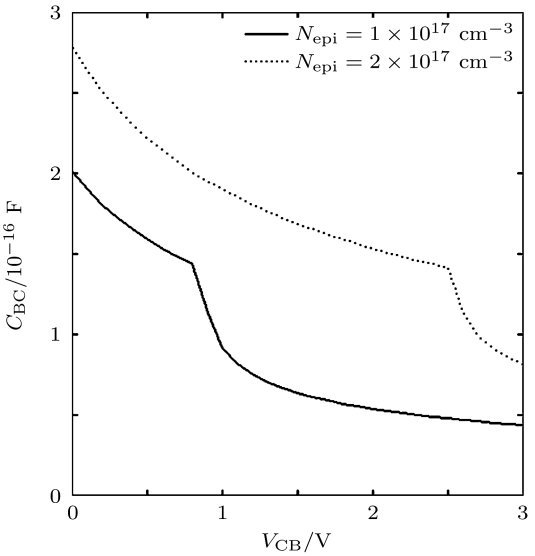


Fig. 4. The base–collector depletion capacitance $C_{\rm BC}$ versus $V_{\rm CB}$ for SOI SiGe HBTs with different collector doping doses.

the proposed model is consistent with the simulation result. The deviation around $V_{\rm jPC}$ is mainly due to the two dimensional extension of the collector SCR as $V_{\rm CB}$ approaches $V_{\rm jPC}$.

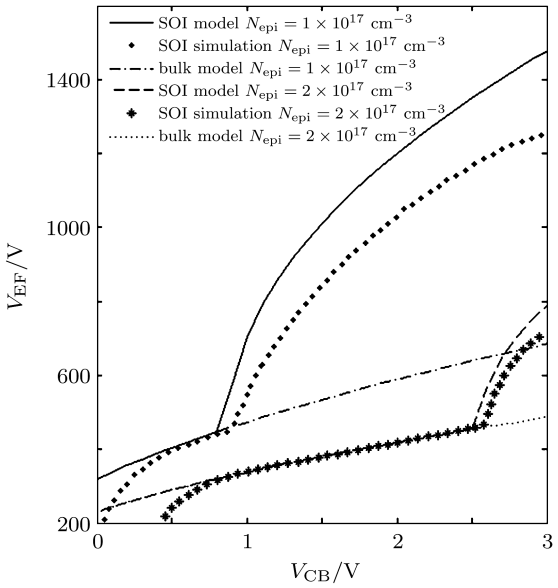


Fig. 5. The $V_{\rm EF}$ versus $V_{\rm CB}$ for SOI SiGe HBTs with different collector doping doses.

4. Conclusions

The Early effect of an SOI SiGe HBT is analysed considering vertical and horizontal collector depletion which is different from that of a bulk counterpart. A new compact formula for the Early voltage is presented and validated by an ISE simulation. The Early voltage shows a kink with the increase of the reverse base–collector bias. Large differences are observed between SOI devices and their bulk counterparts. The presented Early effect model can be employed for a fast evaluation of the Early voltage and is useful to the design, the simulation and the fabrication of high performance SOI SiGe devices and circuits.

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