Numerical study on the dependence of ZnO thin-film transistor characteristics on grain boundary position*

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(Received 15 November 2010; revised manuscript received 4 January 2011)

The dependence of transistor characteristics on grain boundary (GB) position in short-channel ZnO thin film transistors (TFTs) has been investigated using two-dimensional numerical simulations. To simulate the device accurately, both tail states and deep-level states are taken into consideration. It is shown that both the transfer and output characteristics of ZnO TFTs change dramatically with varying GB position, which is different from polycrystalline Si (poly-Si) TFTs. By analysing the mechanism of the carrier transportation in the device, it is revealed that the dependence is derived from the degrees of carrier concentration descent and mobility variation with GB position.

Keywords: grain boundary, ZnO thin film transistors, trap states, simulation

PACS: 72.80.Ey, 73.40.Qv, 85.30.Tv **DOI:** 10.1088/1674-1056/20/5/057201

1. Introduction

Recently, ZnO thin film transistors (TFTs) have attracted much attention due to their unique properties such as low preparation temperature, less light sensitivity and high field effect mobility. Furthermore, impressive progress has been made towards the ultimate goal of realizing reliable electronic performance in practical semiconductors.[1−3] However, one limitation to a larger exploitation of ZnO TFTs comes from the notable variance of their individual characteristics for the polycrystalline structure of ZnO thin film. Another obstacle for further development and utilization of ZnO TFTs is the poor knowledge of the microscopic charge transport processes in the devices.

Modeling and clarifying the primary conduction mechanisms in TFTs are crucial requirements before high-quality devices can be produced. Still, despite the significant boost in device fabrication, there are only a limited number of publications related to the numerical simulation of the ZnO TFTs.[4−7] Previous studies have examined the grain boundaries (GBs) number's effect on ZnO TFTs performance and demonstrated that GB potential height could be modulated by gate bias. However, in all these models, only the deep-level traps in GBs were considered. Recent research advocated that there were also tail states in GBs due to intrinsic structural disorder in the grains for ZnO TFTs.[8] On the other hand, in order to obtain high performance devices, the number of GBs should be cut down, which can be achieved by increasing grain size and/or scaling down device dimensions. As reported by Kashiwaba *et al.*, the grain size of ZnO thin films could reach above 200 nm.[9] The device dimensions became smaller and smaller with technical progress.[10] Simulated researches on the position of single GB for poly-Si TFTs showed that, for both transfer and output characteristics, drain current degradation was smaller when the GB was near the drain edge, while the degradation was larger and kept in almost the same level when the GB was located elsewhere.[11,12] Due to the wide band gap of ZnO and the existence of deep-level traps in GBs, the GB potential barrier height modulation by gate bias for ZnO TFTs is different from that of poly-Si TFTs.[5] Therefore, it is important to study the dependence of ZnO TFTs characteristics on GB position, particularly when channel length is comparable to the grain size.

The object of this work is to use a physically-based two-dimensional simulator ATLAS (see Atlas

*Project supported by the National Natural Science Foundation of China (Grant No. 50872112) and NPU Foundation for Fundamental Research, China (Grant No. JC201017).

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User's Manual Silvaco International 2008) as a tool to investigate the effects of comprehensive GB trap states on ZnO-TFT at different positions and to determine the mechanism of the carrier transportation across the GB at different positions in ZnO TFTs.

2. Model and simulation

2.1. Modeling of GB trap states

The electronic characteristics of semiconductor devices are simulated by solving the Poisson equation and the continuity equation. In polycrystalline semiconductor, as the carriers are captured by GB trap states, the trap model at GBs is included in the right-hand side of the Poisson equation by adding trapped net carrier density $N_{\rm T}$,[13]

$$\mathrm{div}(\varepsilon\nabla\psi) = q(n - p + N_{\rm A}^{+} - N_{\rm D}^{+} + N_{\rm T}), \quad (1)$$

$$N_{\rm T} = n_{\rm T} - p_{\rm T}, \quad (2)$$

where n and p are electron and hole concentrations, $N_{\rm D}^{+}$ and $N_{\rm A}^{+}$ are ionized donor and accepter concentration, and $n_{\rm T}$ and $p_{\rm T}$ are trapped electron and hole density respectively. Because of the inherent defects such as oxygen vacancy and interstitial zinc,[14,15] ZnO is always an intrinsic n-type semiconductor (i.e. $N_{\rm A}^{+} = 0$).

The electron and hole concentrations are expressed as

$$n = N_{\rm C}\exp\left(\frac{E_{\rm F} - E_{\rm C}}{kT_{\rm L}}\right), \quad (3)$$

$$p = N_{\rm V}\exp\left(\frac{E_{\rm V} - E_{\rm F}}{kT_{\rm L}}\right), \quad (4)$$

where $E_{\rm F}$ is Fermi energy level , k is Boltzmann constant, $T_{\rm L}$ is the lattice temperature, $E_{\rm C}$ and $E_{\rm V}$ are conduction band and valence band energy level; and $N_{\rm C}$ and $N_{\rm V}$ are the effective density of states for electrons in the conduction band and the one for holes in the valence band, which can be calculated by using

$$N_{\rm C} = \left(\frac{2\pi m_{\rm e}^{*} kT_{\rm L}}{h^2}\right)^{3/2}, \quad (5)$$

$$N_{\rm V} = \left(\frac{2\pi m_{\rm h}^{*} kT_{\rm L}}{h^2}\right)^{3/2}, \quad (6)$$

where $m_{\rm e}^{*}$ and $m_{\rm h}^{*}$ are effective masses of electron and hole respectively and h is Planck constant.

The ionized donor density is usually expressed as

$$N_{\rm D}^{+} = \frac{N_{\rm D}}{1 + \exp\left[(E_{\rm F} - E_{\rm D})/kT_{\rm L}\right]}, \quad (7)$$

where $N_{\rm D}$ and $E_{\rm D}$ are the donor density and its corresponding energy level.

The trap state at the GB is separated into two classes: donor-like trap state and acceptor-like trap state. Donor-like trap states are positively charged when unoccupied and therefore can capture electrons. Conversely, acceptor-like trap states are negatively charged when unoccupied and therefore can capture holes (i.e. emit electrons). The probability of the states occupied will be varied in different state energy level, so the trapped electron and hole densities can be calculated by the integral operation as

$$n_{\rm T} = \int_{E_{\rm V}}^{E_{\rm C}} g_{\rm D}(E) f_{\rm D}(E)\mathrm{d}E, \quad (8)$$

$$p_{\rm T} = \int_{E_{\rm V}}^{E_{\rm C}} g_{\rm A}(E) f_{\rm A}(E)\mathrm{d}E, \quad (9)$$

where $g_{\rm D}(E)$ and $g_{\rm A}(E)$ are the density of donor-like and acceptor-like trap states and $f_{\rm D}(E)$ and $f_{\rm A}(E)$ are the occupation probability for donor-like and acceptor-like traps respectively.

Taking into account the existence of exponentially distributed tail state near the conduction (donor-like) and the valence (acceptor-like),[8,16] and the two deep level states with Gaussian distribution (one donor-like and the other acceptor-like),[4,17] the final density of states (DOS) was modeled as

$$g_{\rm D} = N_{\rm TD}\exp\left(\frac{E_{\rm V} - E}{W_{\rm TD}}\right) + N_{\rm GD}\exp\left[-\left(\frac{E - E_{\rm MD}}{\mathrm{W}_{\rm GD}}\right)^2\right], \quad (10)$$

$$g_{\rm A} = \mathrm{N}_{\rm TA}\exp\left(\frac{E - E_{\rm C}}{W_{\rm TA}}\right) + N_{\rm GA}\exp\left[-\left(\frac{E_{\rm MA} - E}{W_{\rm GA}}\right)^2\right], \quad (11)$$

where the DOS for exponential tail distribution is described by its valence and conduction band edge intercept densities ($N_{\rm TD}$ and $N_{\rm TA}$) and by its characteristic decay energy ($W_{\rm TD}$ and $W_{\rm TA}$); and the DOS for Gaussian distributions is described by its total donor-like and acceptor-like density of states ($N_{\rm GD}$ and $N_{\rm GA}$) and by its characteristic decay energy ($W_{\rm GD}$ and $W_{\rm GA}$) and its peak energy ($E_{\rm MD}$ and $E_{\rm MA}$). E is the trap energy level. Normally, the total donor-like trap states and acceptor-like trap states are the same in quantity.[18]

The occupation probabilities are given by

$$f_{\rm D} = \frac{v_{\rm p}\sigma_{\rm dh}p + v_{\rm n}\sigma_{\rm de}n_{\rm t}}{v_{\rm n}\sigma_{\rm de}(n + n_{\rm t}) + v_{\rm p}\sigma_{\rm dh}(p + p_{\rm t})}, \quad (12)$$

$$f_{\rm A} = \frac{v_{\rm n}\sigma_{\rm ae}n + v_{\rm p}\sigma_{\rm ah}p_{\rm t}}{v_{\rm n}\sigma_{\rm ae}(n+n_{\rm t}) + v_{\rm p}\sigma_{\rm ah}(p+p_{\rm t})}, \quad (13)$$

where $v_{\rm n}$ and $v_{\rm p}$ are the electron thermal velocity and the hole thermal velocity and $\sigma_{\rm ae}$, $\sigma_{\rm ah}$, $\sigma_{\rm de}$ and $\sigma_{\rm dh}$ are electron and hole capture cross sections for acceptor-like traps and donor-like traps, respectively. The effective electron and hole concentrations $n_{\rm t}$ and $p_{\rm t}$ are given by

$$n_{\rm t} = n_{\rm i}\exp\left(\frac{E-E_{\rm Fi}}{kT_{\rm L}}\right), \quad (14)$$

$$p_{\rm t} = n_{\rm i}\exp\left(\frac{E_{\rm Fi}-E}{kT_{\rm L}}\right), \quad (15)$$

where $E_{\rm Fi}$ is intrinsic Fermi energy level and $n_{\rm i}$ is the intrinsic carrier concentration, which is given for Boltzmann statistics by

$$n_{\rm i} = \sqrt{N_{\rm C}N_{\rm V}}\exp\left[\frac{-(E_{\rm C}-E_{\rm V})}{2kT_{\rm L}}\right]. \quad (16)$$

2.2. Device structure and simulation parameters

The device for simulation is an n-type staggered bottom-gate TFT as shown in Fig. 1, which is the most popular type for practical manufacturing. The thicknesses of the undoped ZnO layer and gate SiO_2 layer are 50 and 100 nm respectively. The channel length is 400 nm and the contact length of the drain and source is 100 nm. In our model, there are no trap states located in the grain regions and ZnO–SiO_2 interface, but in the GB region. The grain and grain boundaries are considered to have the same semiconductor properties and the only difference is the presence of the trapping states in the grain boundary. Because the grain size is comparable to the channel length, we assume that only one GB exists in the channel and it is perpendicular to the channel. The width of the grain boundary is estimated at about 1 nm as in previous simulation studies.[4] More parameters of the material are taken from some other references,[8,19−22] as collected in Table 1.

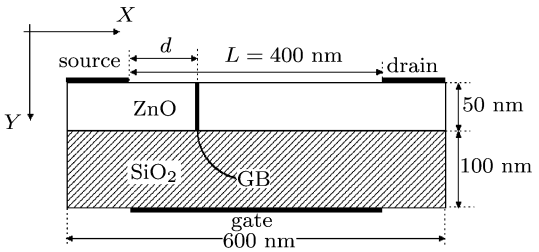


Fig. 1. Schematic of staggered bottom-gate structure of a ZnO TFT for simulation.

Table 1. Material parameters of ZnO used in the simulation.

Material parameters	Value
Lattice temperature, $T_{\rm L}$	300 K
Band gap, $E_{\rm g}(E_{\rm C}-E_{\rm V})$	3.4 eV
Effective mass of electron, $m_{\rm e}^*$	0.318 m_0
Effective mass of hole, $m_{\rm h}^*$	0.5 m_0
Donor concentration, $N_{\rm D}$	1×10^{16} cm^{-3}
Dielectric constant, $\varepsilon_{\rm s}$	8.12
Electron affinity, $\xi(E_{\rm vac}-E_{\rm C})$	4.29 eV
Work function, $\phi(E_{\rm vac}-E_{\rm F})$	4.45 eV
Electron thermal velocity, $v_{\rm n}$	3×10^5 m·s^{-1}
Hole thermal velocity, $v_{\rm p}$	1.5×10^5 m·s^{-1}
Density of acceptor-like and donor-like	
Tail states, $N_{\rm TA}$ and $N_{\rm TD}$	5×10^{18} cm^{-3}·eV^{-1}
Density of acceptor-like and donor-like	
Deep-level states, $N_{\rm GA}$ and $N_{\rm GD}$	1×10^{12} cm^{-3}·eV^{-1}
Characteristic decay energy acceptor-like and	
Donor-like tail states, $W_{\rm TA}$ and $W_{\rm TD}$	0.05 eV
Characteristic decay energy of acceptor-like and	
Donor-like deep-level states, $W_{\rm GA}$ and $W_{\rm GD}$	0.25 eV
Peak energy peak distribution of acceptor-like and	
Donor-like deep-level states, $E_{\rm MA}$ and $E_{\rm MD}$	1.7 eV
Capture cross section of electron and	
Hole states, $\sigma_{\rm ae}$, $\sigma_{\rm ah}$, $\sigma_{\rm de}$ and $\sigma_{\rm dh}$	4×10^{-15} cm^2

In the simulation, a GB position is defined to be at different distances from the source edge, i.e. $d = 20$, 100, 200, 300, 380 nm. The device with no GB is also simulated for comparison.

3. Results and discussion

Figure 2 shows the simulated transfer characteristics at the drain voltage $V_d = 0.5$ V (a), 2 V (b) and 8 V (c). It is clearly seen that the degradation occurs mainly in the sub-threshold region and becomes serious as the GB is close to the source edge, which is observed more clearly from the $\sqrt{I_d} - V_g$ curve. At higher V_d (2 V and 8 V), the GB close to the drain edge almost does not affect the drain current, although the GB near the source edge still reduces the drain current markedly. Similarly, the output characteristics as shown in Fig. 3 are also strongly dependent on the GB position.

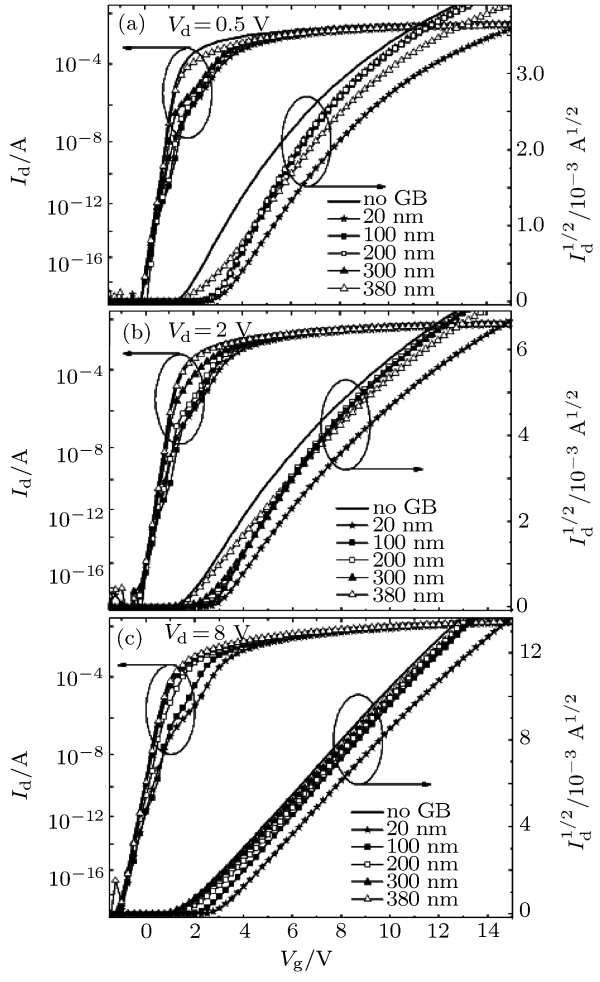


Fig. 2. Transfer characteristics of a modeled ZnO TFTs with a GB positioned at $d = 20$, 100, 200, 300 and 380 nm and with no GB under $V_d = 0.5$ V (a), 2 V (b) and 8 V (c).

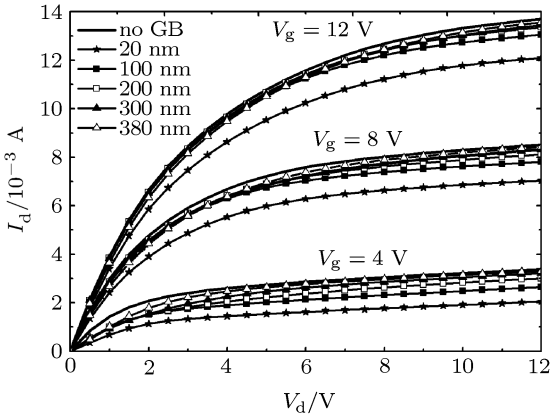


Fig. 3. Output characteristics of a modeled ZnO TFTs with a GB at $d = 20$, 100, 200, 300 and 380 nm and with no GB.

It is clearly shown that the depression of the drain current is serious when the GB is close to the source edge. Compared with poly-Si TFTs,[11] ZnO TFTs are more sensitive to GB positions. This is probably due to the GB potential height in ZnO devices that can be modulated by gate bias.

As mentioned above, the distinct dependence of ZnO TFTs characteristics on grain boundary position occurs mainly in the sub-threshold region for transfer characteristics and in the whole region for output characteristics. It is necessary to clarify how the GB at different positions affects the carrier transportation under different bias conditions. According to Levinson's theory,[23] free electrons are induced in the interface of the channel layer and insulation layer when a positive gate bias is applied in a polycrystalline semiconductor TFTs. On the other hand, there are a large number of trapping states in the GB, which lead to free electrons trapping and concentration declining near the GB. After trapping the free electrons, the traps become electrically charged, creating a potential energy barrier that impedes the motion of electron from one grain to another, thereby reducing their mobility.

As shown in Fig. 4(a), the free electron concentration drops seriously on the right-hand side of the GB and it keeps a low level in the rest part of the channel. In addition, the closer the GB to the drain, the less the free electron concentration drops. It is consistent with the result of Fig. 4(b), where the GB potential barrier height (V_B) is reduced when GB is closer to the drain. This result can be explained by Baccarani's model[24] that the GB potential barrier height is governed by trapped net carrier density N_T, carrier density per unit volume N_D in the grain and grain size l_g. The potential barrier height V_B is given by

$$V_B = \frac{qN_D l_g^2}{8\varepsilon_s}, \quad N_D l_g \leq N_T, \tag{17}$$

$$V_{\rm B} = \frac{qN_{\rm T}^2}{8\varepsilon_s N_{\rm D}}, \quad N_{\rm D} l_g \geq N_{\rm T}. \tag{18}$$

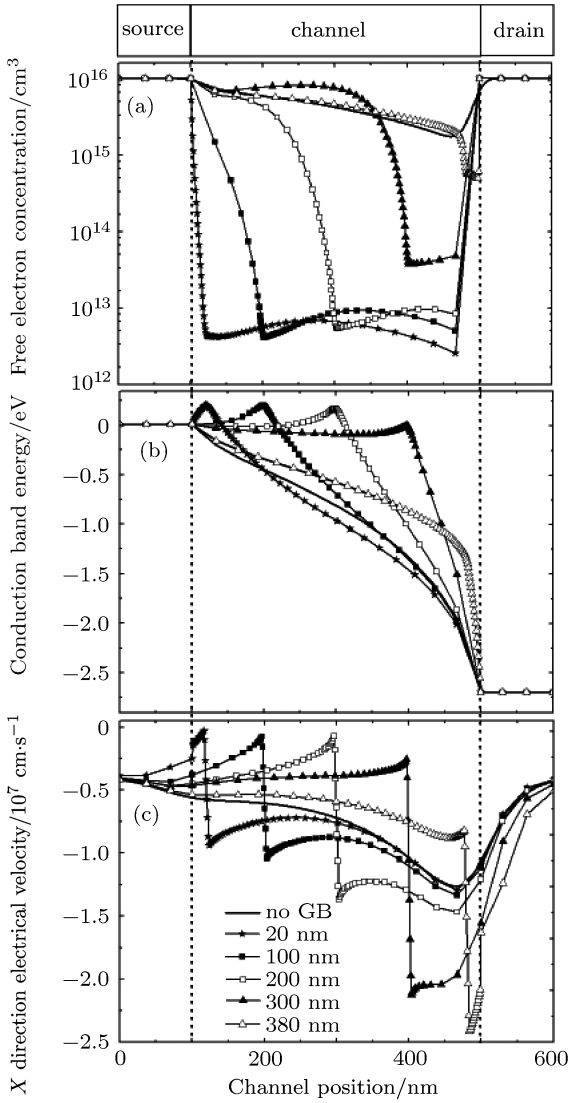


Fig. 4. Cross section of free electron concentration (a), conduction band energy (b) and X-direction electrical velocity (c) near the interface to the insulating layer for ZnO TFTs with GB positioned at d = 20, 100, 200, 300 and 380 nm and with no GB. The bias condition is $V_{\rm d}$ = 8 V and $V_{\rm g}$ = 2 V.

The calculated result indicates $N_D l_{\rm g} < N_{\rm T}$, which means that GB is not fully filled and the potential barrier height increases with the trapped net carrier density, resulting in the variation of $V_{\rm B}$ with the position of GB.

Figure 4(c) illustrates the X-direction electron velocity near the insulating layer. It is clear that the electrons in the device with no GBs are accelerated from source to drain under an applied positive drain bias. However, as the GB exists in the channel, the electrons motion is inhibited on both sides of the GB but accelerated in the GB region. Furthermore, the hindering effect is more serious when the GB is near the source edge, while the accelerating effect becomes more significant when the GB is near the drain edge. We believe that the phenomenon may be due to two major factors. On the one hand, the free electrons are trapped on both sides of the GB and the depletion region is created by the positively charged donor ions. The depletion region forms a potential barrier at the boundary to forbid the carriers mobility. The potential barrier height drops with the GB getting near the drain edge, so that the hindering effect is weakened. On the other hand, the applied electric filed intensity is higher in the GB region than in the grain. Moreover, the less the degree of trap occupancy is, the larger the applied electric field intensity is,[25] resulting in the electrons to be accelerated intensively in the GB region when GB is close to the drain edge.

4. Conclusion

The dependence of ZnO TFT characteristics on grain boundary position has been investigated using two-dimensional device simulation. The results indicate that in single GB short-channel ZnO TFTs, the closer the GB to the source edge is, the bigger the decline of drain current for both transfer and output characteristics is. The GB effect is minor when it is near the drain edge. By further analysis of the GB effects on the carrier transportation, it is found that this dependence originates from the capability of GB states trapping carriers, the height of the GB potential barrier and its effect on carriers' mobility.

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