Hot carrier injection degradation under dynamic stress*

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In this paper, we have studied hot carrier injection (HCI) under alternant stress. Under different stress modes, different degradations are obtained from the experiment results. The different alternate stresses can reduce or enhance the HC effect, which mainly depends on the latter condition of the stress cycle. In the stress mode A (DC stress with electron injection), the degradation keeps increasing. In the stress modes B (DC stress and then stress with the smallest gate injection) and C (DC stress and then stress with hole injection under $V_g = 0$ V and $V_d = 1.8$ V), recovery appears in the second stress period. And in the stress mode D (DC stress and then stress with hole injection under $V_g = -1.8$ V and $V_d = 1.8$ V), as the traps filled in by holes can be smaller or greater than the generated interface states, the continued degradation or recovery in different stress periods can be obtained.

Keywords: hot carrier injection, alternate stress, recovery, degradation

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1. Introduction

As the device dimensions are continuously shrunk with the rapid development of very large scale integration (VLSI), hot carrier injection (HCI) is becoming more and more serious, and has long been one of the most important reliability issues for metal oxide semiconductor field effect transistor (MOSFET) devices.[1−3] As the maximum of electric field is located in the drain region, the hot carrier injection can generate interface states at the Si/SiO_2 interface of near-drain region. After a long time, HCI will result in damage at the interface and lead to the degradation of the device. Several HCI degradation models have been proposed to accurately predict the lifetime of devices under operation voltage and their results coincided with experiment data well in a larger scale region.[2] However, when the device gets into ultra small scale, the results from the models proposed before deviate from the experiment data. Thus a new model is proposed to predict the degradation of the devices.

All these studies are related to the DC (direct current) stress, but there is no study on the degradation under dynamic stress. In circuits of real practice, devices always work under pulsed stress. Therefore, in this paper, we study the degradation of the device under different alternated stresses and obtain more details about the physical mechanisms.

2. Devices and experiments

The PMOSFETs used here are of surface channel. They were manufactured using a 90-nm process technology with lightly doped drain (LDD) structure and shallow trench isolation (STI) scheme. The gate oxides of all devices were annealed in N_2O atmosphere after thermal growth. The devices used here have an ultra-thin gate oxide thickness of 1.4 nm, gate width of 10 μm and gate length of 90 nm. Agilent B1500A, a high precision semiconductor parameter analyzer, was used to complete the tests. The experiments were conducted at room temperature.

3. Results and discussion

Figure 1 shows the relationship of gate current to the gate voltage from 0 V to 1.8 V under the drain voltage stress 1.8 V. From Fig. 1, we can see that the injection carrier varies with gate voltage changing. When the gate voltage has zero or small

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value, the main injection carrier is hole (hole injection), but when gate voltage is large it is electron (electron injection). Therefore, when the pulsed voltage stress with high level $V_g = 1.8$ V and low level $V_g = 0$ V as shown in Fig. 2 is applied to the gate with $V_{drain} = 1.8$ V, the injections under different conditions can be determined by this observation.[4,5] When the high level $V_g = 1.8$ V is applied, there should be electron injecting into the oxide corresponding to the point $V_g = V_d = 1.8$ V in Fig. 1. When the low level $V_g = 0$ V is applied, hole injection comes out corresponding to the point with $V_g = 0$ and $V_d = 1.8$ V in Fig. 1.

To study the effects under different injection conditions, the devices are subjected to different stress voltages shown in Table 1. Mode A is for DC stress with electron injection, mode B is for DC stress and then stress with the smallest gate injection, and modes C and D are for DC stress and then stresses with hole injection.[6−8] Each experiment lasts for 1.5 cycles, namely, 3000s.

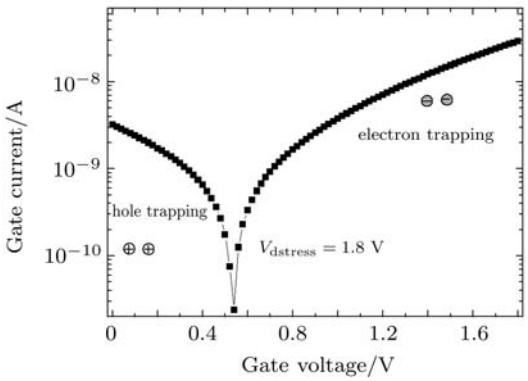


Fig. 1. Relationship of gate current to the gate voltage.

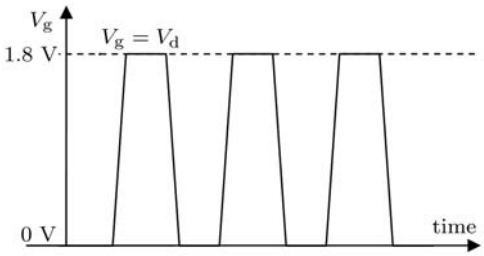


Fig. 2. Pulsed voltage stress with high level $V_g = V_d = 1.8$ V and low level $V_g = 0$ V.

Table 1. Parameter degradations of devices under alternation stresses.

stress condition ($V_s = V_{sub} = 0$ V)		degradation (after 3000s)/%			
		$\Delta G_{mlin}/G_{mlin0}$	$\Delta V_{th}/V_{th0}$	$\Delta I_{dsat}/I_{dsat0}$	$\Delta I_{dlin}/I_{dlin0}$
mode A	$V_g = V_d = 1.8$ V	20.86	17.79	13.05	18.65
mode B	$V_g = V_d = 1.8$ V —— $V_g = 0.5$ V, $V_d = 1.8$ V —— $V_g = V_d = 1.8$ V	15.21	13.17	8.70	13.9
mode C	$V_g = V_d = 1.8$ V —— $V_g = 0$ V, $V_d = 1.8$ V —— $V_g = V_d = 1.8$ V	16.51	12.76	8.81	14.21
mode D	$V_g = V_d = 1.8$ V —— $V_g = -1.8$ V, $V_d = 1.8$ V —— $V_g = V_d = 1.8$ V	25.32	27.05	16.32	23.94

The degradations of devices under different stress conditions are listed in Table 1. From Table 1 it follows that the degradation results of modes A, B and C are all smaller than those of D. Therefore, the degradation under alternating stress can be smaller or larger than that of DC stress. To study the degradation mechanism in detail, the degradations of threshold voltage, drain current and transconductance under different stress modes are shown in Fig. 3. All of them show similar tendencies. Therefore, we take the most typical parameter, the threshold voltage, as the analysed object to study the device damage under different stress modes.

In the first process, the devices are subjected to the stress with hot electron injection. The degradation mechanism in this process accords with the DC stress degradation rule as we mentioned before. In the second stress interval, the degradation trends are different under different stress conditions. As the degradation curves show recovery trends under the conditions of modes B and C, these stress conditions are called HC recovery stress conditions. Under the condition of mode D the degradation increases with stressing time, so the stress condition is HC enhanced stress condition.

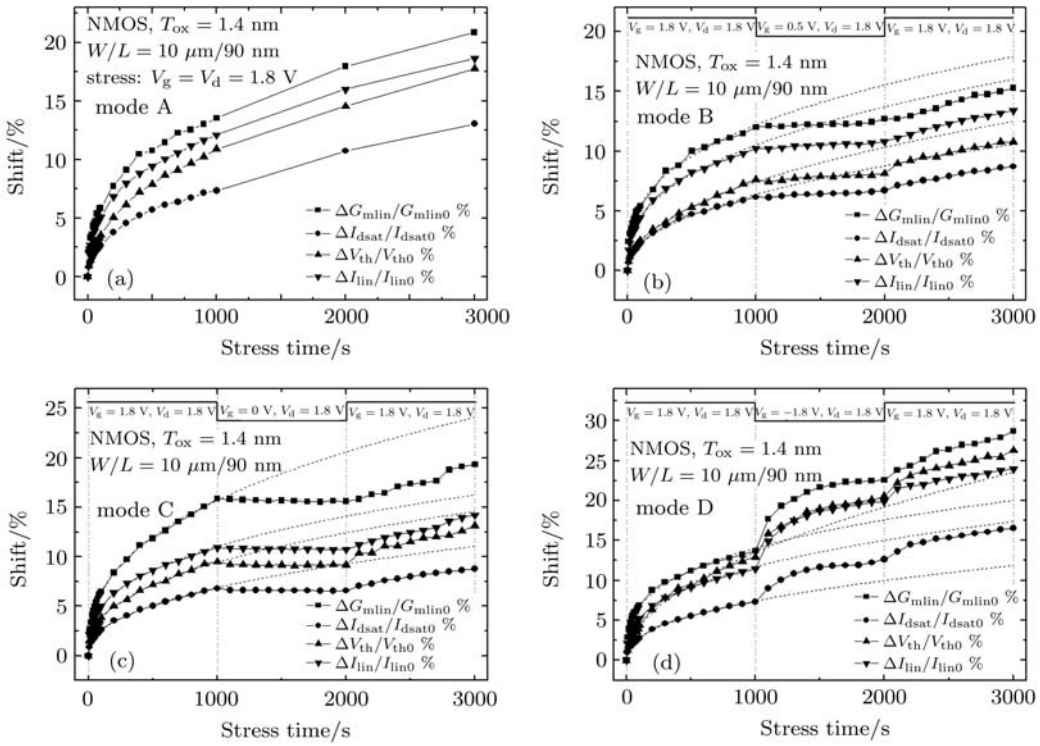


Fig. 3. Parameter degradations under stresses of (a) mode A, (b) mode B, (c) mode C, and (d) mode D.

It is known that in the stress process the hot carriers are mainly caused by lateral channel electric field. The peak channel electric fields of the device under different stress conditions are simulated by Silvaco software, and the results are shown in Fig. 4. We can find that the peaks of the lateral channel electric field are all located in the LDD areas of the device.

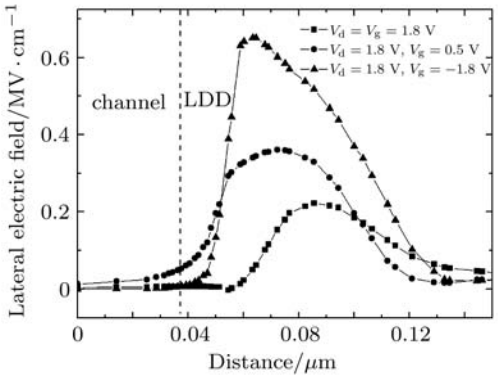


Fig. 4. Distributions of lateral channel electric field under different stress conditions.

In the process of HC stress condition, the electrons from the source are accelerated by the lateral channel electric field, and then cause impact ionization in the depletion region, producing electron–hole pairs, and transferring part of the energy to the electron–hole pairs. The hole obtained energy gets into the substrate by the electron field to form the substrate current, and some of the electrons change the motion direction after the impact and are injected into the Si/SiO_2 interface. As the thickness of the device gate oxide is only 1.4 nm, it can be considered that the device degradation in the first stress interval under alternative stress condition is due mainly to the Si/SiO_2 interface state caused by the channel hot electrons. As shown in Fig. 5(a), the increase of the interface states leads to the increase of the threshold voltage of the device, and the decrease of the linear and saturated drain currents, caused by the interface state scattering of the electrons from the source.

In the second stress period, some different phenomena occur. With the value of V_d unchanged, we gradually reduce the value of V_g to the point when the gate current gets the minimum value, and at this time the hole current and electron current are equal. As the electric field reduces from drain to source, the net charges of the electrons and holes injecting from LDD area to the gate oxide are smallest. Therefore, the damage of the oxide under this stress is relatively small as shown in Fig. 5(b). The curve in Fig. 3(b) shows that the degradation stays almost unchanged in the period.

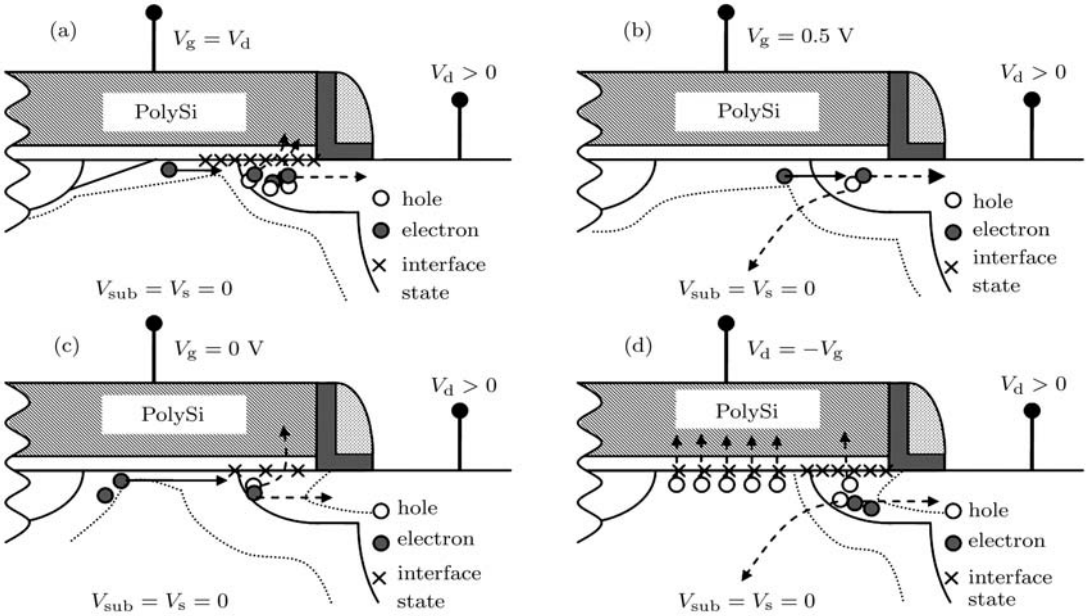


Fig. 5. Channel carrier injections under different stress conditions.

With the decrease of V_g, when $V_g = 0$ V, due to the short channel length of the device and the high voltage applied to the drain, the source and drain depletion layer connect by the electric field as shown in Fig. 5(c). The accelerated electrons of the source side produce the electron-hole pairs by impact ionization in the channel. Some of the electrons get into drain side by the electric field to form the drain current, while a small part of the holes move to the Si/SiO_2 interface. And this part of the holes may fill in the interface states, caused by the hot electron injection in the former stress period. As the energy and number of the holes are small, we can see a small recovery of the degradation, as shown in Fig. 3(c).

For the stress condition of mode D, from Table 1, it can be seen that the device degradation is increased. This stress condition is an off-state stress condition, also known as gate induced drain leakage (GIDL) stress. In this stress condition, the electrons tunnel from LDD region to the drain by band-to-band tunneling, and the holes remain in depletion region. Due to the electric field increasing from drain to gate, the holes in depletion region will be accelerated into the gate and the holes in the substrate will be injected into the gate oxide, which are shown in Fig. 5(d). As the energy and number of the holes are very large, the holes may fill in the electron-traps caused by the electrons in the previous stress time, leading to some recovery of the degradation. However, at the same time the holes will also produce a large number of hole-traps at the Si/SiO_2 interface, which means the increase of the interface states. As the interface states induced are more than the traps filled in by holes, the increase of degradation appears. And then, with the time going on, the interface states are produced continuously. Therefore, the enhanced degradation comes out under this stress condition, which is shown in Fig. 3(d). This stress enhanced hot carrier degradation is called the hot electron-hot hole alternating enhanced degradation.[9,10]

The GIDL stress condition (stress condition of mode D) is the process of which the degradation in each cycle gradually increases. In order to find out how long the degradation increase will last, the experiments were done with the same devices under a long alternating stress test. The cycle of the stress time is 4000 s, and each stress interval in a cycle is 2000 s. The stress condition in each cycle is $V_g = V_d = 1.8$ V and $V_g = -1.8$ V & $V_d = 1.8$ V. The total stress time is 12000 s. The degradation curves are shown in Fig. 6.

From the curves it can be seen that in first 6000 s, the degradation trend is consistent with that in Fig. 3(d). However, in subsequent stress time, a very short period of recovery of the degradation occurs in the hot hole injection process. For the degradation due to the interface damage near drain side, caused by hot–electron (HE) injection under HC stress conditions, it is the electrons that induce the trap charges at the Si/SiO_2 interface. For the HHI stress process, the first hot holes will produce interface states in the channel, and fill in part of the hole traps caused by

HE. As the interface states induced at this time are more than the traps filled in by holes, and the interface states are produced continuously with the time increasing, the continuous degradation appears in the former stress period. But in the following stress period, the traps filled in by holes are greater than the interface states, so at first, a very short period of recovery of the degradation can be observed, and then with the stress time increasing, the interface states are produced continuously and the degradation increases. From the results, the degradation under the alternate stress will gradually approach to that under the pure HE stress. As the stress time increases, the degradation curves of the various parameters gradually approach to the dot line of degradation under HE stress.

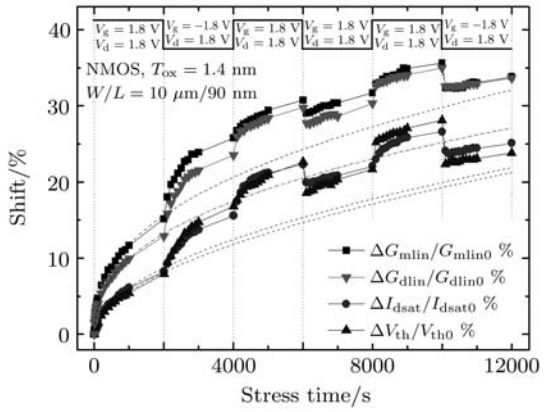


Fig. 6. Device degradation under alternate stress.

The different alternate stresses can reduce or enhance the HC effect, which mainly depends on the latter condition of the stress cycle. It is difficult to accurately estimate the degradation of a device in an actual circuit, but in general, with stress time increasing, the degradation curves of the device under different stress conditions approach to those of DC stress gradually.

4. Conclusions

In this paper, HCI under dynamic stress is studied. From the experiment results, we can obtain different degradations under different stress modes. The different alternate stresses can reduce or enhance the HC effect, which mainly depends on the latter condition of the stress cycle. In mode A (DC stress with electron injection), the degradation keeps increasing. In the modes B (DC stress and then stress with the smallest gate injection) and C (DC stress and then stress with hole injection under $V_g = 0$ V & $V_d = 1.8$ V), there is recovery in the second stress period. In the mode D (DC stress and then stress with hole injection under $V_g = -1.8$ V & $V_d = 1.8$ V), degradation or recovery depends on the fact that the traps filled in by holes are smaller or greater than the interface states. Therefore, there are degradation and recovery during different stress periods.

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