Ultra-low on-resistance high voltage (> 600 V) SOI MOSFET with a reduced cell pitch*

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A low specific on-resistance ($R_{S,on}$) silicon-on-insulator (SOI) trench MOSFET (metal–oxide–semiconductor–field–effect–transistor) with a reduced cell pitch is proposed. The lateral MOSFET features multiple trenches: two oxide trenches in the drift region and a trench gate extended to the buried oxide (BOX) (SOI MT MOSFET). Firstly, the oxide trenches increase the average electric field strength along the x direction due to lower permittivity of oxide compared with that of Si; secondly, the oxide trenches cause multiple-directional depletion, which improves the electric field distribution and enhances the reduced surface field (RESURF) effect in the SOI layer. Both of them result in a high breakdown voltage (BV). Thirdly, the oxide trenches cause the drift region to be folded in the vertical direction, leading to a shortened cell pitch and a reduced $R_{S,on}$. Fourthly, the trench gate extended to the BOX further reduces $R_{S,on}$, owing to the electron accumulation layer. The BV of the MT MOSFET increases from 309 V for a conventional SOI lateral double diffused metal–oxide semiconductor (LDMOS) to 632 V at the same half cell pitch of 21.5 μm, and $R_{S,on}$ decreases from 419 m$\Omega\cdot$cm^2 to 36.6 m$\Omega\cdot$cm^2. The proposed structure can also help to dramatically reduce the cell pitch at the same breakdown voltage.

Keywords: silicon-on-insulator, electric field, breakdown voltage, trench gate, trench

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1. Introduction

Improvement on the specific on-resistance ($R_{S,on}$) has been limited by a long drift region for a conventional high voltage lateral MOSFET. Trench technology is used to reduce cell pitch and increase the packing density of a power MOSFET while maintaining its high breakdown voltage.[1−5] A trench was used in the drift region under the gate so as to reduce the field peak at the end of the gate field plate when the drift doping was high, which led to a trade-off between breakdown voltage (BV) V_{BV} and R_{on},[1] where the effect of the trench was limited nevertheless. Two structures in which the gate and source or the gate and drain were placed in one trench were used to reduce both cell pitch and $R_{S,on}$.[2,3] Unfortunately, they are good options only for MOSFETs with $V_{BV} < 100$ V, owing to the complex fabrication process and weakened effect of devices with a higher BV. A novel 250-class lateral trench MOSFET was proposed in bulk Si.[4] $V_{BV} > 600$ V power devices are actually widely employed in high voltage power fields, such as motor control and traction fields, where low power dissipation is a major concern.

According to the structure in Ref. [4] and the authors' investigation on power SOI devices with enhanced dielectric field strength,[6−12] we propose an SOI power MOSFET with multiple trenches: two oxide trenches in the drift region and one trench gate extended to the buried oxide (BOX). The oxide trenches improve the BV as well as greatly reducing both cell pitch and $R_{S,on}$, the extended trench gate further reduces $R_{S,on}$. The proposed device has a high BV, an ultra-low $R_{S,on}$ and a reduced cell pitch in the state-of-the-art 600-class lateral MOSFETs.

2. Device structure and mechanism

Figure 1 shows the schematic cross sections of the SOI MT MOSFET and an SOI conventional LD-

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MOS (SOI Con. LDMOS). Two oxide trenches are placed between the source and drain for the SOI MT MOSFET. The drain region is in the centre; the oxide trenches, the source and gate trench are in the peripheral region in sequence. $W_{\rm T}$ and $D_{\rm T}$ are the width and the depth of the two oxide trenches, respectively. $t_{\rm S}$ and $N_{\rm d}$ are the thickness and the doping concentration of the SOI layer, respectively. $t_{\rm I}$ is the BOX thickness. Figure 1 shows the x and the y directions in simulation.

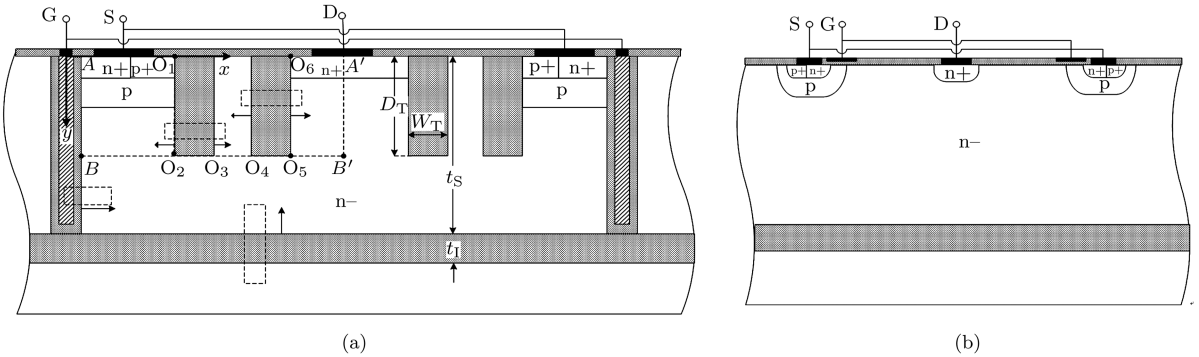


Fig. 1. Schematic cross sections of (a) SOI MT MOSFET and (b) SOI conventional LDMOS.

The oxide trench is built into the drift region to improve the field distribution. In the x direction, the Gauss law is expressed as $\varepsilon_{\rm Si}E_{\rm Si} = \varepsilon_{\rm OX}E_{\rm TOX}$ in the Si/trench oxide interface, where $E_{\rm Si}$ and $E_{\rm TOX}$ are the electric field strengths of the Si and trench oxide in the interface, $\varepsilon_{\rm OX}$ and $\varepsilon_{\rm Si}$ are the relative permittivities of oxide and Si, respectively. Firstly, the oxide trenches increase the $E_{\rm TOX}$ due to lower $\varepsilon_{\rm OX}$ of 3.9 than $\varepsilon_{\rm Si}$ of 11.9. Secondly, the oxide trenches cause the drift region to be folded in the vertical direction, leading to a reduced cell pitch. Thirdly, multiple-directional depletion is caused and strengthened by the four structures in the dash rectangle of Fig. 1, where the arrows show the depleting directions in the Si regions. In short, the oxide trenches reshape the electric field, leading to an enhanced RESURF effect. Therefore, the BV is increased and cell pitch as well as $R_{\rm S,on}$ is reduced. In the on-state, in addition to the vertical inversion layer channel in the p region, the long electron accumulation layer is formed beside the extended gate in the n-drift region. Both increase the effective vertical conduction region and thus further reduce $R_{\rm S,on}$.

3. Results and discussion

Figure 2 shows the electric field distributions in the x direction for the SOI MT MOSFET and the Con. LDMOS. The low permittivity of the oxide results in a high field strength of the trench oxide for the MT MOSFET compared with that of the Si drift region for Con. LDMOS. This fact conforms with the surface field distribution in Fig. 2(a). The two oxide trenches and the BOX strengthen the multiple-directional depletion. This causes the electric field reshaping effect and the RESURF enhancing effect. These two effects increase the field strength in the Si region under the oxide trenches. However, the multiple-directional depletion and the RESURF effect are weak due to the absence of the two trenches and the presence of the thick SOI layer in the SOI Con. LDMOS. Consequently, at BB' cut lines (in Fig. 1), the field strength is high for the MT MOSFET while it is almost zero for the Con. LDMOS as illustrated in Fig. 2(b). Figures 3(a) and 3(b) show the electric field distributions and the potential distributions in the y direction for the two structures, respectively. Both the electric field reshaping effect and the RESURF enhancing effect increase the field strength under the drain and thus result in a uniform field distribution in the SOI layer along the y direction in Fig. 3(a). According to Gauss law $\varepsilon_{\rm Si}E_{\rm SOI} = \varepsilon_{\rm OX}E_{\rm BOX}$ in the SOI/BOX interface (where $E_{\rm SOI}$ and $E_{\rm BOX}$ are the interface electric field strengths of the SOI layer and BOX, respectively), the increase in $E_{\rm SOI}$ leads to an increase in $E_{\rm BOX}$ and, thus, the voltages sustained by the SOI layer and the BOX (denoted as $V_{\rm S}$ and $V_{\rm I}$) increase as seen in Fig. 3(b). The BV, which is equal to the sum of $V_{\rm S}$ and $V_{\rm I}$, is improved ultimately. For a SOI MT MOSFET with half the cell pitch of 21.5 μm, the interface

field strengths increase to 2.9×10^5 V/cm (in Si) and 8.7×10^5 V/cm (in BOX) from 0.26×10^5 V/cm (in Si) and 5.4×10^5 V/cm (in BOX) of the Con. LDMOS at $x = 21$ μm, respectively. The BV of 632 V is obtained for the MT MOSFET by simulation, while it is just 309 V for the Con. LDMOS.

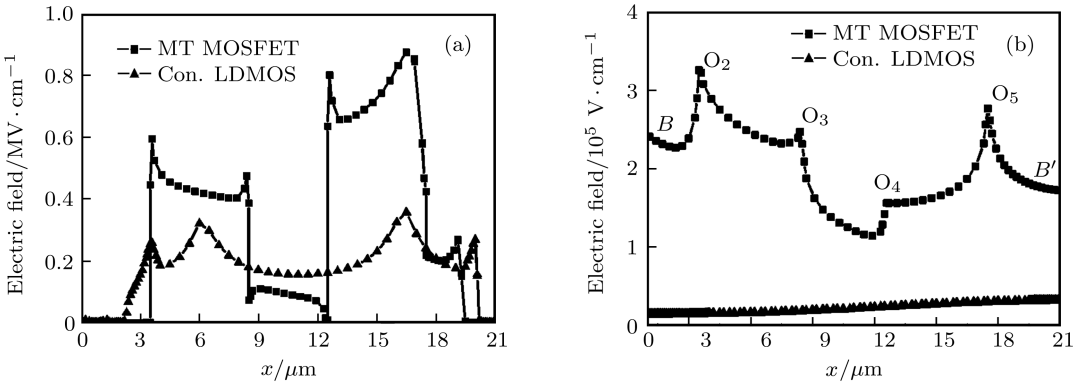


Fig. 2. Lateral electric field distributions (a) at surface and (b) along BB' line ($y = 16.01$ μm).

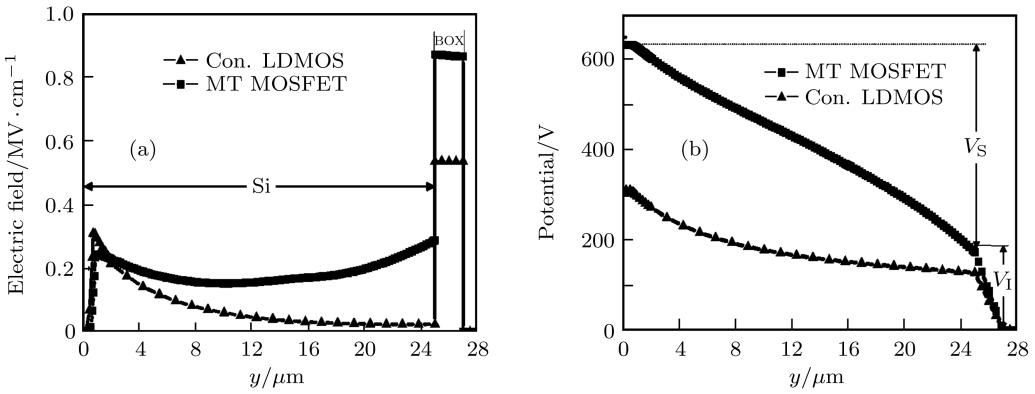


Fig. 3. Electric field distributions (a) and potential distributions (b) in the y direction ($x = 21$ μm), with $W_T = 5$ μm, $D_T = 16$ μm for DT MOSFET, $t_S = 25$ μm, $t_I = 2$ μm and half cell pitch of 21.5 μm for three devices, the N_d being optimized to obtain the maximum BV for each device.

Figure 4 shows equi-potential contours for the two structures. From the source to the drain region for MT MOSFET, the voltage drop in surface (i.e. in O_1O_6) is equal to the voltage drop in the Si region around the two oxide trenches (i.e., along the O_1-O_2-O_5-O_6 line in Fig. 1(a)), as illustrated in Fig. 4(a)). It proves that the oxide trenches cause the drift region to be folded in the vertical direction and thus reduce the cell pitch. Figure 4 demonstrates that the field reshaping effect of the oxide trenches and the RESURF enhancing effect result in the high field strengths in the Si regions under the oxide trenches and under the drain. However, for the Con. SOI LDMOS the Si region in the dot line rectangle of Fig. 4(b) is not effective to share the BV, which accords well with Figs. 3(a) and 3(b).

Figure 5 shows their current flowline contours. The values of BV, $R_{S,on}$ and FOM are given for the SOI MT MOSFET and some parameters of several published structures with the 600 V-class BV are listed in Table 1. Firstly, the extended trench gate widens the effective conduction region for the MT MOSFET, while the conduction region is located in the surface for the Con. LDMOS; secondly, the optimal N_d increases to 1×10^{15} cm^{-3} for the MT SOI MOSFET due to the multiple-directional depletion and the enhanced RESURF effect, while the optimal N_d is 3×10^{13} cm^{-3} for the SOI Con. LDMOS due to the thick SOI layer. Therefore, the $R_{S,on}$ for MT MOSFET is much lower than that of the Con. LDMOS. It is also prior to those of the state-of-art devices with 600-class BV. V_{BV} and the FOM of MT MOSFET are far higher than those of any other device in Table 1. The maximum temperatures are 344 K and 341 K for the SOI MT MOSFET and Con. LDMOS at 0.5 mW/μm, respectively. The heat is dissipated mainly through the heat sinker attached to the

substrate, which results in a similar maximum temperature between those of the MT MOSFET and the Con. LDMOS.

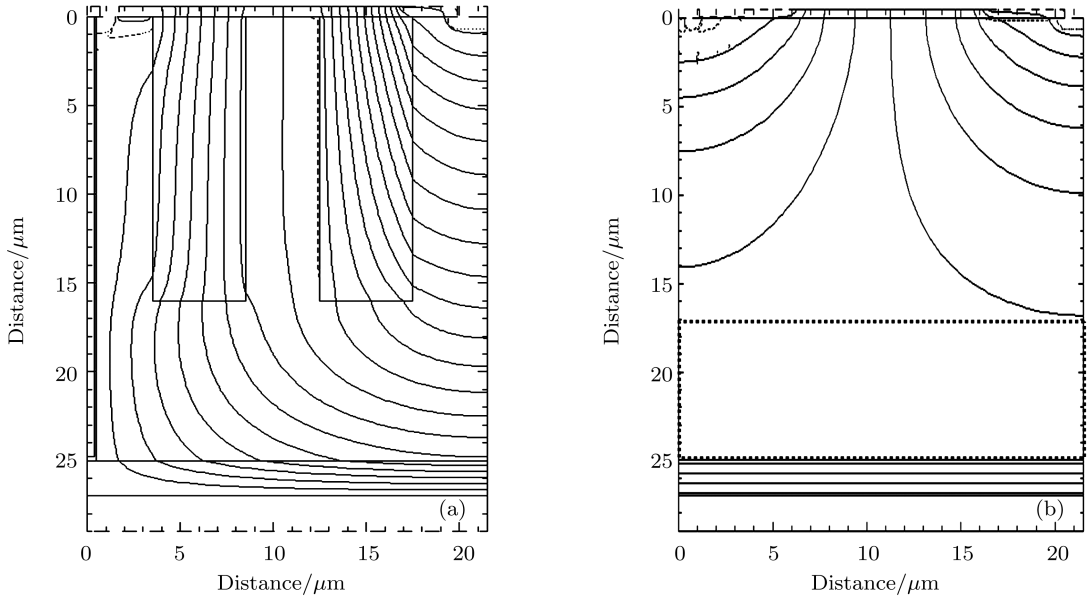


Fig. 4. Equi-potential contours at breakdown voltage for (a) SOI MT (632 V) and (b) SOI Con. LDMOS (309 V) (30 V/contour).

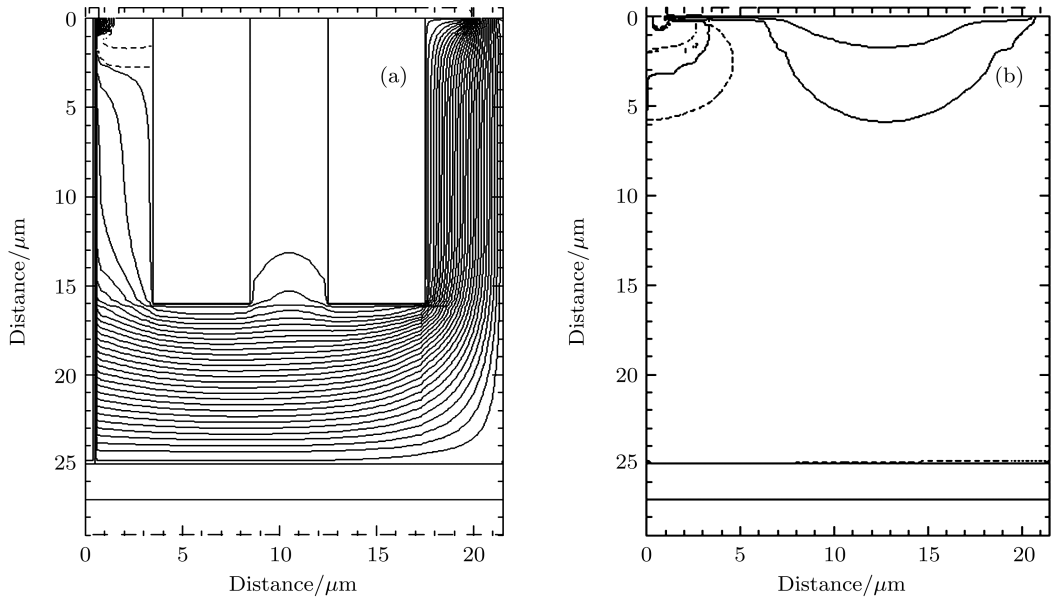


Fig. 5. Current flowline contours with 10^{-7} A $\cdot$ μm^{-1}/contour, $V_{\rm d} = 0.5$ V, and $V_{\rm g} = 15$ V.

Table 1. Parameters $V_{\rm BV}$, $R_{\rm S,on}$ and FOM for SOI and bulk Si MOSFETs with the 600 V-class BV.

	device types	$V_{\rm BV}$/V	$R_{\rm S,on}$/m$\Omega \cdot$cm^2	$(V_{\rm BV}^2/R_{\rm S,on})$/MW $\cdot$ cm^{-2}
SOI	Con. LDMOS	309	419	0.23
	MT	632	36.6	10.9
	SOCOS[13]	600	76	4.7
	graded SOI[13,14]	600	220	1.6
	thick SOI[13,15]	600	200	1.8
bulk Si	double-resurf[16]	650	174	2.4
	Refs. [13] and [17]	600	200	1.8

The dependences of BV and $R_{S,on}$ on the number of the oxide trenches (i.e. n) are shown in Fig. 6, where the width and the depth of every oxide trench keep the constants of $W_T = 4$ μm and $D_T = 16$ μm. As the number of the oxide trench increases, the V_{BV} increases because of the increase of total oxide width, and $R_{S,on}$ decreases due to the increasing optimal N_d. However, the optimal ratio of depth to width of each trench is limited by the process technology; that is to say, we should not design numerous and narrow trenches. The device at $n = 0$ denotes the device with trench gate and without oxide trenches.

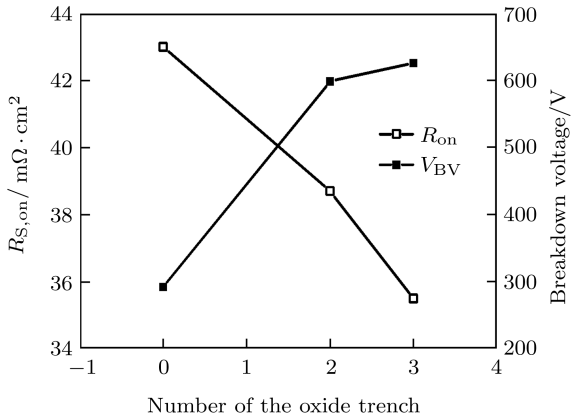


Fig. 6. Dependences of V_{BV} and $R_{S,on}$ on the number of the oxide trenches, with $W_T = 4$ μm and $D_T = 16$ μm.

Figure 7 shows the influences of L_d on the V_{BV} and $R_{S,on}$ of the SOI Con. LDMOS. It can be seen that the V_{BV} monotonically increases until the V_{BV} reaches a saturated BV of 500 V. We can make two conclusions as follows: 1) the maximum V_{BV} is limited by the vertical dimensional parameters (i.e. t_S and t_I) at $L_d > 80$ μm; 2) $V_{BV} > 600$ V is impossible to obtain since the thick SOI layer weakens the couple effect between the PN junction and the vertical MIS-like structure, leading to the low electric field strengths in the bottom of the SOI layer as well as in the BOX. The PN junction is formed by the p-base and n-drift region and the MIS-like structure consists of the substrate, BOX (i.e. "I") and the n-drift (i.e. "S") herein.

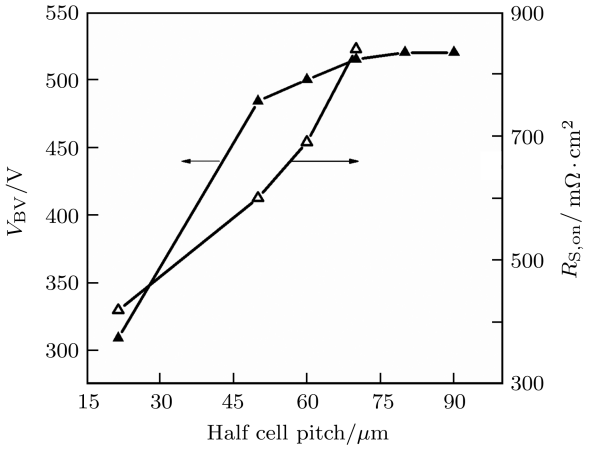


Fig. 7. Influences of L_d on V_{BV} and $R_{S,on}$ of SOI Con. LDMOS.

For the SOI MT MOSFET, we can form the trench gate and dielectric isolation trenches by employing the same fabrication process as that used in Refs. [18], [19] and [20].

4. Conclusion

An extended trench gate SOI lateral MOSFET with two oxide trenches in the drift region is proposed and investigated by simulation. The oxide trenches cause multiple-dimensional depletion and enhance the RESURF effect, resulting in an enhanced blocking voltage. The oxide trenches also fold the drift region in the vertical direction, leading to shortened cell pitch and thus an ultra-low specific on-resistance. The extended trench gate widens the effective conduction area and thus further reduces the on-resistance. The BV value doubles and $R_{S,on}$ is reduced by one order magnitude at the same cell pitch size compared with those of the SOI convention LDMOS. The novel device has a great potential application in fields that require high voltages and low power loss.

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