Characterization of Al_2O_3/GaN/AlGaN/GaN metal–insulator–semiconductor high electron mobility transistors with different gate recess depths*

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In this paper, in order to solve the interface-trap issue and enhance the transconductance induced by high-k dielectric in metal–insulator–semiconductor (MIS) high electron mobility transistors (HEMTs), we demonstrate better performances of recessed-gate Al_2O_3 MIS-HEMTs which are fabricated by Fluorine-based Si_3N_4 etching and chlorine-based AlGaN etching with three etching times (15 s, 17 s and 19 s). The gate leakage current of MIS-HEMT is about three orders of magnitude lower than that of AlGaN/GaN HEMT. Through the recessed-gate etching, the transconductance increases effectively. When the recessed-gate depth is 1.02 nm, the best interface performance with τ_{it}=(0.20–1.59) μs and D_{it}=(0.55–1.08)$\times 10^{12}$ cm$^{-2}\cdot$eV^{-1} can be obtained. After chlorine-based etching, the interface trap density reduces considerably without generating any new type of trap. The accumulated chlorine ions and the N vacancies in the AlGaN surface caused by the plasma etching can degrade the breakdown and the high frequency performances of devices. By comparing the characteristics of recessed-gate MIS-HEMTs with different etching times, it is found that a low power chlorine-based plasma etching for a short time (15 s in this paper) can enhance the performances of MIS-HEMTs effectively.

Keywords: AlGaN/GaN gate-recessed MIS-HEMT, frequency-dependent capacitance and conductance, drain current injection technique, knee resistance

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1. Introduction

Gallium nitride-based high electron mobility transistors (HEMTs) are extremely promising for microwave and mm-wave power electronics applications because of their high breakdown field and high saturation velocity. Khan *et al.*[1] first demonstrated them in 1993. Wu *et al.*[2] reported the first RF data of a GaN HEMT at 2 GHz in 1996. In order to improve material quality, two major breakthroughs in device design, the adoption of SiN_x passivation layer in 2000[3] and the implementation of field plates,[4–6] ensured a record power density of 30 W/mm at 8 GHz reported in 2004[7] and 41.4 W/mm at 4 GHz reported in 2006.[8] However, the performance and the reliability of AlGaN/GaN HEMT have some problems in, such as, current slump, high gate leakage current, and high drain leakage current.[9,10] GaN MIS-HEMT with a thin high-k dielectric film is one of the effective solutions to reduce the high gate leakage current and improve the device performance.[11] In the present paper, in order to solve the interface-trap issue and enhance the transconductance induced by high-k dielectric in MIS-HEMTs, we demonstrate the performances of GaN-based recessed-gate Al_2O_3 MIS-HEMTs which are fabricated by Fluorine-based Si_3N_4 etching and Chlorine-based AlGaN etching with three etching times (15 s, 17 s and 19 s). After Chlorine-based etching, the interface-trap density is reduced obviously without generating any new type of trap.

2. Device and fabrication

AlGaN/GaN MIS-HEMTs with different gate depth structures were grown on 2-in sapphire sub-

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strates using the metal–organic chemical vapour deposition (MOCVD). Figure 1 shows the cross-sectional view of the recessed-gate MIS-HEMT structure used in this paper. The heterostructure consists of an AlN nucleation layer, an unintentionally doped-GaN buffer (~ 1 μm) and an undoped 19 nm-thick AlGaN barrier layer. The Al mole fraction was determined by x-ray diffraction to be 30%. The device fabrication started with mesa isolation performed by reactive ion etching (RIE) with Cl_2. Ohmic contacts consisting of Ti/Al/Ni/Au (22 nm/140 nm/55 nm/45 nm) were annealed in a nitrogen ambient at 870 °C for 40 s. The Si_3N_4 film (60 nm) was deposited as a passivation layer using plasma enhanced chemical vapour deposition (PECVD) at 250 °C. Different gate recesses were fabricated by using Fluorine-based reactive-ion etching Si_3N_4 and Chlorine-based reactive-ion etching AlGaN with three etching times (15 s, 17 s and 19 s). The Schottky contact was formed by Ni/Au (20 nm/140 nm).

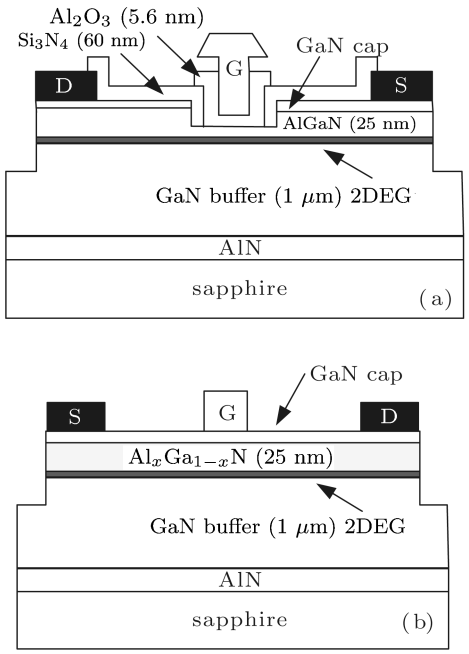


Fig. 1. Schematic structures of recessed-gate MIS-HEMT (a) and GaN HEMT (b).

3. Measurement and discussion

To measure the gate recess depths 1-MHz capacitance–voltage (CV) measurements (see the Fig. 2) were carried out on the fabricated Schottky diodes. The recessed-gate etching can effectively increase the values of transconductance and the maximum I_D density in all gate-recessed MIS-HEMTs.[12,13] As the density of the interface-trap was obviously reduced by chlorine-based reactive-ion etching, the two-dimensional electron gas (2DEG) carrier concentration (N_{cv}) of recessed-gate MIS-HEMT was higher than that of un-recessed-gate MIS-HEMT. Moreover, the plasma induced damage influences the reduction of 2DEG carrier concentrations in different gate recess MIS-HEMTs (see Table 1).

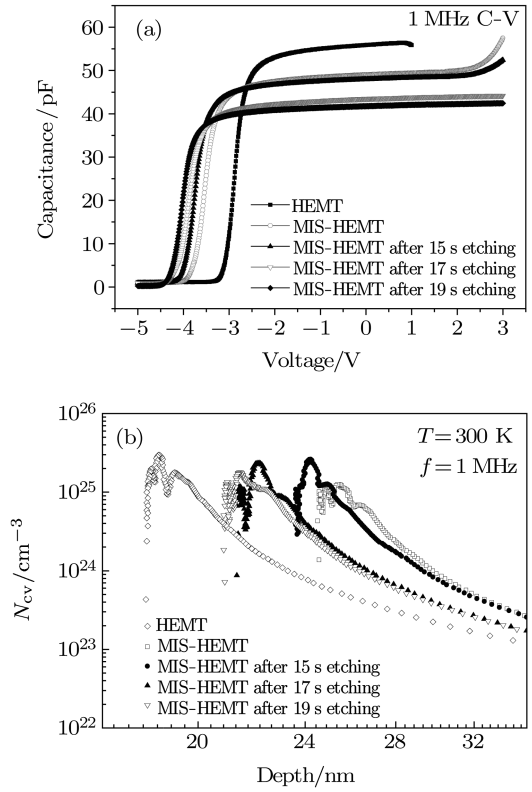


Fig. 2. The C–V characteristics (a); and carrier density distributions (b) of different recessed-gate MIS-HEMTs.

Table 1. Device characteristics of different recessed-gate MIS-HEMTs.

	no etching	Cl_2 etching 15 s	Cl_2 etching 17 s	Cl_2 etching 19 s
recess depth/nm	0	1.0	3.2	3.7
$N_{DC-V}/10^{25}$ cm^{-3}	1.25	2.61	2.34	1.79
2DEG depth/nm	25.2	24.2	22.2	21.5
I_{DSS}/mA·mm^{-1}	978.4	1023.0	1027.0	1045.7
$g_{m,peak}$/mS·mm^{-1}	162.4	173.6	184.9	188.7
V_{th}/V	–5.2	–4.9	–4.6	–4.4
I_{on}/I_{off}	4.6×10^5	3.7×10^5	3.5×10^5	3.3×10^5
SS/(mV/dec)	234	179	124	144

Figure 3(a) shows the comparisons of barrier thickness and $V_{\rm th}$(MOS)–$V_{\rm th}$(HEMT) versus etching time; and figure 3(b) indicates the gate leakage characteristics of different devices. The high nonlinearity of etching depth versus etching time may be related to the formation of a thin oxide layer in the GaN cap surface before or during the etching. The gate leakage current of MIS-HEMT is about three orders of magnitude lower than that of AlGaN/GaN HEMT. With recess depth increasing, the gate leakage current becomes higher than that of MIS-HEMT. Some defects (N vacancies) generate plasma bombardment during the plasma etching.[14] The N vacancies, which reduce the Schottky barrier height and enhance the tunneling effect,[15] are regarded as n-type doped in the etched AlGaN surface (see Fig. 4). The obvious increase in gate leakage current is due to the increased roughness and the occurrence of these N vacancies in the etched AlGaN surface.

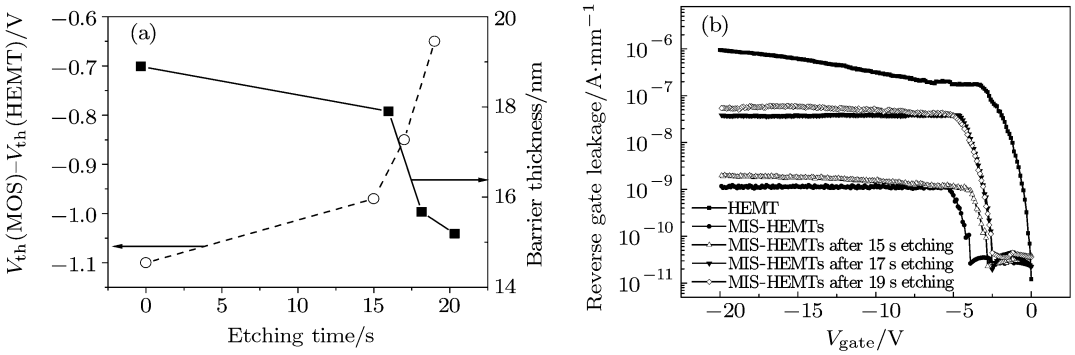


Fig. 3. (a) Comparison of barrier thicknesses and $V_{\rm th}$(MOS)–$V_{\rm th}$(HEMT) versus etching time; and (b) gate leakage characteristics of different devices.

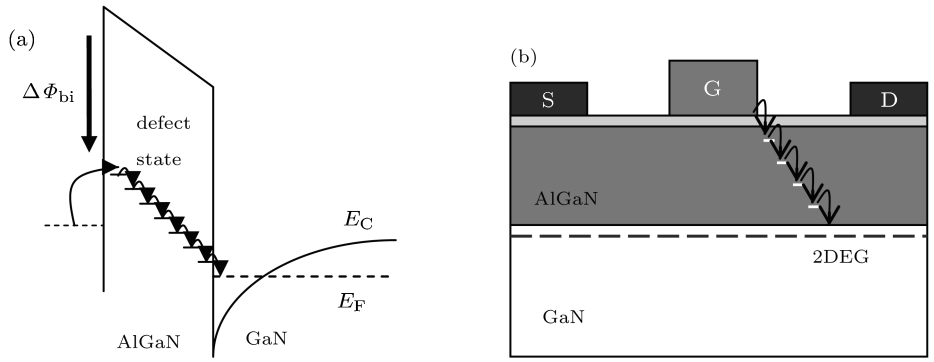


Fig. 4. (a) Schematic band diagram describing the mechanism of gate leakage increase due to trap-assisted electron tunneling; and (b) generated defects in the etched AlGaN surface and the gate leakage path across the AlGaN barrier.

The capacitance and the conductance measurements in a frequency range from 10 kHz to 1 MHz are used to characterize the trapping effects in the HEMTs and MIS-HEMTs with different gate recess depths. The equivalent parallel capacitance $C_{\rm p}$ and conductance $G_{\rm p}$ each as a function of frequency, under the assumption of a continuum of trap levels, can be expressed as[16]

$$C_{\rm p} = C_{\rm b} + \frac{qD_{\rm T}}{\omega\tau_{\rm T}\tan(\omega\tau_{\rm T})},$$

and

$$\frac{G_{\rm p}}{\omega} = \frac{qD_{\rm T}}{2\omega\tau_{\rm T}}\ln[1+(\omega\tau_{\rm T})^2],$$

where $D_{\rm T}$ is the trap density, $\tau_{\rm T}$ is the trap state time constant, $C_{\rm b}$ is the barrier capacitance, and ω is the radial frequency. The values of $D_{\rm T}$ and $\tau_{\rm T}$ can be extracted by fitting the experimental data of $C_{\rm p}(\omega)$ or $G_{\rm p}(\omega)$. The conductance data are used to analyse the trap, as in this case the barrier capacitance $C_{\rm b}$ is not required to be known. The curves for typical $G_{\rm p}/\omega$ versus ω for the HEMTs and MIS-HEMTs with dif-

ferent gate recess depths, measured at selected biases near threshold voltage, are shown in Fig. 5.

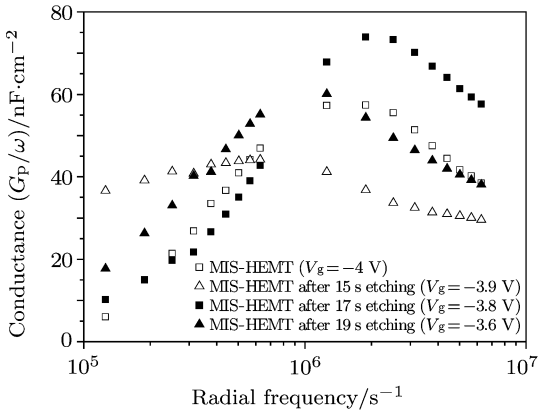


Fig. 5. Comparison of curves for G_p/ω versus ω curves between MIS-HEMTs and HEMTs with different etching depths.

When the recessed-gate depth is about 1 nm, the best interface with τ_{it}=(0.20–1.59) μs and D_{it}=(0.55–1.08)$\times 10^{12}$ cm^{-2}·eV^{-1} is obtained. After chlorine-based etching, the interface-trap density has reduced obviously without generating any new type of trap (shown in Table 2). A low power chlorine-based plasma treatment effectively removes the natural oxidation which introduces N vacancies and relevant defects in the AlGaN near-surface region because of the escape of N atoms in the form of NO_x as well as partial formation of Al oxide and Ga oxide as indicated in Ref. [17]. In comparison with conventional MIS-HEMTs, the recessed-gate MIS-HEMTs each have a low subthreshold swing (see Fig. 6). It is indicated that the recessed-gate MIS-HEMTs have much less interface-traps, which accord well with the C–f analysis results.

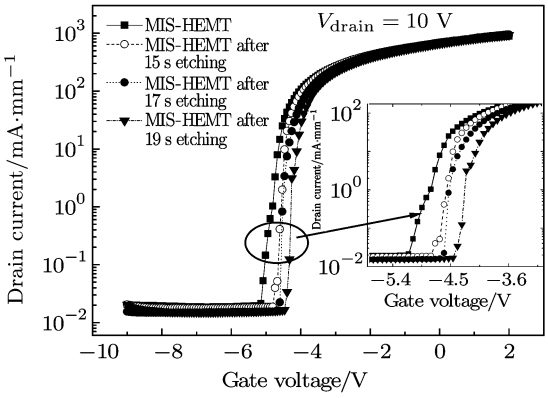


Fig. 6. Subthreshold characteristics of different devices, where the inset describes subthreshold slopes in detail.

Table 2. Characteristics of interface-trap in different devices.

	depth/nm	$D_{it}/10^{12}$ cm^{-2}·eV^{-1}	τ_{it}/μs
MIS-HEMT	0	0.72–1.22	0.19–0.64
MIS-HEMT after 15 s etching	1.0	0.55–1.08	0.20–1.59
MIS-HEMT after 17 s etching	3.2	0.97–1.14	0.24–0.49
MIS-HEMT after 19 s etching	3.7	0.76–1.2	0.19–0.94

The off-state breakdown characteristics of the devices with different gate recess depths, fabricated using drain current injection technique, are shown in Fig. 7 as shown in Refs. [18] and [19]. Setting 1 mA/mm drain current as the breakdown criterion yields off-state breakdown voltages of 102, 102, 87 and 84 V for the devices with 0, 1.0, 3.2 and 3.7 nm gate recess depths, respectively. It suggests that the negatively charged chlorine ions that were introduced during the dry etching of the gate recess accumulated in the top barrier layer, causing upward bending of the conduction band edge as shown in Ref. [15]. The accumulated chlorine ions and the N vacancies in the GaN cap surface which was caused by the dry etching increase the trap state density of the Schottky barrier layer and thus enhance the probability of trap-assisted tunneling as indicated in Ref. [20]. The increase in the electric field with the increase of gate recess depth produces an elevated leakage current, which degrades the breakdown characteristics. We suggest that either the dry etching recipe of the gate recess should be optimized or the post-annealing should be implemented for alleviating the effect of the plasma-induced degradation on the Schottky gate as shown in Refs. [21] and [22].

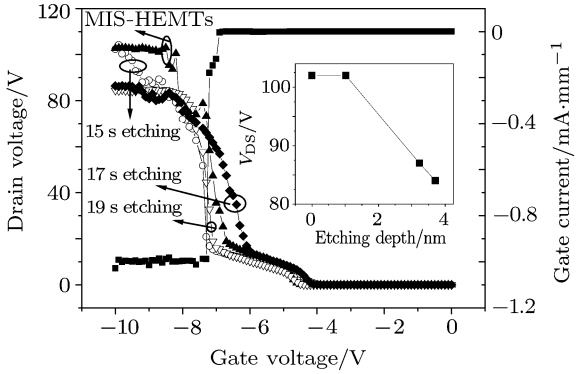


Fig. 7. Off-state breakdown characteristics of different devices, measured by DCIT. Inset shows the curve for breakdown voltage (BV) versus etching depth.

Recess etching has an influence on current collapse due to surface and bulk traps. In order to quantify the current dispersion, we have measured the values of knee resistance [$R_{\rm knee}$=knee voltage/knee current ($V_{\rm k}/I_{\rm k}$)] of pulsed $I_{\rm DS}$–$V_{\rm DS}$ characteristics at different values of individual drain–source sweep voltage ($V_{\rm DS}$ = 0–8, 0–10, 0–15, 0–20, 0–25, 0–28, 0–30 V) and $V_{\rm g}$ = 0 V for different recess and non-recess gate

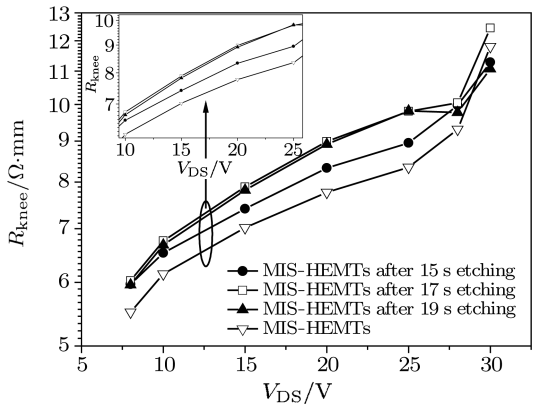


Fig. 8. Knee resistances of different devices, measured at $V_{\rm g}$ = 0 V. Inset shows the increase of knee resistance in detail.

MIS-HEMTs. Figure 8 shows the curves of $R_{\rm knee}$ as a function of $V_{\rm DS}$ for MIS-HEMTs and MIS-HEMTs with different gate recess depths. The increase of current collapse after gate-recess process strongly depends on surface related trap. Conway *et al.*[23] have reported that the $V_{\rm k}$ walkout/current collapse of GaN HEMT by recess gate etching is due to surface trap. They have also confirmed that the shallower recess depth (less surface area) minimizes the $V_{\rm k}$ walkout/current collapse.

By comparing the characteristics of recessed-gate MIS-HEMTs with different etching times, it is found that a low power chlorine-based etching for a short time (15 s in this paper) can enhance the performances of MIS-HEMTs effectively.

4. Conclusion

Through the recessed-gate etching, the transconductance has increased effectively. The gate leakage current of MIS-HEMT is about three orders of magnitude lower than that of AlGaN/GaN HEMT. When the recessed-gate depth is about 1 nm, the best interface performance with $\tau_{\rm it}$ =(0.20–1.59) μs and $D_{\rm it}$=(0.55–1.08)$\times10^{12}$ cm^{-2}·eV^{-1} can be obtained. After chlorine-based etching, the interface-trap density has reduced considerably without generating any new type of trap. The accumulated chlorine ions and the N vacancies in the AlGaN surface caused by the plasma etching can degrade the breakdown and the high frequency characteristics of devices. By comparing the characteristics of recessed-gate MIS-HEMTs with different etching times, it is found that a low power chlorine-based plasma etching for a short time (15 s in this paper) can enhance the performances of MIS-HEMTs effectively.

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