Enhancement-mode AlGaN/GaN high electronic mobility transistors with thin barrier*

Ma Xiao-Hua(马晓华)[a)b)†], Yu Hui-You(于惠游)[a)], Quan Si(全 思)[b)], Yang Li-Yuan(杨丽媛)[b)], Pan Cai-Yuan(潘才渊)[a)], Yang Ling(杨 凌)[b)], Wang Hao(王 昊)[b)], Zhang Jin-Cheng(张进成)[b)], and Hao Yue(郝 跃)[b)]

[a)] *School of Technical Physics, Xidian University, Xi'an* 710071, *China*

[b)] *Key Laboratory of Wide Band Gap Semiconductor Materials and Devices, School of Physics Technology, Xidian University, Xi'an* 710071, *China*

(Received 14 August 2010; revised manuscript received 9 October 2010)

An enhancement-mode (E-mode) AlGaN/GaN high electron mobility transistor (HEMTs) was fabricated with 15-nm AlGaN barrier layer. E-mode operation was achieved by using fluorine plasma treatment and post-gate rapid thermal annealing. The thin barrier depletion-HEMTs with a threshold voltage typically around –1.7 V, which is higher than that of the 22-nm barrier depletion-mode HEMTs (–3.5 V). Therefore, the thin barrier is emerging as an excellent candidate to realize the enhancement-mode operation. With 0.6-μm gate length, the devices treated by fluorine plasma for 150-W RF power at 150 s exhibited a threshold voltage of 1.3 V. The maximum drain current and maximum transconductance are 300 mA/mm, and 177 mS/mm, respectively. Compared with the 22-nm barrier E-mode devices, $V_{\rm T}$ of the thin barrier HEMTs is much more stable under the gate step-stress.

Keywords: high electron mobility transistors, AlGaN/GaN, thin barrier, fluorine plasma treatment, threshold voltage

PACS: 73.40.Kp, 73.61.Ey, 78.30.Fs **DOI:** 10.1088/1674-1056/20/2/027303

1. Introduction

The development of high electron mobility transistors (HEMTs) based on GaN and its alloys has largely advanced in recent years, enabling state-of-the-art microwave amplifiers.[1] The material system has demonstrated excellent thermal and electric stability, as well as high mobility and breakdown field, but the conventional HEMT is a depletion-mode device.[2–5] While significant progress has been made toward developing depletion-mode devices, a normally off device is highly desirable for two key applications: power switching converters and digital logic circuits.

The E-mode HEMTs have been fabricated by a variety of techniques including the growth of a thin barrier layer,[6] or recessed-gate structure by etching a part of AlGaN layer,[7–9] fluorine plasma treatment[10–14] and using a piezoelectric cap technique.[15,16] The gate-recess structure is to reduce the thickness of the barrier layer under the gate metal which can effectively modify the $V_{\rm T}$ of AlGaN/GaN HEMTs to positive direction. However, the ICP–RIE (inductively coupled plasma–reactive ion etching) etching will introduce damage and defects to the AlGaN layer, which will affect the device performance. For example, the uniformity in the recess-etch depth and consequently the uniformity in the threshold voltage and gate capacitance, are other challenging issues for this method.

A technique based on fluoride-based plasma treatment of the gate region using a 15-nm AlGaN barrier is reported in this paper. The barrier thickness can be controlled by changing the growth condition accurately. This approach combined with a post-gate anneal has enabled the realization of E-HEMT with a high $V_{\rm T}$ of 1.3 V and $I_{\rm max}$ of 300 mA/mm.

2. Device structure and fabrication process

The AlGaN/GaN HEMT layer was grown by metal-organic chemical vapour deposition (MOCVD) on a sapphire substrate. The heterostructure consists of a 100-nm-AlN nucleation layer, a 1-μm-GaN buffer

*Project supported by the Major Program and State Key Program of National Natural Science Foundation of China (Grant Nos. 60890191 and 60736033) and the National Key Science & Technology Special Project (Grant No. 2008ZX01002-002).

†Corresponding author. E-mail: xhma@xidian.edu.cn

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layer, 1-nm-AlN interlayer, and an un-doped 15-nm AlGaN barrier layer. The AlN mole fraction of the AlGaN was 0.3. Hall measurement of the structure yields an electron sheet density of 1.33×10^{13} cm^{-2} and a mobility of 1615 cm^2/Vs at room temperature.

A schematic cross section of fabricated HEMT is showed in Fig. 1. The fabrication process was similar to that used in our previous work.[11] The devices fabrication started with mesa isolation which was formed by reactive ion etching (RIE) with the etch-depth of 200 nm. Source and drain Ohmic contact were formed by using evaporating Ti/Al/Ni/Au (22 nm/140 nm/55 nm/45 nm) annealed at 870 °C for 30 s. TLM measurement gave a transfer resistance of 0.3 Ω·mm and a sheet resistance of 345 Ω·mm. Gate regions were treated by fluorine plasma for 150-W RF power at 150 s prior to gate metallization. The implanted region was opened by Step-and-Repeat System separately and etched by RIE separately. The gate windows with 0.6-μm gate length were opened by photolithography. Finally, the Ni/Au Schottky gate was deposited by electron-beam evaporation. D-mode HEMTs were also fabricated on the same sample without plasma treatment to the gate regions. Direct current (DC) characteristics were measured by Agilent B 1500A semiconductor parameter analyser, and capacitance–voltage characteristics were measured by Keithley 4200scs.

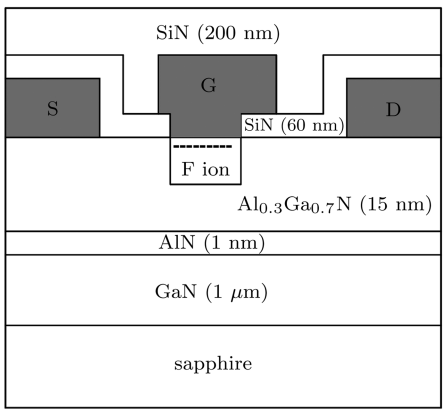


Fig. 1. Cross section of the enhancement-mode AlGaN/GaN HEMT.

3. Results and discussion

The DC transfer and transconductance characteristics of devices treated with fluorine plasma treatment (before and after rapid thermal annealing) are plotted in Figs. 2(a) and 2(b), respectively. The device with a 15-nm AlGaN barrier showed a higher $V_{\rm T}$ (1.3 V) compared to the device with 22-nm AlGaN barrier (0.57 V) under the same condition. In thin barrier AlGaN/GaN HEMTs, the 2DEG electrons are close to the Schottky gate and with the help of the gate metal work function, the threshold voltage can be shifted positively. The implanted fluorine ions can get closer to the channel in thin barrier under the same condition. Thus, the fluorine ion can effectively deplete 2DEG, and a higher $V_{\rm T}$ is achieved. The fluorine concentration is approximated by a linear distribution[11] while the concentration of fluorine ion is the highest near the AlGaN surface and drops by one order of magnitude in the channel.[13] It can be deduced that in the thin barrier HEMTs, 2DEG channel close to the surface where the concentration of F is higher, the fluorine ions can effectively deplete the electrons and achieve a higher $V_{\rm T}$.

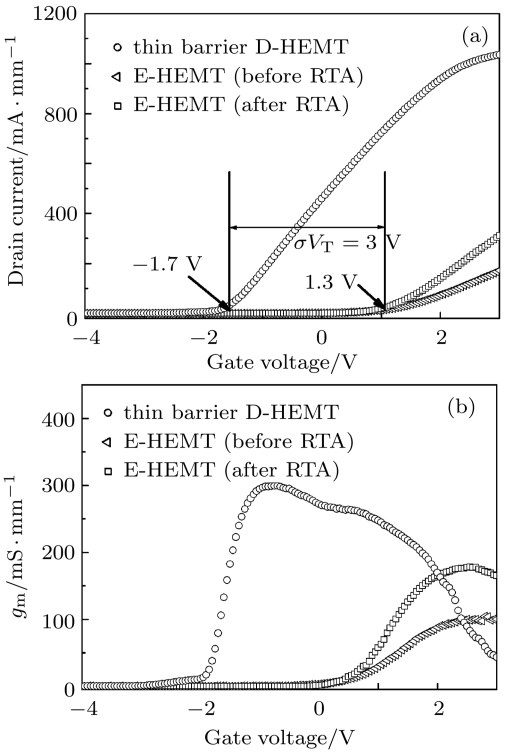


Fig. 2. The DC transfer characteristics (a) and transconductance characteristics (b) of D-mode HEMTs, E-mode HEMTs before and after rapid thermal annealing (RTA) at 300 °C for 2 minute biased at $V_{\rm ds} = 10$ V, $V_{\rm gs} = -4 \sim 3$ V.

The E-HEMT with a 15-nm AlGaN barrier showed a higher $V_{\rm T}$ (1.3 V) compared to D-HEMT with lower $V_{\rm T}$ (–1.7 V). The DC transfer characteristics in Figs. 2 and 3 show that the maximum $V_{\rm T}$ has a shift of 3 V for the thin barrier HEMTs and 4.1 V for the 22-nm barrier HEMTs, respectively. Due to the smaller shift of $V_{\rm T}$, the thin barrier E-HEMT shows a better reliability. The maximum transconductance

increases from 104 mS/mm to 177 mS/mm after rapid thermal annealing (RTA) at 300 °C for 2 minutes. At gate bias of 3 V, the maximum drain current reached 300 mA/mm, as shown in Fig. 4, which is 80% higher than that of maximum drain (166 mA/mm) before RTA. However, the peak of transconductance and current is smaller than that of HEMTs without fluorine plasma treatment, which is attributed to the decrease in mobility. Comparison of the current–voltage characteristics of E-mode devices before and after RTA, it is suggested that the annealing can recover the damages induced during the plasma treatment and achieve a high current density and transconductance.

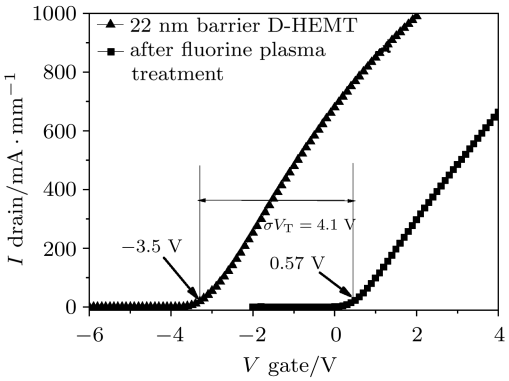


Fig. 3. The DC transfer characteristics of E-mode HEMTs and D-mode HEMTs with 22-nm barrier.

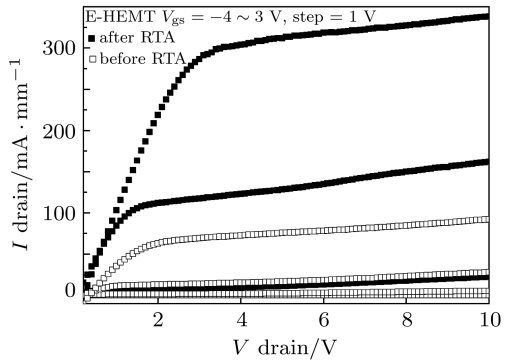


Fig. 4. The DC output characteristic of thin barrier E-mode device before and after RTA.

It is shown in Fig. 5 that the accumulation capacitance of diodes is larger than that without fluorine plasma treatment. The variation of accumulation capacitance of thin barrier HEMTs (290 nF/cm^2) is larger than that of the 22-nm barrier HEMTs (100 nF/cm^2) after fluorine plasma treatment. It can be deduced that the influence of fluorine plasma treatment in the thin barrier structure is larger than that of 22-nm barrier HEMTs. The insert shows the carrier concentration profile versus Schottky gate diodes depth. The gate-to-channel distance decreases about 4 nm after fluorine plasma treatment for both thin barrier HEMTs and 22-nm barrier HEMTs. This result is in good agreement with the atomic force microscope (AFM) measurement result. The etching depth of 4 nm was measured by AFM (Fig. 6). The carrier concentration is decreased from 1.33×10^{13} cm^{-2} to 0.6×10^{13} cm^{-2} after fluorine plasma treatment. As the fluorine plasma etches AlGaN layers, the electron density can be decreased simply due to a thinner AlGaN layer and the control of the gate increase, thus it results in a positive shift of V_T.

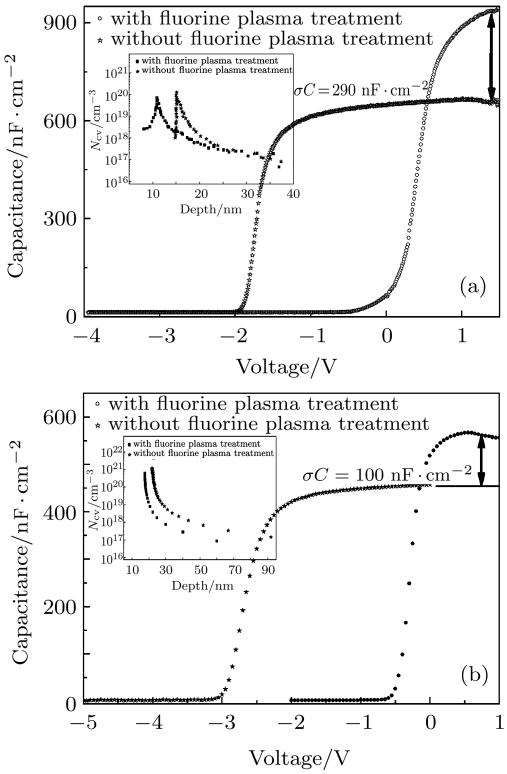


Fig. 5. The C–V characteristics of Schokky diode with and without fluorine plasma treatment, (a) 15-nm barrier HEMTs, (b) 22-nm barrier HEMTs, measured at 100 kHz. The insert shows the 2DEG carrier concentration vs. Schottky gate diodes depth profile.

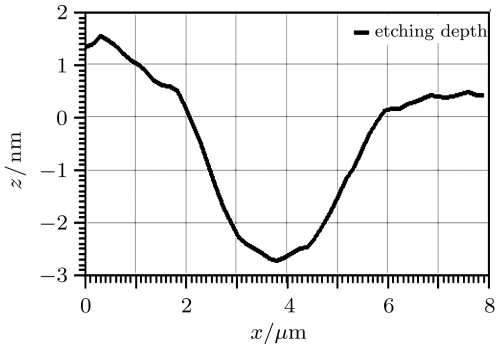


Fig. 6. AFM image showing 4-nm etching depth of fluorine plasma treatment on the AlGaN layer.

The gate step-stress was applied to both 15-nm barrier device and 22-nm barrier device. The degradation of $V_{\rm T}$ after stress was shown in Fig. 7. During stress mode, the drain-source voltage $V_{\rm ds}$ was maintained at 0 V and the gate-source voltage $V_{\rm gs}$ was varied from –1 V to –39 V. The bias voltage stress keeps 1 minute every step. Followed by DC measurement, the threshold voltage of D-mode HEMTs is constant under gate step stress. For the 22-nm E-mode HEMTs the threshold voltage has a negative shifts of 1 V under the gate step stress, while for the thin barrier E-mode the threshold voltage is much more stable and has a negative shift of 0.2 V. It can be deduced that the threshold voltage shift of E-mode devices is due to the fluorine ions far away from the gate regions after stress. Compared with 22-nm E-mode devices, the thin barrier is much stable. It is highly likely that using the thin barrier, the implanted fluorine ions can get closer to the channel, which have a better stability during the electric stress. Furthermore, the positive shifts of $V_{\rm T}$ generated by etching AlGaN layer do not change after the electric stress. The etching AlGaN layers have a relatively larger influence on the thin barrier HEMTs than the 22-nm HEMTs. Thus, the $V_{\rm T}$ of thin barrier devices is much stable under the gate step-stress.

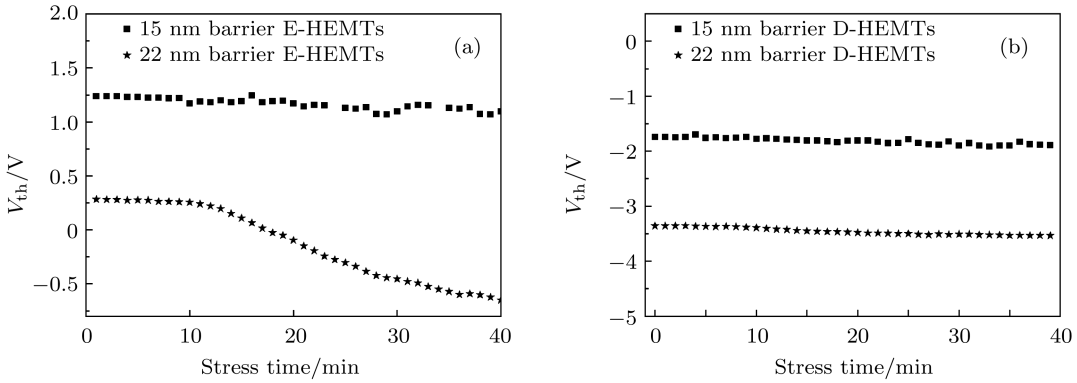


Fig. 7. The degradation of the threshold voltage after gate step-stress for 15-nm barrier device and 22-nm barrier device: (a) E-mode HEMTs, (b) D-mode HEMTs.

4. Conclusion

In conclusion, we fabricated a thin barrier E-mode HEMTs combined with fluorine plasma treatment. The E-mode HEMTs exhibited a higher $V_{\rm T}$ of 1.3 V in comparison with that of the 22-nm E-mode HEMTs (0.57 V) under the same condition of fluorine plasma treatment. The annealing are found to be effective in recovering plasma induced damages. Due to the shorter gate-to-channel distance, the implanted fluorine ions get closer to the channel. With the help of the gate metal work function and the fluorine ions under the gate, the thin barrier E-HEMTs achieve a higher $V_{\rm T}$. The C–V measurement results suggest that with fluorine plasma treatment the gate-to-channel distance decreases 4 nm, in good agreement with the AFM measured result. Compared with the 22-nm barrier E-HEMTs, the $V_{\rm T}$ of thin barrier devices is much more stable under the gate step-stress.

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