Novel high-voltage power device based on self-adaptive interface charge*

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This paper presents a novel high-voltage lateral double diffused metal–oxide semiconductor (LDMOS) with self-adaptive interface charge (SAC) layer and its physical model of the vertical interface electric field. The SAC can be self-adaptive to collect high concentration dynamic inversion holes, which effectively enhance the electric field of dielectric buried layer ($E_{\rm I}$) and increase breakdown voltage (BV). The BV and $E_{\rm I}$ of SAC LDMOS increase to 612 V and 600 V/μm from 204 V and 90.7 V/μm of the conventional silicon-on-insulator, respectively. Moreover, enhancement factors of η which present the enhanced ability of interface charge on $E_{\rm I}$ are defined and analysed.

Keywords: self-adaptive interface charge, inversion holes, dielectric layer electric field, breakdown voltage

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1. Introduction

Silicon-on-insulator (SOI) is a promising technology for power integrated circuit (IC) owing to its effective isolation, lower leakage current, and high breakdown voltage $V_{\rm BV}$. The breakdown voltage of SOI high voltage device is limited by the low vertical breakdown voltage ($V_{\rm B}$), and some works have been carried out.[1−4] Enhancing the electric field of the buried dielectric is a feasible way to increase the $V_{\rm B}$, so $V_{\rm BV}$ by ENDIF (enhanced dielectric layer field) and several new structures have been proposed,[5−13] in which, introducing self-adaptive interface charges (SACs) is effective and attractive.

In this paper, a new SAC high voltage lateral double diffused metal–oxide semiconductor (LDMOS) and its working mechanism are proposed, which provides a new and effective method to enhance $E_{\rm I}$ by introducing self-adaptive interface charges and so increase $V_{\rm BV}$. Compared with conventional technology of complementary metal–oxide semiconductor (CMOS), SAC SOI LDMOS only needs an additional mask and process.

2. Structure and mechanism

The SAC SOI LDMOS and its mechanism are shown in Figs. 1(a) and 1(b). The interface holes accumulating operation of the proposed SAC SOI is completely different from that in Fig. 1(c). Linear variable distance high concentration n^+-regions are made on the interface of top dielectric buried layer (SiO_2). When a high positive voltage $V_{\rm d}$ is applied to the drain, while source, gate and substrate are grounded, the n^+-regions is self-adaptive to accumulate additional charges by the vertical electric field ($E_{\rm V}$) and located in the spacing of two neighbouring n^+-regions on the interface by the force from lateral electric field ($E_{\rm L}$) and the compositive operation of Coulomb's forces with the ionized donors in the undepleted n^+-regions, electrons are induced and located on the interface of bottom dielectric buried layer (SiO_2).

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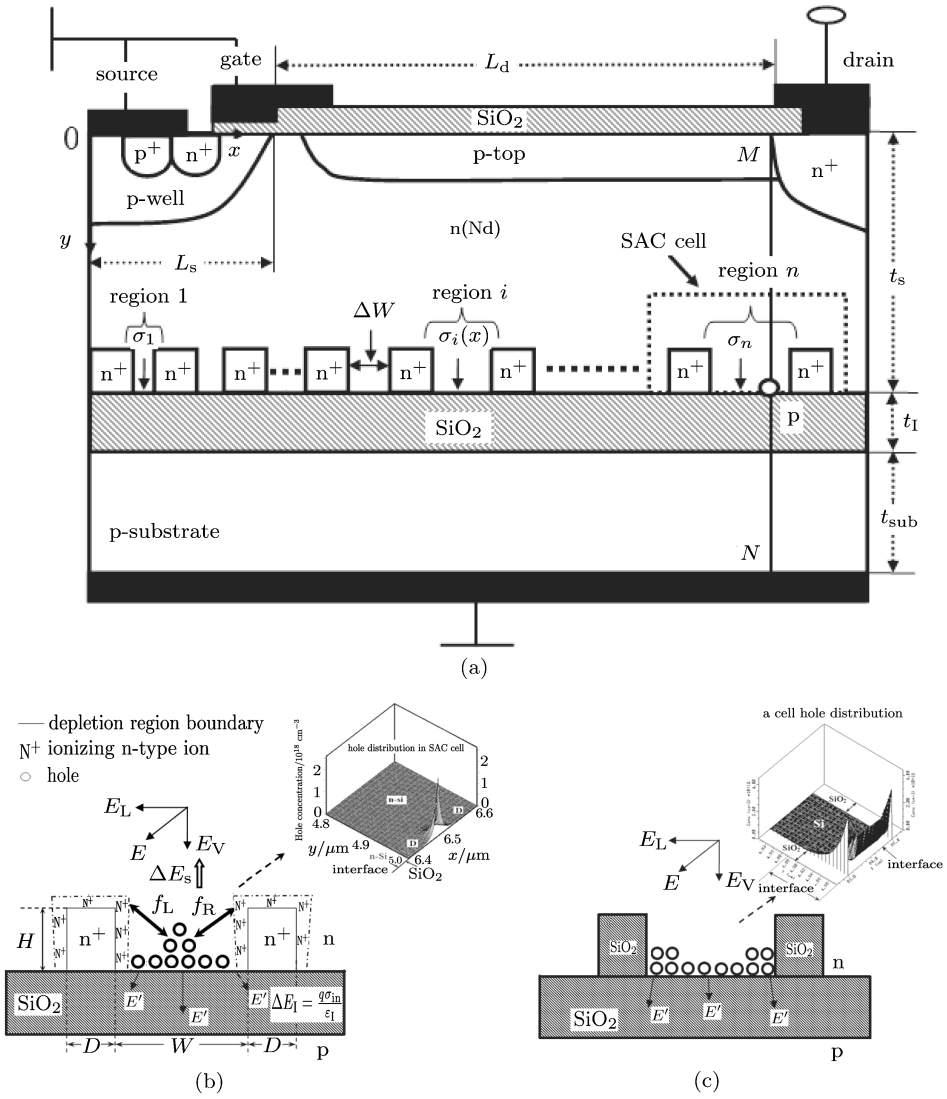


Fig. 1. Structure and mechanism of SAC SOI LDMOS: (a) device structure; (b) a cell structure and the work mechanism of SAC SOI, where E_L and E_V are the lateral and vertical electric field, f_L and f_R are the Coulomb's forces from the left and right ionizing n-type ions in the undepleted n^+-regions, respectively; (c) a cell structure and the work mechanism of DSOI/PSOI.[8,9]

Suppose that the charge density σ_{in} of each SAC cell is equal, which divide the devices into n regions as shown in Fig. 1(a): the first SAC cell with interface charge density σ_1 is region 1, while the last SAC cell (under the drain) with interface charge density $\sigma_n = \sigma_{L_d+L_S}$ is region n. When a high positive voltage V_d is applied to the drain while the source, gate and substrate are grounded, two-dimensional (2D) potential $\phi(x,y)$ in the drift region can be written as $\phi(x,y) = \omega(x,y) + \varphi(x,y)$, where $\omega(x,y)$ and $\varphi(x,y)$ are the contributions of V_d and depleted impurities in drift region, respectively, in which, $\varphi(x,y)$ satisfies 2D Poisson equation:

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_s},$$
$$0 \le x \le L_d + L_s, 0 \le y \le t_s, \quad (1)$$

where ε_s is the permittivity of silicon and q is electron charge. For fully-depleted drift region, the vertical electric field in top silicon layers

$$E_y(x,y) = -\frac{\partial\varphi(x,y)}{\partial y} = \psi_1(x) + \psi_2(x)y,$$
$$0 \le x \le L_d + L_s, 0 \le y \le t_s. \quad (2)$$

Solving Eq. (2) with the boundary conditions yields

$$\varphi(x,y) = -\frac{1}{2}\psi_2(x)y^2 + \psi_2(x)t^2 + \frac{q\sigma_i(x)t_I}{\varepsilon_I} + \varphi(x, t_s + t_I), \quad (3)$$

where $t = t_s\sqrt{0.5 + t_I\varepsilon_s/t_s\varepsilon_I}$ is the characteristic thickness of SOI/PSOI devices.

From Eq. (3), we can obtain electric potential distribution along MN as

$$\varphi(L_{\rm d}+L_{\rm s},y)=\frac{q\sigma_i(L_{\rm d}+L_{\rm s})t_{\rm I}+\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},t_{\rm s}+t_{\rm I})-\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},0)}{2\varepsilon_{\rm I}t^2}y^2+\varphi(L_{\rm d}+L_{\rm s},0). \quad (4)$$

From Eq. (4), the vertical electric field is derived as

$$E_y(L_{\rm d}+L_{\rm s},y)=\frac{\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},0)-q\sigma_i(L_{\rm d}+L_{\rm s})t_{\rm I}-\varepsilon_{\rm I}\varphi(L_{\rm d}+L_{\rm s},t_{\rm s}+t_{\rm I})}{\varepsilon_{\rm I}t^2}y. \quad (5)$$

With Eq. (5) and Gauss-theory on the interface, the electric fields in silicon and dielectric buried layer $E_{\rm s}$ and $E_{\rm I}$ of P point are obtained as

$$E_{\rm s}=\frac{t_{\rm s}}{t^2}\left[V_{\rm d}-\varphi(L_{\rm d}+L_{\rm s},t_{\rm s}+t_{\rm I})-\frac{t_{\rm I}q\sigma_{\rm L_d+L_s}}{\varepsilon_{\rm I}}\right], \quad (6)$$

$$E_{\rm I}=\frac{\varepsilon_{\rm s}t_{\rm s}}{\varepsilon_{\rm I}t^2}[V_{\rm d}-\varphi(L_{\rm d}+L_{\rm s},t_{\rm s}+t_{\rm I})]+\frac{t_{\rm s}^2q\sigma_{\rm L_d+L_s}}{2\varepsilon_{\rm I}t^2}. \quad (7)$$

From Eqs. (6) and (7), interface charge $\sigma_{L_{\rm d}+L_{\rm S}}$ in the proposed SAC SOI can enhance $E_{\rm I}$ in comparison with the conventional SOI ($\sigma_{L_{\rm d}+L_{\rm S}}=0$), while shield the silicon layer electric field $E_{\rm s}$ avoiding silicon layer premature breakdown (shown as $\Delta E_{\rm I}$ and $\Delta E_{\rm s}$ in Fig. 1(b), respectively). These all will contribute to a high breakdown voltage. Moreover, with $\sigma_{L_{\rm d}+L_{\rm S}}=0$, equations (6) and (7) can be used for the conventional SOI.

3. Results and discussion

The 2D device simulations[14] for the proposed SAC SOI LDMOS specified in Table 1 were performed to verify the device operation.

Table 1. Device parameters used in the simulation.

device parameters	SAC SOI	Con. SOI
drift length, $L_{\rm d}$	30 μm–90 μm	30 μm–90 μm
thickness of SOI layer, $t_{\rm s}$	5 μm	5 μm
thickness of Buried layer, $t_{\rm I}$	1 μm	1 μm
thickness of p-top layer, $t_{\rm p}$	0.5, 1, 1.5 μm	–
thickness of p-substrate layer, $t_{\rm sub}$	2 μm	2 μm
p-substrate concentration, $N_{\rm sub}$	3×10^{14} cm^{-3}	3×10^{14} cm^{-3}
thickness of SAC, H	0–1.2 μm	–
n^+-region length in SAC, D	0–2.5 μm	–
spacing of two neighboring n^+-region in SAC, W	1.8–2.76 μm	–
n^+-region concentration in SAC layer, N_{n^+}	1×10^{17} cm^{-3}–1×10^{19} cm^{-3}	–

From Eqs. (6) and (7), the theoretical dependence of interface charge (hole) density $\sigma_{\rm in}$ on $E_{\rm I}$ is shown in Fig. 2(a), and $\sigma_{\rm in}$ achieves a linear enhancement of $E_{\rm I}$ with a slight effect of silicon electric field $E_{\rm s}$. The $E_{\rm I}$ increases from the conventional 108 V/μm to 345.48 V/μm and 571.58 V/μm with adding $\sigma_{\rm in}$ from 0 cm^{-2} to 6.23×10^{12} cm^{-2} and 1.17×10^{13} cm^{-2}, respectively ($E_{\rm s}=30$ V/μm). Moreover, we define enhancement factor η which presents the enhanced ability of interface charge on the electric field of buried dielectric field $E_{\rm I}$ in comparison with the conventional device with $\sigma_{\rm in}=0$ cm^{-2} from Eqs. (6) and (7) as

$$\eta=1+\frac{q\sigma_{\rm in}}{\varepsilon_{\rm s}E_{\rm s}}, \quad (8)$$

where η is improved by adding $\sigma_{\rm in}$ as $E_{\rm I}$ does and reaches to 6.94 and 12.89 with $\sigma_{\rm in}=1.17\times10^{13}$ cm^{-2} for $E_{\rm s}=30$ V/μm and 15 V/μm, respectively, as shown in Fig. 2(a), that is to say, $E_{\rm I}$ has an effective increase due to interface charge. Enhancement factor of BV γ is homoplastically defined as η compared with the conventional device

$$\gamma=1+\frac{t_{\rm I}q\sigma_{\rm in}}{0.5\varepsilon_{\rm I}t_{\rm s}E_{\rm s}+\varepsilon_{\rm s}t_{\rm I}E_{\rm s}}. \quad (9)$$

For $E_{\rm s}=15$ V/μm, γ is 2.11 and 3.93 with $\sigma_{\rm in}$ of 1.99×10^{12} cm^{-2} and 5.27×10^{12} cm^{-2} as shown in Fig. 2(a), which presents that breakdown voltage is improved by twice and quadruple, respectively. Simulated results of $\sigma_{\rm in}$ and η at breakdown for SAC SOI LDMOS are shown in Fig. 2(b). The $\sigma_{\rm in}$ linearly increases from source to drain with potential at x axis and therefore, achieves a linear enhancement of $E_{\rm I}$ as Figs. 2(a) and 2(b). The η under the drain for SAC SOI reaches 18.5 because the high concentration holes, whereas η is always equal to 1 because of $\sigma_{\rm in}=0$ cm^{-2} for conventional SOI.

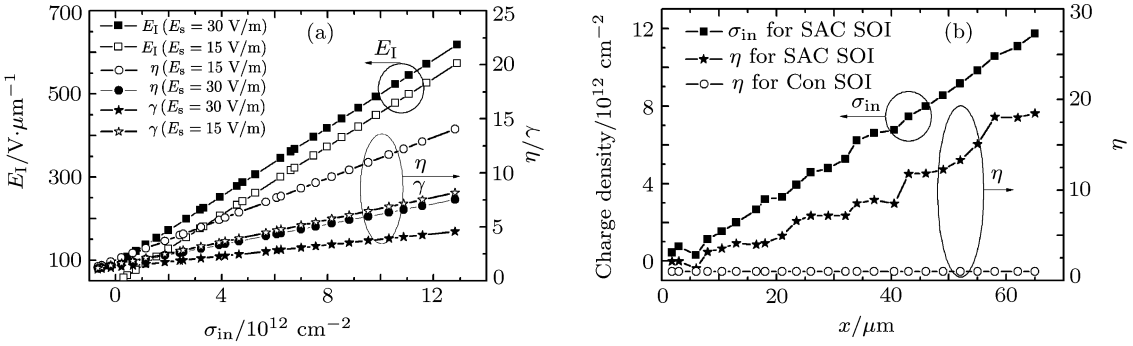


Fig. 2. Influences of charge (hole) density σ_{in} on E_I and V_{BV}: (a) theoretical dependence of σ_{in} on E_I and enhancement factors η and γ ($t_s = 5$ μm, $t_I = 1$ μm for γ); (b) simulated results of σ_{in} and η at breakdown for SAC SOI ($t_s = 5$ μm, $t_I = 1$ μm, $L_d = 61$ μm, $D = H = 0.5$ μm, $\Delta W = 0.04$ μm).

Figure 3 gives the comparison of surface electric field and the equipotential contours distributions at breakdown for the proposed SAC SOI and conventional SOI LDMOS. It is clear that equipotential contours distribution of SAC SOI is more uniform than that of conventional SOI. And, interface holes of SAC SOI effectively modulate surface electric field, which means that a more uniform surface electric field is achieved for the proposed SAC SOI than that of conventional one as shown in Fig. 3.

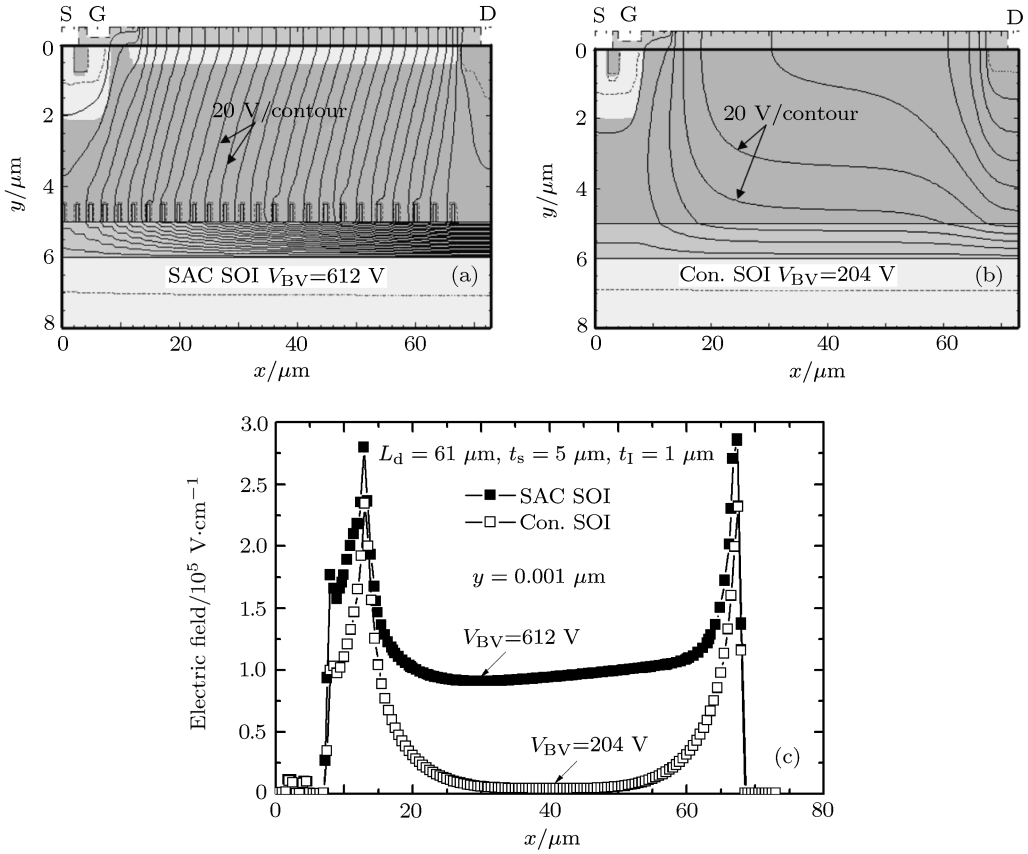


Fig. 3. Equipotential contours and surface electric fields distributions ($y = 0.001$ μm) at breakdown for SAC SOI and the conventional SOI: (a) equipotential contours distribution for SAC SOI ($N_d = 1.15 \times 10^{15}$ cm^{-3}); (b) equipotential contours distribution for the conventional SOI ($N_d = 2.6 \times 10^{15}$ cm^{-3}); (c) surface electric field distribution for the two structures.

Figure 4 shows charge distribution for the SAC SOI LDMOS at breakdown. Figure 4(a) is the hole and electron concentrations on both top and bottom interfaces of the buried dielectric layer for the SAC SOI LDMOS at breakdown. Plentiful holes are located on the top interface whose concentration increases from the source

to the drain with the increase of potential. Moreover, there are 10^{17} cm^{-3} electrons existing on the bottom interface. Figure 4(c) gives holes distribution at P point in an SAC cell under the drain, in which, inversion layer is about 90 nm. Figure 4(d) gives the dependences of holes concentration on applied voltages. With adding $V_{\rm d}$ from 100 V to $V_{\rm BV}$ (612 V), hole concentration increases, and for each $V_{\rm d}$, hole concentration is enhancive from source to drain with the increase of potential. This shows that interface hole has the self-adaptive characteristic and ability which are automatically varied with the applied voltage and effective enhancement on $E_{\rm I}$ to make the device endurable to the applied voltages.

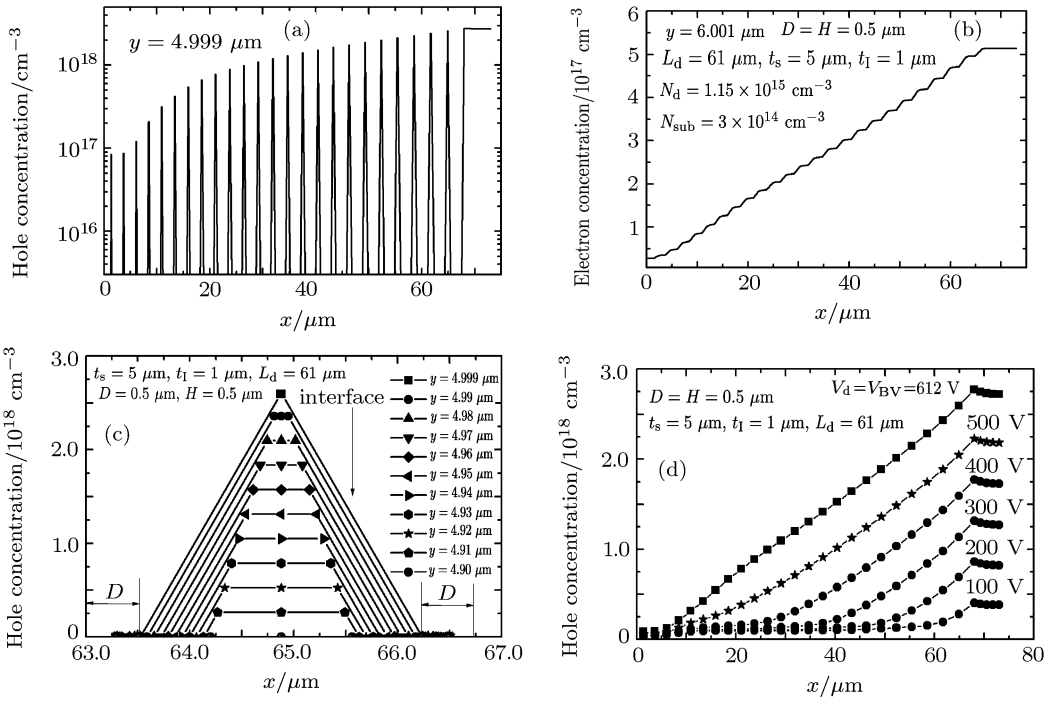


Fig. 4. Charge distribution for the SAC SOI LDMOS at breakdown ($t_{\rm s}$ = 5 μm, $t_{\rm I}$ = 1 μm, $L_{\rm d}$ = 61 μm, $D = H$ = 0.5 μm, ΔW = 0.04 μm): (a) hole/electron; (b) concentrations on both top (y = 4.999 μm) and bottom (y = 6.001 μm) interfaces of the buried dielectric layer; (c) hole distribution in an SAC cell with different vertical distances under the drain; (d) hole concentrations vs. $V_{\rm d}$ of middle of every SAC cell.

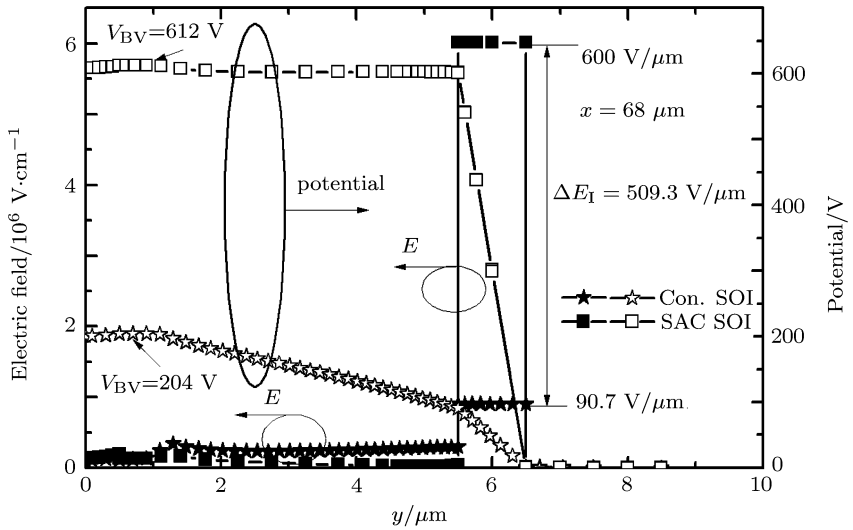


Fig. 5. Vertical electric field and potential distributions at breakdown under the drain ($t_{\rm s}$ = 5 μm, $t_{\rm I}$ = 1 μm, $L_{\rm d}$ = 61 μm, $D = H$ = 0.5 μm, ΔW = 0.04 μm).

Figure 5 is the vertical electric field and potential distributions at breakdown under the drain. The $E_{\rm I}$ increases from 90.7 V/μm of the conventional SOI to 600 V/μm of SAC SOI, which results in a beakdown

voltage of 612 V for SAC SOI in comparison with 204 V for the conventional SOI. Voltage shared by buried dielectric layer ($V_{\rm I} = t_{\rm I}E_{\rm I} = 600$ V) is above 90% of breakdown voltage. Inversion charges reduce Si layer electric field $E_{\rm s}$ to 3.63 V/μm and avoid Si layer premature breakdown.

Figure 6(a) shows vertical electric fields in Si ($E_{\rm SV}$) and SiO_2 ($E_{\rm IV}$) on the top interface along x axis. For SAC SOI, $E_{\rm I}(x)$ increases with the increase of holes concentration of Fig. 6 from source to drain. Therefore, $E_{\rm IV}$ is much larger than $3E_{\rm SV}$ under the drain in comparison with the conventional dependence of $E_{\rm IV} = 3E_{\rm SV}$. $E_{\rm SV}(x)$ for each point is almost invariable because of a series of $n^+n^-n^+$-structures (SAC cell) with a sustainingly applied voltage of 20 V as shown in Fig. 3, and $E_{\rm SV}(x)$ is less than 30 V/μm due to the shielding effect of holes, whereas those of conventional SOI increase from source to drain with the increase of potential and reach to 30 V/μm under the drain where breakdown occurs ($x = 67.94$ μm). Breakdown point for SAC SOI is at $x = 13.10$ μm because of high lateral electric field. Enhancement of holes on $E_{\rm I}$ can be clearly seen from three-dimensional distribution of electric field shown in Fig. 6(b).

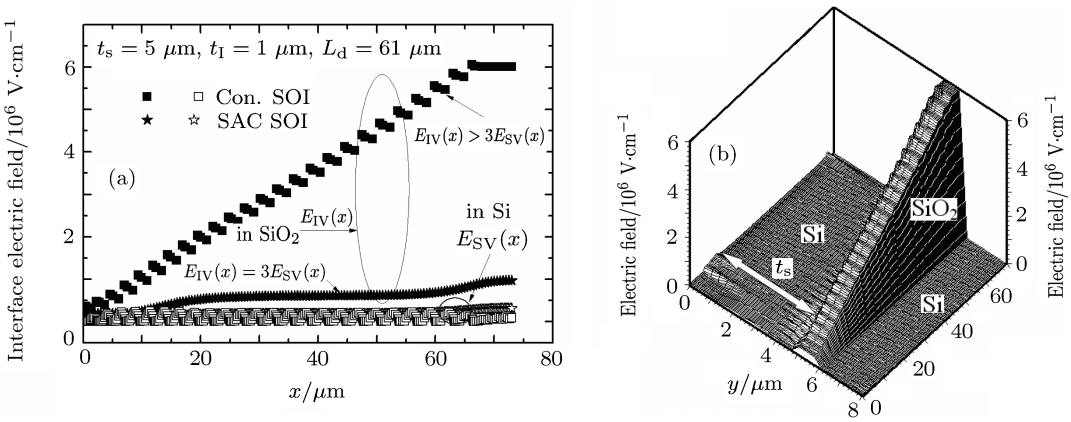


Fig. 6. Electric field distribution at breakdown ($t_{\rm s} = 5$ μm, $t_{\rm I} = 1$ μm, $L_{\rm d} = 61$ μm, $D = H = 0.5$ μm): (a) vertical electric fields in Si ($E_{\rm SV}$) and in SiO_2 ($E_{\rm IV}$) on the top interface; (b) three-dimensional distribution of electric field.

Figure 7 shows the influences of $N_{\rm n^+}$ (concentration of n^+-regions) on $V_{\rm B}$, $E_{\rm I}$ and the maximal hole concentration $N_{\rm h,m}$. It can be seen that when $N_{\rm n^+}$ is larger than 2.1×10^{18} cm^{-3}, $V_{\rm B}$ is invariable as well as $E_{\rm I}$ and $N_{\rm h,m}$. When $N_{\rm n^+}$ is less than 2.1×10^{18} cm^{-3}, $V_{\rm B}$ decreases with the decrease of $N_{\rm n^+}$. The reason can be explained as follows: when $N_{\rm n^+}$ is larger than 2.1×10^{18} cm^{-3}, the n^+-regions under the drain are undepleted and the ionized donors are invariable, that is independent of $N_{\rm n^+}$.

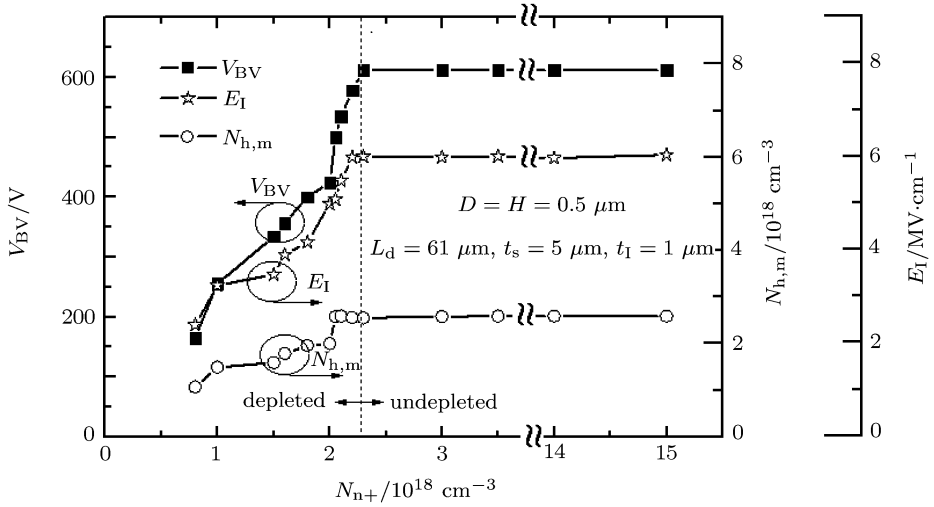


Fig. 7. Influences of interface n^+-regions concentration $N_{\rm n^+}$ on breakdown voltage, $E_{\rm I}$ and the maximal hole concentration $N_{\rm h,m}$.

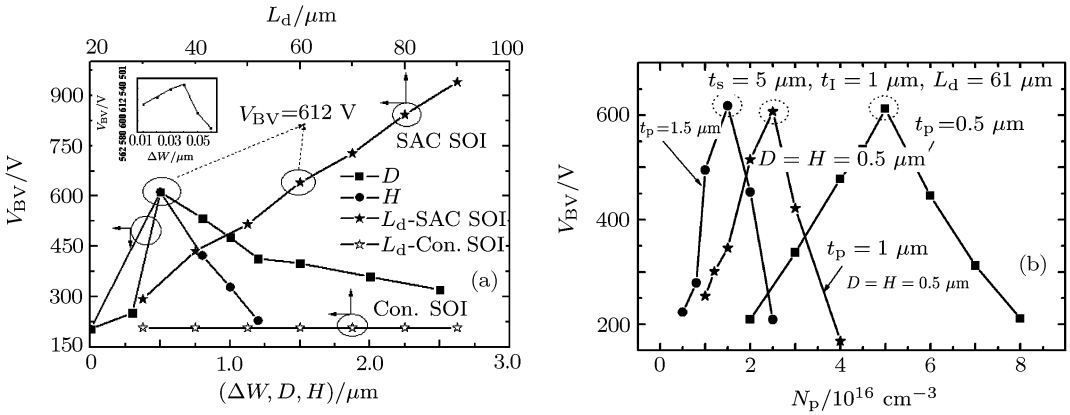


Fig. 8. Influences of device parameters on breakdown voltage. $t_s = 5\ \mu$m, $t_I = 1\ \mu$m, $t_{sub} = 2\ \mu$m for all: (a) H, D and L_d on breakdown voltage. $L_d = 61\ \mu$m for H and D. $H = D = 0.5\ \mu$m for L_d. $N_{sub} = 3 \times 10^{14}$ cm^{-3} for all; (b) N_p (with $N_{sub} = 3 \times 10^{14}$ cm^{-3}) and N_{sub} on breakdown voltage. $H = D = 0.5\ \mu$m, $\Delta W = 0.04\ \mu$m and $L_d = 61\ \mu$m for all.

Figure 8 shows the influences of structure parameters on V_{BV} for the SAC SOI. Figure 8(a) shows the influences of H, D, ΔW and L_d on V_{BV}. It can be seen from Fig. 8(a) that there is a maximum $V_{BV} = 612$ V with $H = D = 0.5\ \mu$m, $\Delta W = 0.04\ \mu$m, and V_{BV} is improved with the increase of L_d which breaks through the breakdown voltage of the conventional SOI just shown in Fig. 8(a), too. Moreover, when H or D is 0 μm, SAC SOI becomes a conventional SOI whose V_{BV} only 204 V. Figure 8(b) shows the influences of the p-top layer. The maximal V_{BV} are almost equal for different p-top layer thicknesses (t_p) of 0.5, 1 and 1.5 μm. In addition, the maximal V_{BV} appears when $N_p \times t_p$ is about 2.5×10^{12} cm^{-2} which satisfies the RESURF (REduced SURface Field) condition, and after that, V_{BV} sharply decreases because of premature breakdown at n^+–p junction of the drain side.

The major steps of the process flow are depicted in Table 2, and the associated device cross sections are shown in Fig. 9 for the SAC SOI LDMOS. Start from two silicon wafers (wafer 1 and wafer 2). First the ⟨100⟩ silicon wafer 1 with n^+-regions formed by implanting 2×10^{15} cm^{-2} arsenic at 180 keV (shown in Table 2). The thickness of the n^+-regions after masked implantation processing is estimated as 500 nm. Then wafer 2 is thermally oxidized. Wafer 2 has an oxide layer on bottom, wafer 1 has linear variable distance arsenic implantation on top, these two wafers are bonded together using van der Walls forces at 1180 °C for 3 hours in an oxidizing atmosphere. Finally, the wafer is annealed at high temperature, then thinned and polished the wafer 1 to 5 μm. Therefore, only an additional process of arsenic implantation before bonding is needed to form SAC SOI. Other fabrication processes are fully compatible with conventional CMOS/SOI technology.

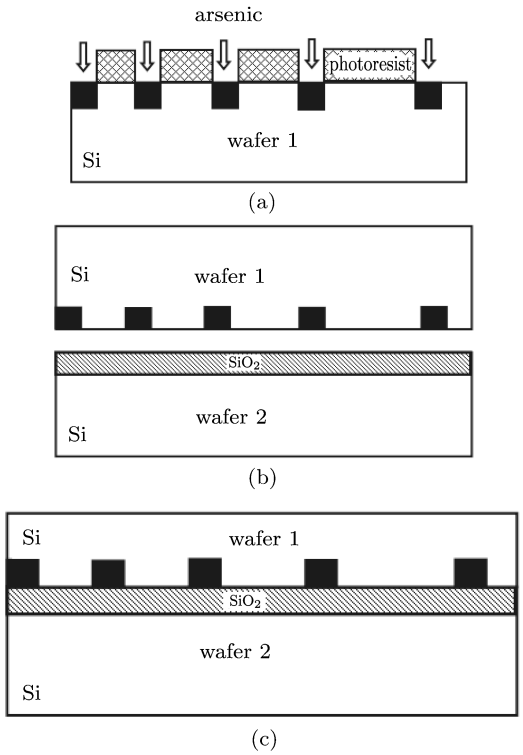


Fig. 9. Schematic principle of SAC SOI technology: (a) linear variable distance arsenic implantation; (b) thermal oxidizing, cleaning and bonding; (c) annealing, then thinning and polishing wafer 1.

Table 2. Summary of process flow.

process flow	parameter	SOI wafers	units
wafer 1			
arsenic implantation	n^+-regions dose	2×10^{15}	cm^{-2}
	n^+-regions energy	180	keV
	n^+-regions thickness	0.5	μm
p-well implantation	boron-dose	1×10^{13}	cm^{-2}
	boron-energy	150	keV
p-top implantation	boron-dose	1.65×10^{12}	cm^{-2}
	boron-energy	50	keV
p-well & p-top drive in	time	1.3	hours
gate polysilicon deposition	temperature	1138	°C
n^+ source/drain implantation	thickness	0.5	μm
	arsenic-dose	1×10^{16}	cm^{-2}
	arsenic-energy	100	keV
p^+ body contact implantation	boron-dose	5×10^{15}	cm^{-2}
	boron-energy	80	keV
Al deposition	thickness	1	μm
wafer 2			
substrate layer	silicon thickness	2	μm
	boron-dose	1.5×10^{10}	cm^{-2}
buried layer	BOX SOI thickness	1	μm
bonding wafer 1 & wafer 2			
high-temperature SDB and thinning	SDB temperature	1180	°C
polishing	SDB time	3	hours

4. Conclusion

A high-voltage linear variable distance SAC SOI has been presented, and its breakdown mechanism has been investigated. The SAC SOI effectively utilizes the enhancement effect of the interface charges on the electric field of the dielectric buried layer to increase breakdown voltage. The $E_{\rm I}$ increases from 90.7 V/μm of the conventional SOI to 600 V/μm of SAC SOI, which results in a breakdown voltage of 612 V for SAC SOI compared with 204 V for the conventional SOI with the same $t_{\rm s}$, $t_{\rm I}$ and $L_{\rm d}$. The preparation of the SAC SOI wafer has been discussed.

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