The modulation effect of substrate doping on multi-node charge collection and single-event transient propagation in 90-nm bulk complementary metal-oxide semiconductor technology*

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Variation of substrate background doping will affect the charge collection of active and passive MOSFETs in complementary metal-oxide semiconductor (CMOS) technologies, which are significant for charge sharing, thus affecting the propagated single event transient pulsewidths in circuits. The trends of charge collected by the drain of a positive channel metal-oxide semiconductor (PMOS) and an N metal-oxide semiconductor (NMOS) are opposite as the substrate doping increases. The PMOS source will inject carriers after strike and the amount of charge injected will increase as the substrate doping increases, whereas the source of the NMOS will mainly collect carriers and the source of the NMOS can also inject electrons when the substrate doping is light enough. Additionally, it indicates that substrate doping mainly affects the bipolar amplification component of a single-event transient current, and has little effect on the drift and diffusion. The change in substrate doping has a much greater effect on PMOS than on NMOS.

Keywords: substrate doping, charge collection, single event transient propagation, bipolar amplification

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1. Introduction

Single-event transient (SET) is the main radiation-induced noise and source of soft errors in advanced complementary metal-oxide semiconductor (CMOS) integrated circuits (ICs).[1−4] The transmission of SET in combinational logic circuits causes the system output to detect errors. The SETs on cross-coupled inverters' nodes may cause storage cells such as static random access memory (SRAM) and flip–flop occurring single-event upset (SEU). The SET becomes one of the key factors sensitive to single-event effects (SEEs) in ICs. The characteristics of SET and SEU should be taken into account for designing radiation-hardened ICs. As transistor density increases on chip in each new technology, the probability of a single particle causing SET in a circuit or depositing charge on multiple nodes increases.[5−8] Previous works in 130-nm and 90-nm bulk CMOS show the existence of charge sharing and how dual interlocked cell (DICE) latches are vulnerable to upsets in these technologies.[9,10]

Experimental work at 130 nm shows that charge sharing can affect the pulsewidths of propagated SET,[11] and this mechanism is called pulse quenching. Mixed-mode three-dimensional (3D) technology computer-aided design (TCAD) simulations at 90-nm technology node show that pulse quenching can occur at normal incidence for minimally spaced and sized circuits. Recent experimental data and simulations show that pulse quenching is more prevalent in the common N-well design than in the separate N-well design, leading to significantly reduced SET pulsewidths and SET cross-section in the common N-well design.[12]

For bulk CMOS technology, many parameters will affect the charge generation and collection process after particle strike. Studies show that heavily doped P^+ deep wells can improve SEU threshold for SRAM cells.[13] Bulk potential and minority carrier mobility can be modulated by the substrate doping. Many research works have been carried out

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to study the impact of substrate concentration on the charge collection.[14−16] The most fundamental method for hardening against SEU can be accomplished by introducing extra doping to limit substrate charge collection.[14] The dependence of the collection mechanisms on the substrate doping and reverse bias level of n^+–p junction is discussed in Ref. [15]. Reference [16] studied the effect of substrate doping on SET pulses shape in 130-nm N metal-oxide semiconductor field effect transistor (NMOSFET). As technology feature size scales to nanometers, the charge sharing effect becomes particularly notable. Substrate doping will affect the charge collection of both active and passive devices, thus the SET pulsewidths propagated in circuit will be affected. It is significant to discuss the substrate doping on propagated SET pulsewidths.

This paper first studies the impact of substrate doping on propagated SET pulsewidths, compares the amount of charge collected by PMOS and NMOS with the change of substrate background doping, and analyses the impact of substrate doping on various mechanisms during the charge collection process. Secondly, it verifies that the source of PMOS will inject carriers after strike and the amount of charge injected will increase as the substrate doping increases, whereas the source of NMOS will mainly collect carriers. Finally, it indicates that the substrate doping mainly affects the bipolar amplification component of SET current, and has little effect on the drift and diffusion. The change of substrate doping has a much greater effect on PMOS than on NMOS.

2. Related works

A three-stage inverter chain is shown in Fig. 1; each of the output nodes of the inverter is labeled as out1, out2, and out3, respectively. Assume a low input to the chain. At first, the P3 of Inv3 is on, the P2 of Inv2 is off, and out2 is low. If a particle strikes the off-state P2 drain, the low state at out2 is driven to high due to the charge collection and an SET pulse is generated. The SET pulse will be propagated to Inv3, causing a transition at out3 from high to low and P3 turns off. When P3 becomes off, it will collect the charge generated from the struck P2. Because of charge sharing effect, the state of out3 will jump to high. This low-to-high transition at out3 "resets" the node voltage to the pre-event state, and the pulse at out3 is truncated, or quenched by the delayed charge collection.[11]

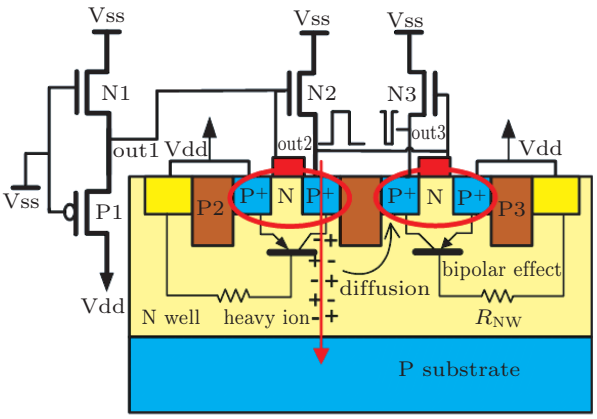


Fig. 1. (colour online) A chain of inverters illustrating the change in SET pulse width during the propagation.

Two factors will affect the voltage of out3 node dynamically. One is the electrical signal of the SET pulse propagated from out2; the other is the delayed charge collection at out3 due to charge sharing from the struck node out2. The propagated SET pulsewidths are determined by these two factors. Since the occurrence of quenching is caused by multi-node charge collection, it is necessary to understand substrate background doping on the impact of multi-node charge collection, which may offer important guidance for designing anti-SET/SEU ICs.

3. Simulation setup

Device simulation is an effective means to study the generation and propagation of the SET pulse. In this paper, Synopsys TCAD 3D mixed simulation is employed to study the characteristics of SET propagated in an inverter chain. The 90-nm CMOS bulk technology used in this paper is the same as that in Ref. [17]. Device model parameters are consistent with other transistor models in which the same technology is used. The doping profiles are calibrated within the 3D model by process simulation and an inverse modeling approach,[18] and they are consistent with the I–V characteristics between TCAD and simulation program with integrated circuit emphasis (SPICE) simulations. The PMOS struck by particles and the adjacent PMOS use the 3D model whereas other NMOS and PMOS transistors use the SPICE model. The following physical models are used: (i) Fermi–Dirac statistics; (ii) band–gap narrowing effect, (iii) doping dependent Shockley–Read–Hall (SRH) recombination and Auger recombination; (iv) temperature, doping, electric field, and carrier–carrier-scattering impacts on mobility; (v) incident heavy ions which are modeled

using a Gaussian radial profile with a characteristic 1/e radius of 30 nm and a Gaussian temporal profile with a characteristic decay time of 0.5 ps. All simulations are conducted on a YINHE high-performance computing cluster.

4. Substrate doping on SET pulse propagation

A 3D dual-PMOS model is designed, shown in Fig. 2. The PMOS struck by particles is called the active device, and the adjacent device is called the passive device. This dual-PMOS model is used to replace P1 and P2 in Fig. 1, while the SPICE model is used for other transistors. Figure 3 shows the SET voltage pulsewidths at out2 and figure 4 shows that the SET pulsewidths propagated to out3 change with substrate doping. The value of LET is 40 MeV·cm^2/mg, and spacing between P2 and P3 is 0.14 μm which is the minimum spacing of layout design rule. It can be seen from Figs. 3 and 4 that the SET pulsewidths at out2 and out3 change greatly with the fluctuation of substrate doping, and the trends at the two nodes are totally opposite. From the view of inhibition SET propagation, the SET propagated to out3 can be migrated by increasing the substrate concentration, despite the fact that it can enhance the SET pulsewidths at out2.

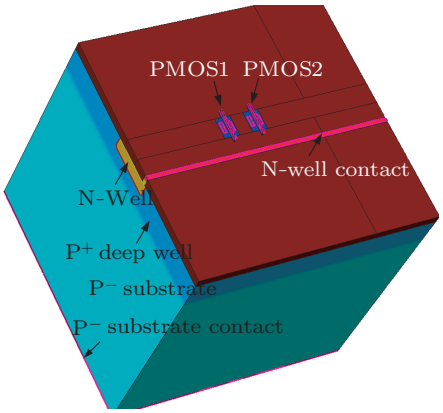


Fig. 2. (colour online) A 3D dual-PMOS model for 90-nm bulk CMOS.

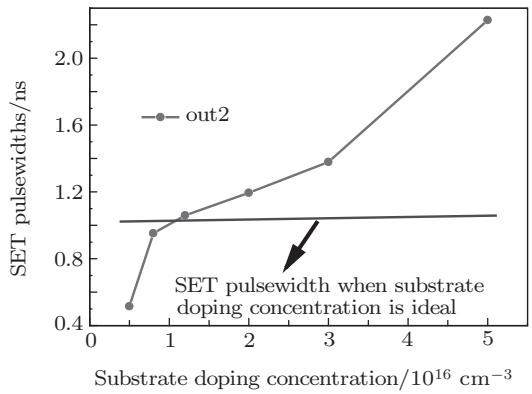


Fig. 3. The relationship between pulsewidths of out2 node and substrate doping.

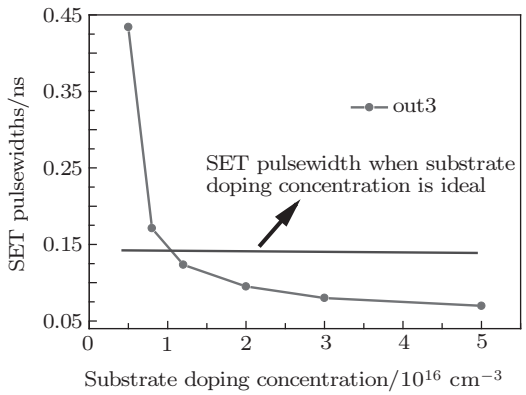


Fig. 4. The relationship between pulsewidths of out3 node and substrate doping.

5. Analysis of results

5.1. The impact of substrate doping on mobility

The doping concentration can affect the mobility of carriers, shown in Eq. (1). The mobility will decrease as the concentration increases, so the current density in device will be affected due to Eq. (2),

$$\mu = \frac{q}{m_*} \frac{1}{AT^{3/2} + BN_i/T^{3/2}}, \tag{1}$$

$$J = \sigma|E| = nq\mu|E|. \tag{2}$$

Lattice scatter is the main mechanism for mobility when the concentration N_i is less than 10^{19} cm^{-3}, and the impurity scatter $BN_i/T^{3/2}$ can be ignored. So the effect of a lightly doped substrate on mobility can be reasonably ignored.

To ensure the effect of substrate doping on mobility is not the key factor governing the amount of charge collected, simulations are implemented using a constant mobility and doping-dependent model, respectively. The results are shown in Fig. 5. Indeed, the change ranges for both models are almost identical which emphasizes that the difference in the amount of

collected charge at different substrate doping is mainly not due to the doping dependence of the mobility.

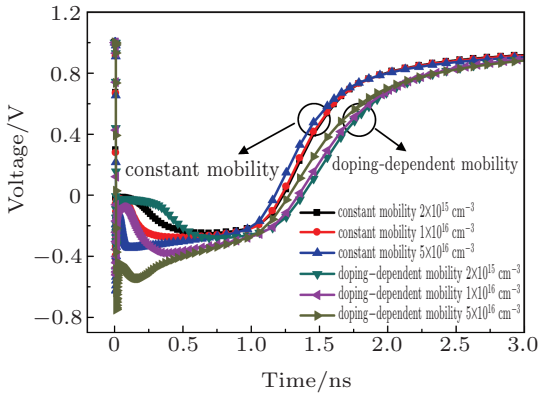


Fig. 5. (colour online) The effect of mobility on SET pulsewidths.

5.2. The impact of substrate doping on the charge-sharing effect

The quenching strength is determined by charge sharing directly. In order to study the impact of substrate doping on SET pulsewidths, the relationship between substrate doping and charge sharing should be considered first. The two PMOS are both set to off-state, which means that the gate, source, and N-well contacts are tied to high, and the substrate and drain are tied to low. There is no connection between them and the layout spacing is 0.14 μm. The amount of charge collected by active and passive PMOS at different substrate doping is calculated, shown in Table 1.

Table 1. The amount of charge collected by active and passive PMOS at different substrate doping.

Change time of substrate doping	Charge collected by active device when doping changes/fC	Change rate	Charge collected by passive device when doping changes/fC	Change rate
×1	430.12	0	122.7	0
×0.2	260.35	–39.5%	30.12	–75.5%
×0.5	302.06	–29.8%	45.21	–63.2%
×0.8	389.22	–9.5%	95.51	–22.2%
×1.2	459.92	6.9%	144.14	17.5%
×2	554.63	28.9%	212.88	73.5%
×5	1046.24	143.2%	614.45	400.1%

In order to compare with PMOS, the amount of charge collected by active and passive NMOS at different substrate doping is calculated, shown in Table 2. For PMOS, it shows that the amount of charge collected by the active and passive device changes greatly with the substrate doping, and for passive PMOS this is especially obvious. When the doping changes 0.5 or 2 times relative to the baseline, the amount of charge collected by passive PMOS changes by more than 50%. For NMOS, as the substrate concentration changes, the amount of charge collected by the passive device will be larger than by the the active device, but both changes are indistinct in comparison with PMOS. Additionally, the change trends of charge collection for NMOS and PMOS are almost opposite as the substrate increases.

It is revealed from Table 1 and Table 2 that the substrate doping will affect the charge collection, and the mechanism of charge collection can be classified as drift, diffusion or bipolar amplification. So substrate concentration must be related to part of the charge collection mechanism. Previous studies[19−20] show that the bipolar amplification is dominant during the PMOS charge collection process, and drift and diffusion are dominant during NMOS charge collection for CMOS technology. The change of PMOS charge collection is significantly higher than for NMOS with the fluctuation of substrate doping, and it can be concluded that substrate concentration mainly affects the bipolar amplification mechanism. On the other hand, substrate doping can reduce the substrate effects on well potential effectively. The distribution of well potential is different for different substrate doping after particle strike. Bulk potential will affect the conduction level of the parasitic bipolar transistor, thus affecting the degree of bipolar amplification, so the substrate doping has great influence on the charge collected by PMOS while it has little influence on NMOS.

Table 2. The amount of charge collected by active and passive NMOS at different substrate doping.

Change time of substrate doping	Charge collected by active device when doping changes/fC	Change rate	Charge collected by passive device when doping changes/fC	Change rate
×1	754.2	0	284.6	0
×0.2	875.78	16.1%	375.97	32.1%
×0.5	804	6.6%	319.88	12.4%
×0.8	770	2.1%	294.83	3.6%
×1.2	743.2	–1.5%	277.41	–2.5%
×2	716.74	–5.0%	261.18	–8.2%
×5	685.77	–9.1%	238.54	–16.2%

The charge collected by active PMOS comes from the source and N-well while the passive PMOS is mainly from source. This is because the particle strikes active PMOS directly. In addition to bipolar amplification components, there are drift and diffusion current components. While the passive PMOS is far from the struck node, the SET current is mainly supplied by the bipolar amplification effect. So the change of charge collection by passive PMOS is much larger than for active PMOS with the change of substrate doping.

As the substrate doping increases, the charges collected by active and passive PMOS are both increased, so the SET pulsewidths are increased at out2. The charge collected by passive PMOS is much larger than for active PMOS, thus passive PMOS collects much more charge and the charge-sharing effect is stronger. While charge sharing can be utilized by the quenching effect to migrate SET propagation, charge sharing is stronger, the quenching effect is more significant, and the SET pulsewidths are also smaller. Therefore, increasing the concentration of substrate may increase the SET pulsewidths at out2, but it leads SET pulsewidths to be smaller when propagated to out3. Whether the strike events can be latched by subsequent latch, upset the SRAMs, or be captured by the timing unit is determined by the propagated SET pulsewidths, which are the key factors for soft error rate (SER).

5.3. The impact of substrate doping on bipolar amplification

In order to verify the effect of substrate doping on bipolar amplification component of SET current, the sources of PMOS and NMOS are removed to form P–N junction structures which are called p^+n junction and n^+p junction, respectively. The structure eliminates the bipolar amplification effect completely which is a conventional means for SET current analysis.

Table 3 shows the charge collected by PMOS and p^+n junction at different substrate doping. It infers that the amount of charge collected by p^+n junction will be much less than PMOS for a given doping, and the charge collected by the n^+p junction will be larger than by NMOS, but the distinction is not obvious, which is shown in Table 4. This is mainly because the charge collection of PMOS is determined by bipolar amplification and the existence of the source plays a decisive role. The charge collection of NMOS is determined by drift and diffusion and the presence of the source has little effect. The change rate of charge collected by PMOS is quite different from p^+n with the fluctuation of substrate doping. For NMOS and n^+p, with the concentration fluctuation, the change rate of charge collection is almost identical. The results show that the substrate doping mainly affects bipolar amplification component in the charge collection process.

Table 3. Charge collected by PMOS and p^+n junctions at different substrate doping.

Change times of substrate doping	Charge collected by p^+n junction when doping changes/fC	Change rate	Charge collected by PMOS when doping changes/fC	Change rate
×1	181.21	0	448.27	0
×0.2	201.22	11.0%	260.1	–42.0%
×0.5	188.2	3.9%	296.83	–33.8%
×0.8	183.1	1.0%	398.77	–11.0%
×1.2	179.7	–0.8%	485.66	8.3%
×2	176.93	–2.4%	595.92	32.9%
×5	172.85	–4.6%	1149.7	156.5%

Table 4. Charge collected by NMOS and n^+p junctions at different substrate doping.

Change times of substrate doping	Charge collected by n^+p junction when doping changes/fC	Change rate	Charge collected by NMOS when doping changes/fC	Change rate
×1	916.41	0	775.43	0
×0.2	831.17	–9.3%	862.18	11.2%
×0.5	880.44	–3.9%	813.14	4.9%
×0.8	904.92	–1.3%	788.0	1.6%
×1.2	921.03	0.5%	767.14	–1.1%
×2	924.23	0.9%	743.27	–4.1%
×5	933.36	1.8%	711.59	–8.2%

The charge injected by the source for NMOS and PMOS at different substrate doping is shown in Table 5. We can observe that the source of PMOS injects a large number of holes into the N-well and most of them will be collected by the drain, but the situation for NMOS is totally different. The negative value means that the source collects electrons, and the source of NMOS will collect electrons instead of injection for most cases. The amount of charge injected (or collected) is quite different with the change of substrate doping for both NMOS and PMOS.

Table 5. Charge injected by the source for NMOS and PMOS at different substrate doping.

Change times of substrate doping	Charge injected by source when doping changes/fC (PMOS)	Change rate (PMOS)	Charge injected by source when doping changes/fC (NMOS)	Change rate (NMOS)
×1	604.54	0	–124.02	0
×0.2	108.1	–82.12%	110.11	–188.78%
×0.5	204.18	–66.23%	–18.46	–85.12%
×0.8	452.4	–25.17%	–90.41	–27.1%
×1.2	736.66	21.85%	–149.97	20.92%
×2	1193.06	97.35%	–217.76	75.58%
×5	2854.5	372.18%	–300.85	142.58%

Note that substrate doping can affect not only the bipolar amplification of PMOS, but also the NMOS device. The following section will discuss this issue in detail.

5.4. The impact of substrate doping on charge collection

Figure 6 shows the cutting directions perpendicular to the drain and source centre, respectively, labeled as cut A and cut B. The electrostatic potential of PMOS is plotted along cut A 50 ps after strike at three different substrate dopings, shown in Fig. 7.

The static potential distribution is different 50 ps after strike with change of substrate doping for PMOS. The potential mainly drops on the reversed drain-well junction since the N-well contact is tied to high, and the electron–hole pairs in the N-well which are similar to plasma will keep the potential at the same level for

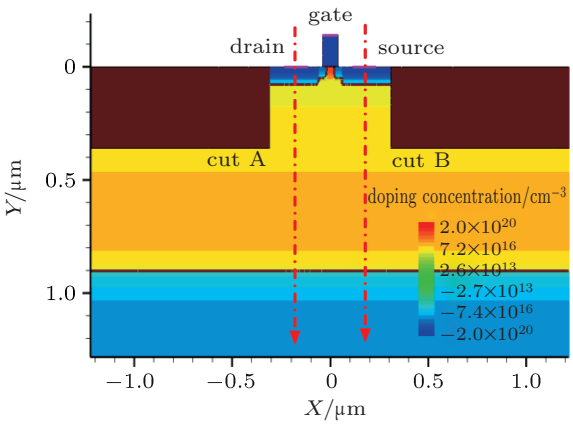


Fig. 6. (colour online) The cutting directions perpendicular to the PMOS drain and source centre.

a certain range of depth. Since the substrate contact is tied to low, as the depth increases, the electrostatic potential will return to equilibrium gradually. Because of the existence of the metal semiconductor work function, the potential in drain and body will be less than 0 V. The electron concentration in the N-well will reduce as the substrate doping increases, and depletion region will spread toward the N-well, so the funnel region contributing to the drift also extends; thus the potential in bulk will be much closer to that in the drain region. This is the reason why the potential in bulk will reduce as the substrate doping increases, as shown in Fig. 7.

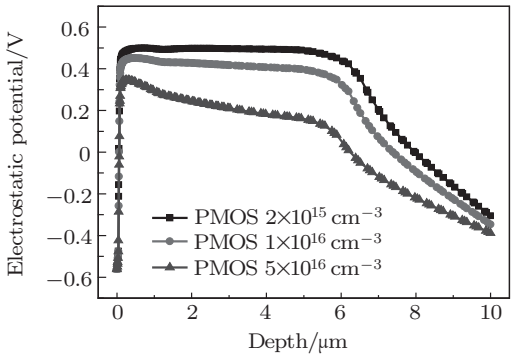


Fig. 7. The electrostatic potential distribution plotted along cut A 50 ps after strike for PMOS at three different substrate dopings.

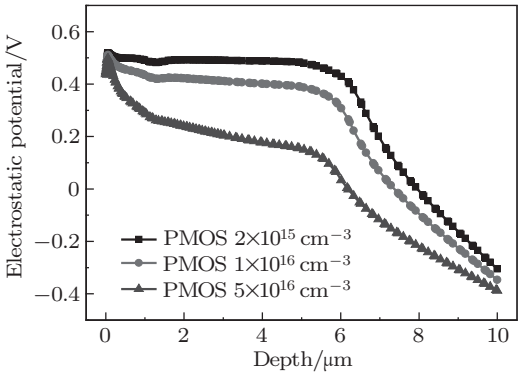


Fig. 8. The electrostatic potential distribution is plotted along cut B 50 ps after strike for PMOS at three different substrate dopings.

The electrostatic potential of PMOS along cut B will reduce as the substrate doping increases, shown in Fig. 8, similar to the potential along cut A. For PMOS, the source is tied to high, when the potential difference of source–well junction is greater than 0.6 V, the parasitic PNP bipolar transistor will turn on and holes will inject into the N-well from the source, thus most injected holes will be collected by the drain of PMOS. The voltage drops on the source-well junction is much larger when the substrate doping is greater, so the electric field increases in the depletion region, shown in Fig. 9. The charge injected by the source will also increase as the electric field increases, so the amount of charge is much greater in heavier substrate doping, as shown in Table 5.

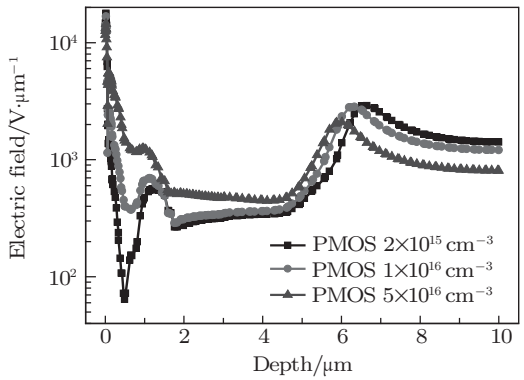


Fig. 9. The electric field distribution plotted along cut B 50 ps after strike for PMOS at three different substrate dopings.

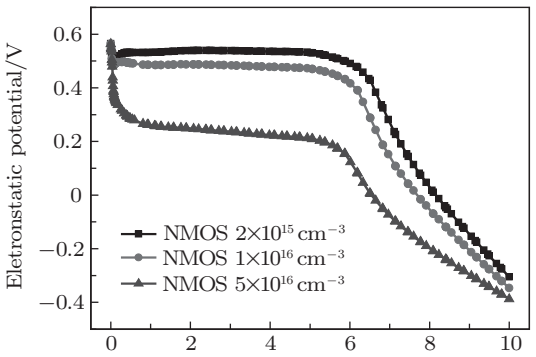


Fig. 10. The electrostatic potential distribution plotted along cut B 50 ps after strike for NMOS at three different substrate dopings.

The potential of NMOS along cut B will reduce with the substrate doping, shown in Fig. 10. For NMOS, the source is tied to low. When the potential difference of source–substrate junction is less than −0.6 V, the parasitic PNP bipolar transistor will turn on and electrons will inject to substrate from the source. On the other hand, because of the existence of metal semiconductor work function, the potential in substrate will be less than 0 V, and it will be larger than 0 V in the source. Thus the source–substrate junction will reverse and the source will start to collect electrons instead of injection.

Figure 11 reveals the electric field distribution along cut B at different substrate dopings for NMOS. For source–substrate junction, the diffusion in the barrier mainly occurs in the P-type substrate region, and

the maximum electric field in the depletion region is shown as

$$E_{\rm m} = -\frac{qN_{\rm A}x_n}{\varepsilon_r\varepsilon_0} = -\frac{Q}{\varepsilon_r\varepsilon_0} = -\sqrt{\frac{2qN_{\rm A}(V_{\rm D}-V)}{\varepsilon_r\varepsilon_0}}, \quad (3)$$

where x_n is the barrier width in the P-type substrate region, $N_{\rm A}$ is the hole concentration of substrate and $V_{\rm D}$ is the potential difference of the P–N junction contact. The electric field will increase as the concentration $N_{\rm A}$ increases, so the amount of charge collected by the NMOS source will be much greater for the heavily doped substrate.

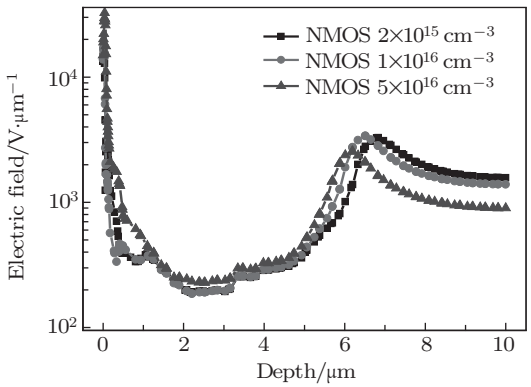


Fig. 11. The electric field distribution plotted along direction cut B 50 ps after strike for NMOS at three different substrate dopings.

6. Conclusion

Variation of substrate background doping will affect the charge collection of active and passive MOSFETs in CMOS technologies, which is significant for charge sharing, thus affecting the propagated SET pulsewidths in circuits. The trends of charge collected by the drain of PMOS and NMOS are just opposite as the substrate doping increases. The source of PMOS will inject carriers after strike and the amount of charge injected will increase as the substrate doping increases, whereas the source of NMOS will mainly collect carriers. This is because the parasitic bipolar transistor for PMOS is PNP, which can be turned on easily when the potential of the N-well fluctuates, and the drain will collect most of the holes from the source. For NMOS, the parasitic bipolar transistor is NPN and the existence of the metal semiconductor work function will turn the NPN off. The source will collect electrons in most cases and the amount of charge collected will increase as the substrate doping increases, so the drain will collect much fewer charges with heavier doping. Note that the source of NMOS can also inject electrons when the doping of substrate is light enough. Additionally, it indicates that substrate doping mainly affects the bipolar amplification component of SET current, and has little effect on the drift and diffusion. The change of substrate doping has a much greater effect on PMOS than on NMOS.

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