A novel planar vertical double-diffused metal-oxide-semiconductor field-effect transistor with inhomogeneous floating islands*

Ren Min(任 敏)†, Li Ze-Hong(李泽宏), Liu Xiao-Long(刘小龙), Xie Jia-Xiong(谢加雄), Deng Guang-Min(邓光敏), and Zhang Bo(张 波)

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, *China*

(Received 23 June 2011; revised manuscript received 10 July 2011)

A novel planar vertical double-diffused metal-oxide-semiconductor (VDMOS) structure with an ultra-low specific on-resistance ($R_{on,sp}$), whose distinctive feature is the use of inhomogeneous floating p-islands in the n-drift region, is proposed. The theoretical limit of its $R_{on,sp}$ is deduced, the influence of structure parameters on the breakdown voltage (BV) and $R_{on,sp}$ are investigated, and the optimized results with BV of 83 V and $R_{on,sp}$ of 54 mΩ·mm^2 are obtained. Simulations show that the inhomogeneous-floating-islands metal-oxide-semiconductor field-effect transistor (MOSFET) has a superior "$R_{on,sp}$/BV" trade-off to the conventional VDMOS (a 38% reduction of $R_{on,sp}$ with the same BV) and the homogeneous-floating-islands MOSFET (a 10% reduction of $R_{on,sp}$ with the same BV). The inhomogeneous-floating-islands MOSFET also has a much better body-diode characteristic than the superjunction MOSFET. Its reverse recovery peak current, reverse recovery time and reverse recovery charge are about 50, 80 and 40% of those of the superjunction MOSFET, respectively.

Keywords: inhomogeneous floating islands, specific on-state resistance, breakdown voltage, body diode reverse recovery

PACS: 85.30.Tv, 85.30.De **DOI:** 10.1088/1674-1056/20/12/128501

1. Introduction

Power metal-oxide-semiconductor field-effect transistors (MOSFETs) are widely used as switches in power systems such as DC–DC converters. Therefore, MOSFETs are required not only to have a high breakdown voltage (BV), but also a low on-resistance, as well as a body diode with superior reverse recovery characteristics to suppress radio noise and voltage surges.[1] A trade-off relationship exists between specific on-state resistance and BV for conventional power MOSFETs. Many groups have reported superjunction (SJ) MOSFETs to improve the trade-off characteristic.[2−5] SJ-MOSFETs, however, have two major drawbacks, the hardness of the body-diode reverse–recovery operation and the difficulty of fabrication. The hardness of reverse recovery with an abrupt current drop imposes electrical stress upon the other circuit elements, producing large electromagnetic interference noise and high-power dissipation.[6]

Recently, a new concept named the floating-islands MOSFET (FLIMOS), in which floating islands are placed into the drift region, has been proposed to reduce on-state resistance without degrading breakdown voltage.[7−10] The additional PN junctions, formed by buried P-type floating islands (FI) in the drift region, sustain a higher blocking voltage, and the high doping concentration in the drift region reduces $R_{on,sp}$. Alves *et al.*[8] implemented a FLIMOS with a single floating island dedicated to automotive applications using a two-step epitaxy process. Compared to the conventional vertical double-diffused metal-oxide-semiconductor (VDMOS), a 33% reduction in the $R_{on,sp}$ for the same BV was obtained. Theoretically, the breakdown voltage can be improved with an increase in the number of floating islands.[7] In order to achieve a better "$R_{on,sp}$/BV" trade-off, Luo *et al.*[9] proposed a trench gate power MOSFET with double buried p-islands, whose widths, thicknesses and doping concentrations are uniform, by using the

*Project supported by the National Key Scientific and Technological Project (Grant No. 2011ZX02503-005) and the Fundamental Research Funds for the Central Universities (Grant No. ZYGX2010J038).

†Corresponding author. E-mail: renmin@uestc.edu.cn

© 2011 Chinese Physical Society and IOP Publishing Ltd

self-alignment process. In this paper, we propose an inhomogeneous FLIMOS (I-FLIMOS), whose distinctive feature is the inhomogeneous FI in the n-drift region. Compared with the homogeneous FLIMOS (H-FLIMOS), higher BV can be obtained by optimizing the electronic field distribution of I-FLIMOS, and lower $R_{\rm on,sp}$ can be achieved due to the wider current path. The trade-off between BV=83 V and $R_{\rm on,sp} = 54$ mΩ·mm^2 of the I-FLIMOS is superior to that reported in Ref. [8].

Although there is much research on the static characteristics of the FLIMOS, its dynamic characteristics need to be explored thoroughly. The reverse–recovery characteristics of the body diodes in the I-FLIMOS have been analysed, and the I-FLIMOS has shown remarkable advantages in comparison with the conventional SJ structure. Otherwise, the fabrication process of I-FLIMOS is simpler than that of the SJ structure. The proposed I-FLIMOS is therefore a very attractive candidate for power systems, thanks to its low $R_{\rm on,sp}$ and better recovery body-diode characteristics.

2. Device structure and process

The I-FLIMOS features separated buried inhomogeneous floating p-islands in the n-type drift region. The D_n (n = 1, 2, 3, ...) is the distance of the n-th buried p-island from the surface, while T_n and W_n represent its thickness and width, respectively. Figure 1(a) shows the schematic cross-section of an I-FLIMOS with two inhomogeneous floating p-islands ($n = 2$).

The FLIMOS is not strictly based on the charge compensation principle,[8] and therefore the control of impurity concentration in the FLIMOS is not as rigorous as that in the SJ devices. Compared to the process of alternate boron implantation and n-epitaxial growth for several turns to form the p-columns in the SJ structure, FLIMOS fabrication has advantages in both cost and complexity. Analogous to the H-FLIMOS shown in Fig. 1(c), the two floating p-islands are realized either by the implantation–epitaxial–implantation process, or by two-step ion implantations with different energies. However, an additional mask is needed to achieve the inhomogeneous floating p-islands.

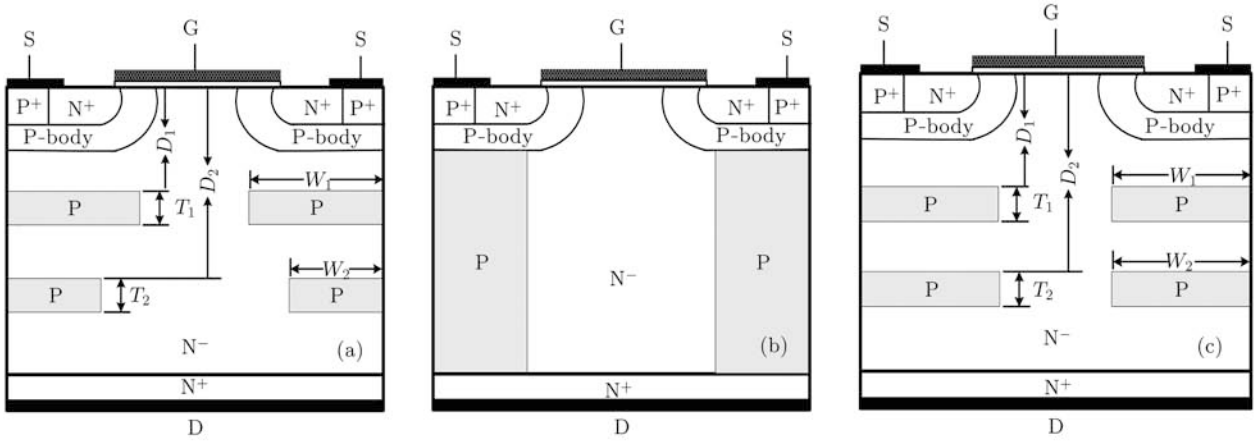


Fig. 1. Schematic diagram of the cross sections of (a) an I-FLIMOS with two buried inhomogeneous floating p-islands; (b) an SJ-MOSFET; and (c) an H-FLIMOS with two homogeneous floating p-islands.

3. Simulation and discussion

3.1. "$R_{\rm on,sp}$/BV" trade-off

The electric field distributions of I-FLIMOS, conventional VDMOS, H-FLIMOS and SJ-VDMOS with approximately equal BVs are shown in Fig. 2. The floating islands improve the BV due to the similar mechanism of floating field-limiting rings (FFLR) in the planar terminations. Under reverse bias conditions, once the depletion region from the P-body reaches the floating island, the potential of the island is enhanced and then the new depletion layer develops from the bottom of the island towards the drain.[8] Thus, the maximal electric field at the P-body/N-epi junction is divided into three electric field peaks, and the BV of the I-FLIMOS is shared by three vertical PN

junctions. In FFLR technology, we can modulate the spacing, width and doping of the rings to achieve an optimized structure whose breakdown voltage is much higher than that of the structure with uniform rings. Similarly, the I-FLIMOS is promising in obtaining a better "$R_{\rm on,sp}$/BV" trade-off than the H-FLIMOS.

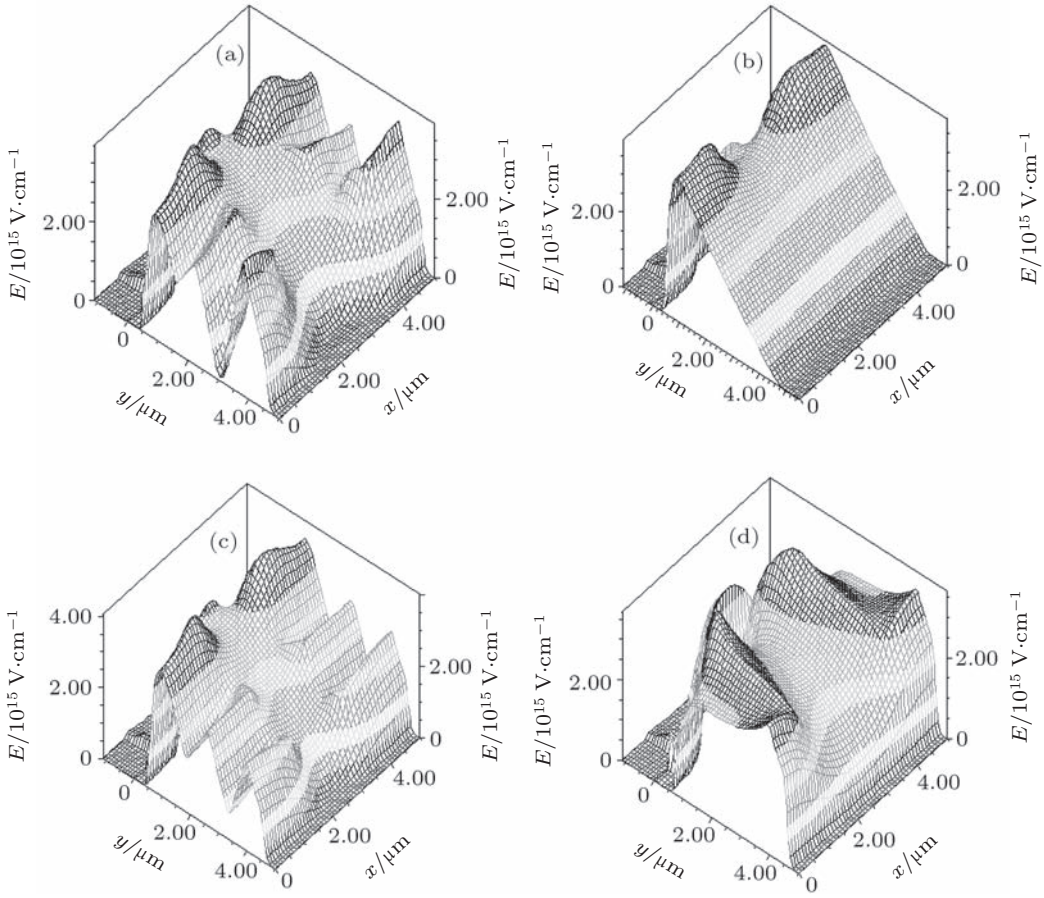


Fig. 2. The electric field distribution: (a) I-FLIMOS; (b) conventional VDMOS; (c) H-FLIMOS; and (d) SJ-VDMOS at $V_{\rm gs} = 0$ and $V_{\rm ds} = {\rm BV}$.

The conventional VDMOS has a "silicon limit" of $R_{\rm on,sp} \propto {\rm BV}^{2.5}$, and the "$R_{\rm on,sp}$/BV" theoretical limit of the H-FLIMOS has been calculated by Cézac *et al.*[7] For the FLIMOS with "n" floating islands in the drift region, the breakdown voltage is equally supported by $(n+1)$ PN junctions. Since the conduction section is reduced compared to a conventional VDMOS, the limit of the drift region resistance of the H-FLIMOS is then equal to:

$$R_{\rm D_H} \approx \frac{L_{\rm a} + L_{\rm b}}{L_{\rm a}} (n+1)^{-1.5} R_{\rm D,lim}, \qquad (1)$$

where $R_{\rm D_H}$ and $R_{\rm D,lim}$ are the drift region resistances of FLIMOS and conventional VDMOS, respectively; $L_{\rm a}$ and $L_{\rm b}$ are the length of the poly and P-body in the half cell, respectively, as shown in Fig. 3.

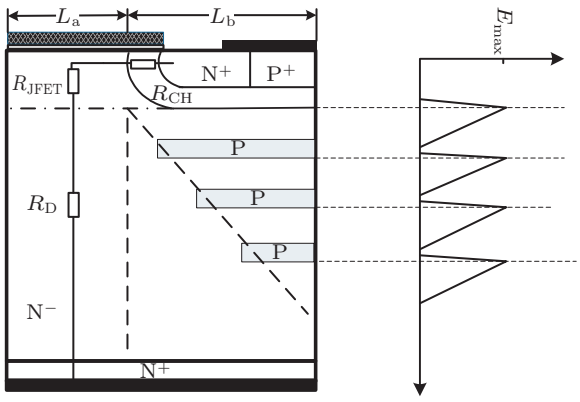


Fig. 3. The resistance of an I-FLIMOS. For the I-FLIMOS with "n" floating islands in the drift region, the BV is approximately equally supported by the $(n+1)$ PN junctions.

In the I-FLIMOS, the compression of the conduction section by the p-islands is less than that in the H-FLIMOS. Therefore, the theoretical limit of the I-

FLIMOS drift region resistance ($R_{\mathrm{D_I}}$) is

$$R_{\mathrm{D_I}} \approx \frac{2L_{\mathrm{a}}+2L_{\mathrm{b}}}{2L_{\mathrm{a}}+L_{\mathrm{b}}}(n+1)^{-1.5}R_{\mathrm{D,lim}} \approx \frac{2L_{\mathrm{a}}}{2L_{\mathrm{a}}+L_{\mathrm{b}}}R_{\mathrm{D_H}}. \quad (2)$$

Obviously, with the increase in n, the "$R_{\mathrm{on,sp}}$/BV" trade-off is improved; on the other hand the fabrication process is more difficult. But for low-voltage applications, the I-FLIMOS can obtain a better "$R_{\mathrm{on,sp}}$/BV" trade-off with a slightly higher fabrication cost.

The simulated BV and $R_{\mathrm{on,sp}}$ of the I-FLIMOS, conventional VDMOS, SJ-VDMOS and H-FLIMOS are shown in Table 1. The device parameters are the best choice in terms of "$R_{\mathrm{on,sp}}$/BV" trade-off, according to two-dimensional (2D) simulations. The I-FLIMOS has a 38% reduction in $R_{\mathrm{on,sp}}$ relative to the conventional structure because it can obtain the same BV with a higher N-epi doping concentration. It also had a 10% reduction in $R_{\mathrm{on,sp}}$ relative to the H-FLIMOS due to the wider current path. Figure 4 shows the current flow lines distribution in these devices at $V_{\mathrm{gs}} = 10$ V and $V_{\mathrm{ds}} = 0.1$ V.

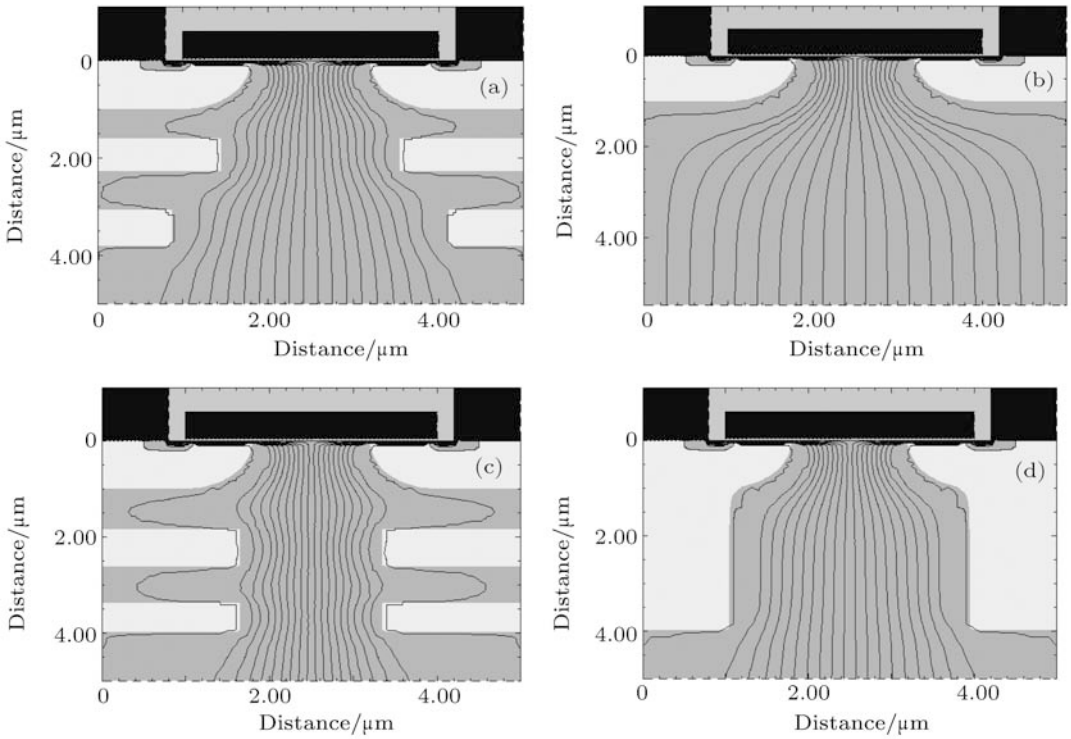


Fig. 4. The current flowlines: (a) I-FLIMOS; (b) conventional VDMOS; (c) H-FLIMOS; and (d) SJ-VDMOS at $V_{\mathrm{gs}} = 10$ V and $V_{\mathrm{ds}} = 0.1$ V.

Table 1. The main device parameters and simulated $R_{\mathrm{on,sp}}$ and BV of the I-FLIMOS, conventional VDMOS, H-FLIMOS and SJ-VDMOS.

Parameters	I-FLIMOS	Conventional VDMOS	H-FLIMOS	SJ-VDMOS
N-epi thickness/μm	4.0	4.5	4.0	4.0
N-epi doping concentration/cm^{-3}	1.5×10^{16}	6×10^{15}	1.5×10^{16}	1.6×10^{16}
The 1st FI doping concentration/cm^{-3}	3×10^{16}	–	3×10^{16}	–
The 2nd FI doping concentration/cm^{-3}	6×10^{16}	–	3×10^{16}	–
P-column doping concentration/cm^{-3}	–	–	–	2×10^{16}
Distance of P-body to the 1st FI/μm	0.6	–	0.8	–
Distance of the 1st FI to the 2nd FI/μm	0.8	–	0.7	–
The 1st FI width W_1/μm	1.6	–	1.7	–
The 2nd FI width W_2/μm	0.8	–	1.7	–
The P-column width/μm	–	–	–	1.0
The 1st FI thickness T_1/μm	0.7	–	0.7	–
The 2nd FI thickness T_2/μm	0.7	–	0.7	–
Cell size/μm	5	5	5	5
V_{ds}/V	83	82	83	82
$R_{\mathrm{on,sp}}$/mΩ·mm^2	54	87	60	51

3.2. Process tolerance

Although the SJ-VDMOS has an approximately linear relation between $R_{\rm on,sp}$ and BV, Praveen *et al.* pointed out that the device is highly sensitive to charge imbalance.[4,11] I-FLIMOS has a significant advantage over SJ-VDMOS because the boron implantation dose control of the p-island does not have to be severely controlled to compensate the space charges in the N-drift layers. We investigated the sensitivity of BV to the process deviation. The simulated results are shown in Fig. 5.

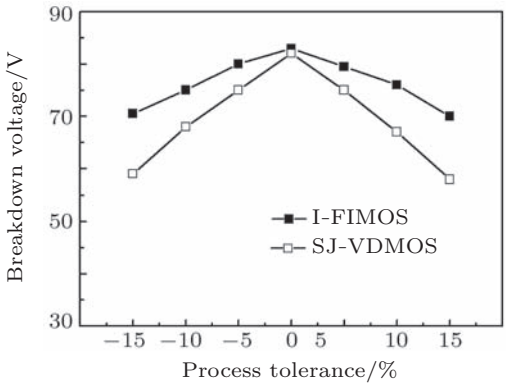


Fig. 5. The sensitivity of BV to the process deviation for SJ-VDMOS and I-FLIMOS.

3.3. Body-diode characteristics

One of the disadvantages of the SJ-MOSFET is its bad body-diode reverse recovery. The P-columns in the epitaxial layer enlarge the P/N junction area, resulting in a high injection of minority carriers to the N-drift region. The injected electron–hole plasmas have to be almost completely removed before the device starts to sustain reverse voltage, which gives rise to a large reverse recovery charge. The drain/source capacitance ($C_{\rm ds}$) of SJ-VDMOS changes rapidly during the reverse recovery process. The $C_{\rm ds}$ shows a very large value at low drain–source voltages. And it falls drastically as drain–source voltage increases and the internal P/N column structure starts to deplete. Therefore, SJ-VDMOS has an abrupt current drop and a hard reverse recovery.

The I-FLIMOS is expected to have a better body-diode characteristic because the floating p-islands are isolated from the source electrode. The injection of minority carriers from the p-islands to the N-drift is negligible. According to the body-diode reverse recovery test circuit provided by ST Microelectronics Corp.,[12] the reverse–recovery processes of I-FLIMOS and SJ-VDMOS were simulated by Medici. As shown in Fig. 6, SJ-VDMOS has a much higher peak reverse–recovery current, which is undesirable from the point of view of the applications. The reverse–recovery peak current ($I_{\rm rrm}$), reverse–recovery time ($T_{\rm rr}$) and reverse recovery charge ($Q_{\rm rr}$) of the I-FLIMOS are about 50, 80 and 40% of those of the SJ-VDMOS, respectively.

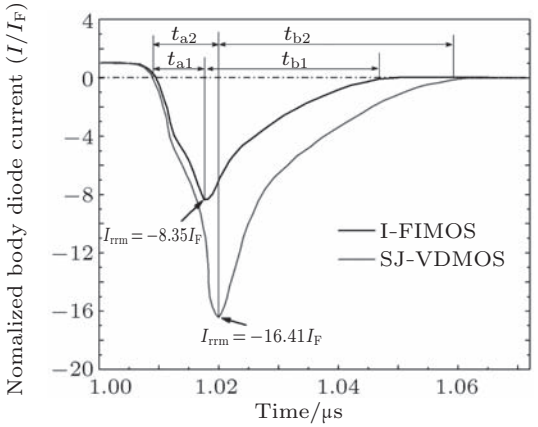


Fig. 6. The normalized body-diode reverse–recovery waveforms of the I-FLIMOS and SJ-VDMOS with the parameters in Table 1.

4. Conclusion

A novel inhomogeneous FLIMOS transistor with an ultra-low specific on-resistance is proposed. Although additional masks may be needed for the fabrication, more design freedom is provided. Simulations show that the I-FLIMOS exhibits a better "$R_{\rm on,sp}$/BV" trade-off than the conventional VDMOS and H-FLIMOS. In particular, it has better body-diode characteristics than the SJ-VDMOS. Charge balance is difficult to achieve in a practical manufacturing situation, so I-FLIMOS is a competitive alternative to SJ-VDMOS in the low-voltage field.

References

[1] Takaya H, Miyagi K and Hamada K 2005 *Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs* May 23–26, 2005 Santa Barbara, p. 43
[2] Duan B X, Zhang B and Li Z J 2007 *Chin. Phys.* **16** 3754
[3] Wang C L and Sun J 2009 *Chin. Phys.* B **18** 1231
[4] Shenoy P M, Bhalla A and Dolny G M 1999 *Proceedings of the 11th International Symposium on Power Semiconductor Devices and ICs* May 26–28, 1999 Toronto, Canada p. 99
[5] Gao Y, Ma L, Zhang R L and Wang D F 2011 *Acta Phys. Sin.* **60** 047303 (in Chinese)

[6] Saito W, Omura I, Aida S, Koduki S, Izumisawa M, Yoshioka H and Ogura T 2005 *Proceedings of the 17th I nternational Symposium on Power Semiconductor Devices and ICs* May 23–26, 2005 Santa Barbara, USA p. 27

[7] Cezac N, Morancho F, Rossel P, Tranducand H and Peyre Lavigne A 2000 *Proceedings of the 12th International Symposium on Power Semiconductor Devices and ICs* USA, Toulouse, France, May 22–25, 2000 p. 69

[8] Alves S, Morancho F, Reynes J M, Margheritta J, Deram I, Isoird K and Tranduc H 2006 *The European Conference on Power Electronics and Applications* September 11–14, 2005, Dresden, Germany p. 10

[9] Luo X R, Fu D P, Gao H M and Chen X 2010 *IEEE International Conference on Communications, Circuits and Systems (ICCCAS)*, July 28–30, 2010 Chengdu, China, p. 496

[10] Galadi A, Morancho F and Hassani M M 2008 *Semicond. Sci. Technol.* **23** 045017

[11] Fang J, Qiao M and Li Z J 2006 *Acta Phys. Sin.* **55** 3656 (in Chinese)

[12] ST Microelectronics Corp. www.stmicroelectronics.com.cn