Research on the electrical characteristics of an organic thin-film field-effect transistor based on alternating-current resistance*

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In this article, an organic thin-film field-effect transistor (OTFFET) with top-gate and bottom-contact geometry based on pentacene as the active layer is fabricated. The experimental data of the I–V are obtained from the OTFFET device. The alternating-current (AC) resistance value of the OTFFET device is calculated using the derivation method from the experimental data, and the AC resistance trend curves of the OTFFET device are obtained with the region fitting method. We analyse the characteristics of the OTFFET device with an AC resistance trend curve. To discover whether it has a high resistance, it is proposed to judge the region of the source/drain voltage ($V_{\rm DS}$) less than the transition voltage, thereby determining whether the contact between the metal electrode and the organic semiconductor layer of the OTFFET device is Ohmic or non-Ohmic. The theoretical analysis shows that the field-effect mobility and the AC resistance are in reverse proportion. Therefore, we point out that reducing AC resistance is necessary if field-effect mobility is to be improved.

Keywords: organic thin-film field-effect transistor, alternating-current resistance, Ohmic contact

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1. Introduction

Organic thin-film field-effect transistors (OTFFETs) are particularly interesting for their potential applications in smart cards, radio-frequency identification tags and driving circuits for flat-panel displays.[1,2] In particular, some basic and key issues have been intensively studied, such as interfacial energy level alignment between organic materials and inorganic materials, contact resistance at the interface between the active layer and the metal electrode, and the effect of evaporation conditions on the molecular arrangement on commonly used substrates.[3−5] Organic electronic devices have progressed rapidly in the past few years. According to reports, OTFFETs based on pentacene as an active layer have shown high field-effect mobility and on/off current ratio values comparable to amorphous silicon.[6−8] It is well known that the electrical properties of OTFFETs are reflected by field-effect mobility, threshold voltage and on/off current ratio. However, these parameters cannot be refined to describe carrier transport processes such as the interfacial situation between the source/drain electrodes and the organic active layer, the relation between gate-voltage and channel conductivity, and the saturated formation. In this paper, we report on a method with which alternating-current (AC) resistance is gained from the output characteristic curve of OTFFETs, and the AC resistance trend curve is obtained through region fitting. We may directly infer the active status of OTFFETs under the different biases using the AC resistance trend curve.

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2. Experiment

According to Refs. [9] and [10], we fabricated a bottom-contact pentacene OTFFET with a top-gate structure on a glass substrate. The entire component was manufactured on a glass basis. The first step was that ITO source/drain electrodes were deposited on the glass substrate. The channel was formed using the lithographic method. The ratio of channel width to channel length, W/L of the OTFFET, was chosen to be 10000 μm/500 μm. The thickness was 80 nm. The second step was that pentacene was deposited on the ITO source/drain electrode as an active layer. To obtain pentacene thin film, we used thermal evaporation of a 98%-purity commercial source in a high vacuum of 2×10^{-3} Pa through a self-organized process. The thickness of the pentacene thin film was 100 nm. The third step was that the gate insulator layer (SiO_2) was made by electron beam evaporation. The thickness of the gate insulator layer was 350 nm. Finally, an aluminium gate electrode of 110 nm was deposited on the gate insulator layer across the shadow mask by thermal evaporation. All the thin films were prepared at low temperature (< 100 °C) and low deposition rate (≤ 0.06 nm/s). The bottom-contact pentacene OTFFET with a top-gate structure is shown in Fig. 1.

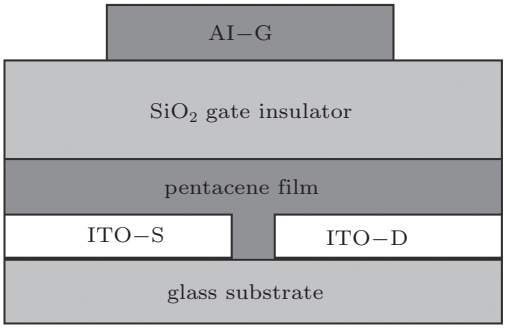


Fig. 1. A pentacene OTFFET device with a top-gate structure.

The output characteristic measurements of the OTFFET were performed with a Keithley 2410 and 6430 Source Meter Parameter Analyser in darkness at room temperature. Figure 2 shows the source/drain current (I_{DS}) versus source/drain voltage (V_{DS}) of the OTFFET device with ITO used as the source/drain electrodes at different values of gate voltage (V_{GS}). The OTFFET device shows typical p-channel characteristics. As can be seen, the output characteristics display clear saturation currents, each of which behave as a quadratic function of gate bias.

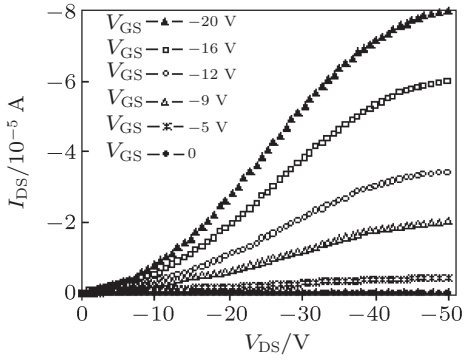


Fig. 2. The output characteristics of the OTFFET device at different values of V_{GS} and V_{DS}.

3. AC resistance and discussion

The AC resistance (r) of the OTFFET device is defined as V_{DS}/I_{DS} ratio values at a fixed value of V_{GS}, and expressed as

$$r = \left.\frac{\mathrm{d}V_{DS}}{\mathrm{d}I_{DS}}\right|_{V_{GS}} \approx \left.\frac{\Delta V_{DS}}{\Delta I_{DS}}\right|_{V_{GS}}.$$

By the above equation, AC resistances corresponding to different values of V_{DS} were extracted from the output characteristics of the OTFFET device at a fixed value of V_{GS}. The plots of AC resistance versus V_{DS} for the OTFFET device with different values of V_{GS}: (a) $V_{GS} = -12$ V, (b) $V_{GS} = -16$ V and (c) $V_{GS} = -20$ V, are shown in Fig. 3.

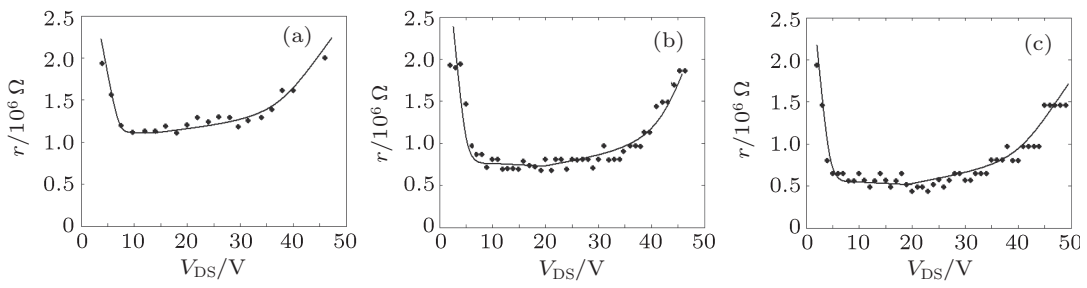


Fig. 3. AC resistances corresponding to different values of V_{DS}.

Figure 3 shows that the AC resistance values are scattered in distribution rather than continuously distributed along a smooth curve, owing to the measurement errors. The AC resistance trend curves (solid line) are obtained through the region fitting method. Three AC resistance trend curves were drawn in Fig. 4.

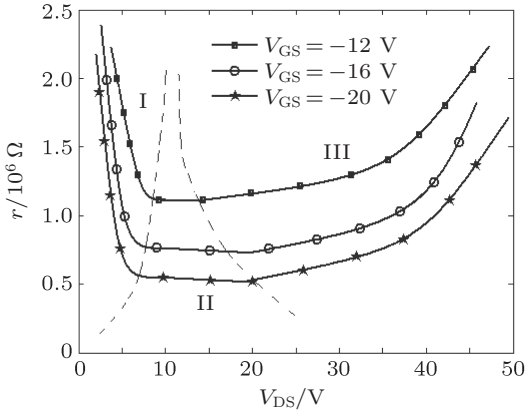


Fig. 4. AC resistance trend curves of the OTFFET device.

The AC resistance trend curves are divided into three regions: high resistance areas (area I), constant resistance areas (area II), and increased resistance areas (area III), as shown in Fig. 4. They are discussed below.

3.1. High resistance area

The high resistance area corresponds to the AC resistance of the OTFFET device at low drain/source voltage V_{DS} ($V_{DS} < V_T$), where V_T is the transition voltage between the high resistance area and the constant resistance area. The occurrence of the high resistance state means that the contact between the source/drain electrodes and the organic semiconductor is a non-Ohmic contact. The Schottky barrier at the interface is formed since the work function of metal electrodes is different from the activation energy of the organic semiconductor.[11–13] The barrier arises on the hole carrier injection side, that is, at the source electrode.[14] Since the barrier hinders hole carriers from being injected from the metal electrode into the organic semiconductor, the OTFFET device presents a high resistance state. However, the external source/drain voltage can reduce the barrier, so the AC resistance of the OTFFET device decreases as the source/drain voltage increases. In this region the AC resistance (r) of the OTFFET device is the sum of the barrier resistance (R_s), contact resistance (R_c) and channel resistance (R_{ch}). In the areas $V_{DS} < V_T$, the following expression is used to describe the resulting resistance:[15]

$$r = R_s + R_c + R_{ch}.$$

Because the measurement of the output characteristic curve is based on the source electrode serving as a public terminal, and the gate voltage is applied between the gate and the source electrodes, the horizontal component of the gate voltage makes a certain contribution to the reduction of the barrier. Therefore, the transition voltage (V_T) decreases with the increase in gate voltage (V_{GS}).

For comparison, we obtain the output characteristic and AC resistance trend curves of the inorganic field-effect transistor (ITFT) as shown in Fig. 5. This device model is MTP2P50. Since the contacts of the interfaces between the source/drain electrode and the semiconductor layer are Ohmic contacts, there is no high resistance area in the AC resistance trend curve of the ITFT at the low drain/source voltage V_{DS} ($V_{DS} < V_T$), as shown in Fig. 5(b). Thus, by observing whether a high resistance area exists in the AC resistance trend curve, we can determine whether the contact of interface of the OTFFET device is Ohmic or non-Ohmic.

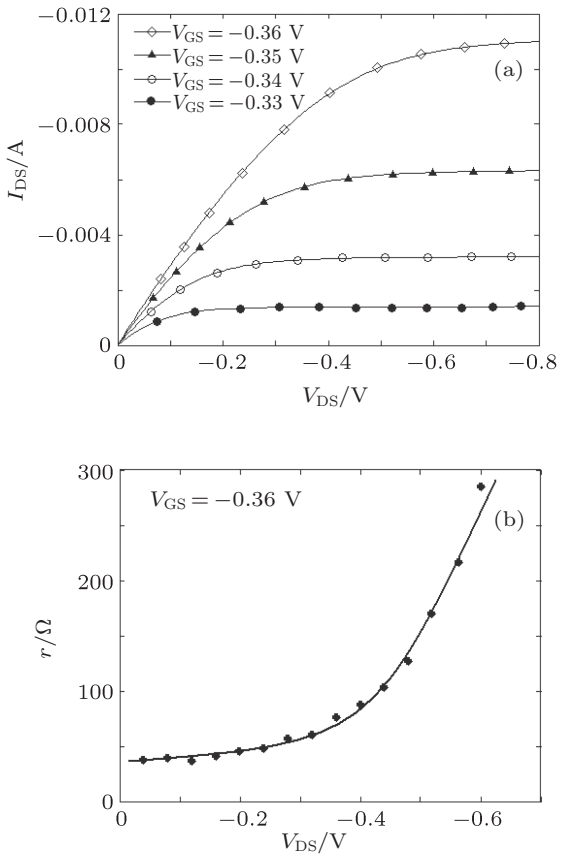


Fig. 5. The output characteristics (a) and AC resistance trend curve (b) of the IFET.

3.2. Constant resistance area

In the constant resistance areas $V_{\rm T} < V_{\rm DS} < (V_{\rm GS}–V_{\rm TH})$, the AC resistance of the OTFFET device does not change with $V_{\rm DS}$. Obviously, the OTFFET device operates in the linear region. In this region, the AC resistance (r) of the OTFFET device is the sum of contact resistance ($R_{\rm c}$) and channel resistance ($R_{\rm ch}$), and expressed as

$$r = R_{\rm c} + R_{\rm ch}.$$

As can be seen, the source/drain voltage variations have no effect on the AC resistance of the OTFFET device. However, the gate voltage variation will lead to the change of the density of carriers in the conductive channel, so the channel resistance will change with the variation of gate voltage ($V_{\rm GS}$). In the linear regime $V_{\rm DS} < (V_{\rm GS}–V_{\rm T})$, the following expression is used to describe $I_{\rm DS}$:[16,17]

$$I_{\rm DS} = \frac{W\mu_{\rm EF}C_{\rm i}}{L}(V_{\rm GS} - V_{\rm TH})V_{\rm DS},$$

where W is the transistor channel width, L is the transistor channel length, $\mu_{\rm EF}$ is the field effect mobility, $V_{\rm TH}$ is the threshold voltage and $C_{\rm i}$ is the insulator capacitance per unit area. If W, L and $C_{\rm i}$ are known, in the linear region, the field-effect mobility is expressed by the following formula:

$$\begin{aligned}\mu_{\rm EF} &= \frac{L}{WC_{\rm i}(V_{\rm GS} - V_{\rm TH})}\frac{\partial I_{\rm DS}}{\partial V_{\rm DS}} \\ &= \frac{L}{WC_{\rm i}(V_{\rm GS} - V_{\rm TH})}\frac{1}{r}.\end{aligned}$$

From the above formulation, the field-effect mobility is in inverse proportion to the AC resistance. Since the field-effect mobility and the conductivity are proportional and the conductivity is in inverse proportion to the resistance, this conclusion is correct. That is to say, in order to increase the field-effect mobility, we must reduce the AC resistance of the OTFFET device, namely reduce the contact resistance and channel resistance. The method of reducing the contact resistance can begin with optimizing the contact interface between the source/drain electrode and semiconductor, and the method of reducing channel resistance can start with increasing the carrier density in the channel of the OTFFET device.

3.3. Increased resistance area

Increased resistance area is correlated to the AC resistances of the source/drain voltage $V_{\rm DS} > (V_{\rm GS}–V_{\rm TH})$. In this period, the OTFFET device is in a saturation operating status. As the source/drain voltage further increases, the channel pinch-off phenomenon occurs, so the AC resistance becomes larger with increasing source/drain voltage.

4. Conclusion

It is indicated in this study that the operating characteristics of an OTFFET device can be qualitatively analysed with the AC resistance trend curves. And according to whether the AC resistance trend curves of the device at $V_{\rm DS} < V_{\rm T}$ exist in high resistance areas, we can determine the interface condition between the source/drain electrodes and the organic semiconductor layer. If a high resistance area appears, the interface contact is a non-Ohmic contact, otherwise it is Ohmic. According to the analysis in theory, the mobility of the OTFFET device is in inverse proportion to the AC resistance. In order to increase the field-effect mobility of the OTFFET device, we must reduce the AC resistance of the OTFFET device, that is reduce the contact resistance and channel resistance. Reducing the contact resistance can be achieved by optimizing the contact interface, and reducing the channel resistance can be implemented by increasing the carrier concentration in the conduction channel of the OTFFET device.

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