The electrical characteristics of a 4H–silicon carbide metal–insulator–semiconductor structure with Al_2O_3 as the gate dielectric*

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A 4H–silicon carbide metal–insulator–semiconductor structure with ultra-thin Al_2O_3 as the gate dielectric, deposited by atomic layer deposition on the epitaxial layer of a 4H–SiC (0001) 8^0N–/N+ substrate, has been fabricated. The experimental results indicate that the prepared ultra-thin Al_2O_3 gate dielectric exhibits good physical and electrical characteristics, including a high breakdown electrical field of 25 MV/cm, excellent interface properties (1×10^{14} cm^{-2}) and low gate-leakage current ($I_G = 1 \times 10^{-3}$ A/cm^{-2}@$E_{ox} = 8$ MV/cm). Analysis of the current conduction mechanism on the deposited Al_2O_3 gate dielectric was also systematically performed. The confirmed conduction mechanisms consisted of Fowler–Nordheim (FN) tunneling, the Frenkel–Poole mechanism, direct tunneling and Schottky emission, and the dominant current conduction mechanism depends on the applied electrical field. When the gate leakage current mechanism is dominated by FN tunneling, the barrier height of SiC/Al_2O_3 is 1.4 eV, which can meet the requirements of silicon carbide metal–insulator–semiconductor transistor devices.

Keywords: Al_2O_3, 4H–silicon carbide, metal–insulator–semiconductor capacitor, gate leakage current, C–V characteristics

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1. Introduction

SiC is a very promising candidate for extreme environments of high temperature, high frequency, high power and radiation hardness due to its excellent physical, chemical and electrical properties. As we know, the performance of SiC power devices is closely related to the bulk and interface characteristics of gate dielectrics. Higher interface state density leads to a reduction in channel mobility, thus lowering the switch speed and increasing gate leakage current, threshold voltage and low-frequency $1/f$ noise. Although more efforts are devoted to producing a high-quality insulator, the interface states density of SiO_2/SiC is at least an order of magnitude higher than that of its counterpart SiO_2/Si.[1,2] In addition, compared with the SiO_2/Si interface, a lower barrier height at the SiO_2/SiC interface will produce a larger leakage current in thermal oxide under high temperature operation, and thus accelerate the failure of oxide.[3] All these seriously limit the high-temperature application of SiC CMOS devices and circuits. To overcome this limit, high dielectric constant (high-k) gate dielectrics have been introduced as a replacement for conventional gate dielectrics. Several intrinsic properties of Al_2O_3, such as large E_g (9 eV), high dielectric constant ($\kappa \sim 10$), high breakdown field (5 MV/cm–10 MV/cm) and a good thermal stability (remaining amorphous even at 1000 °C), make it a viable candidate as a gate dielectric material in SiC-based devices,[4] compared with other high-k gate dielectrics: oxidized-Ta_2Si,[5] SiO_2/TiO_2,[6] Gd_2O_3,[7] SiO_2/HfO_2,[8] AlN,[9] Si_3N_4,[10] and SiO_2/Si_3N_4/SiO_2.[6] The current–voltage (I–V/J–E) characteristics of amorphous Al_2O_3 are already close to those of the ideal SiO_2 thermally oxidized on the SiC substrate. Thus, the insertion of Al_2O_3 can increase the effective thickness of the dielectrics, improve the breakdown characteristics, and also reduce the possibility of the injection of the electrons from gate electrodes to the accumulation region of the device.

In this experiment, an SiC metal–insulator–semiconductor (MIS) structure with ultra-thin Al_2O_3 ($\sim$ 4 nm) as a gate dielectric deposited by the atomic layer deposition (ALD) method on an epitaxial layer of 4H–SiC (0001) 8^0N–/N+ substrate is fabricated.

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High-frequency C–V and I–V measurements at room temperature have shown that the interface equivalent charge density of Al_2O_3/SiC is 1×10^{14} cm^{-2}, and the breakdown electrical field of the Al_2O_3 film is 25 MV/cm. Further research has indicated that the gate leakage current is co-influenced by several mechanisms: Schottky emission, the Frenkel–Poole (FP) mechanism, direct tunneling (DT) and Fowler–Nordheim (FN) tunneling. When it is dominated by FN tunneling, the barrier height of SiC/Al_2O_3 is 1.4 eV, which can meet the requirements of SiC metal–insulator–semiconductor field effect transistor (MISFET) devices for gate dielectric characteristics.

2. Experiment

The N+/N–(0001) 4H–SiC substrate with a 4-μm thick epilayer doped by N (4×10^{15} cm^{-3}), purchased from CREE Inc, was used to fabricate the MIS capacitors. After undergoing a standard RCA wafer cleaning process, an approximately 4 nm thick Al_2O_3 gate oxide was deposited using the ALD method. Then, gate electrodes (Ti(23 Å)/Au(45 Å) (1 Å=0.1 nm)) were sputtered and patterned by a lift-off process. Finally, the bottom electrode Al was sputtered to form a back Ohmic contact. Two sets of samples: circle (inner diameter: 175 μm, outer diameter: 330 μm) and square (77 μm×77 μm) MIS capacitors were fabricated in this experiment. Room-temperature I–V and C–V were measured by HP4156B and Keithley 590 C–V analyzers, respectively.

3. Results and discussion

3.1. Microstructure analysis of the Al_2O_3 film and Al_2O_3/SiC interface

Test results and fitted curves of the phase-structure and binding-state of the Al_2O_3 film are shown in Fig. 1, and were obtained by means of X-ray photoelectron spectroscopy (XPS). The XPS spectra were obtained by Axis Ultra, Kratos using monochromatic Al Kα radiation (150 W, 15 kV, 1486.6 eV). The vacuum in the spectrometer was 1.33×10^{-7} Pa. Binding energies were calibrated relative to the C 1s peak (284.8 eV) from hydrocarbons adsorbed on the surface of the samples. The final spectrum in Fig. 1(a) shows that from the surface to the bottom of the deposited film, five kinds of elements exist: Al 2p, N 1s, O 1s, Si 2p, and Si 2s, and the concentrations are 24.45, 6.16, 59.76, 4.78, and 4.85%, respectively. The Al 2p XPS spectrum is presented in Fig. 1(b), and this figure indicates that the Al element exists in the form of Al_2O_3 because the binding energy of Al 2p is 74.6 eV, which is consistent with the standard X-ray photoelectron peak

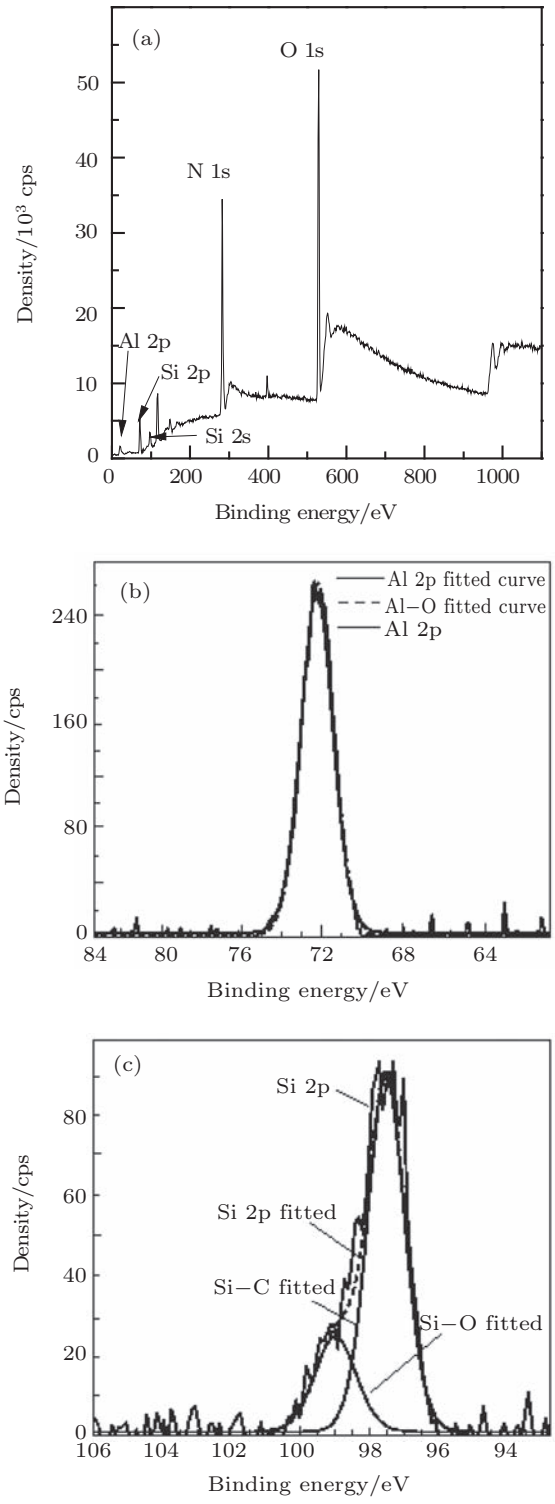


Fig. 1. The XPS spectra of the deposited Al_2O_3 film by ALD in the 4H–SiC epitaxial layer for (a) the final XPS spectrum, (b) the Al 2p XPS spectrum and (c) the Si 2p XPS spectrum.

value of the Al_2O_3 film. We can also see from a comparison of the results of the test and fitted curves from

the Si 2p spectra in Fig. 1(c), that the Si 2p element exists in a two-phase structure: SiC and SiO_2. And a small amount of SiO_2 is purely due to the SiC substrate heated during the deposition of the Al_2O_3 film.

A high-resolution transmission electron microscopy (HRTEM) image of the gate/Al_2O_3/SiC interface is shown in Fig. 2(a). For the ALD method itself, the value of the deposited Al_2O_3 film thickness varies from 3 to 2.6 nm, but the film thickness is controlled in the nm order of magnitude throughout the entire sample. It can also be found from the HRTEM image of the Al_2O_3/SiC interface in Fig. 2(b) that the separation line of Al_2O_3/SiC is distinct, and that the transition layer thickness is only about 1 nm, which is very close to that of Al_2O_3/Si[11] with the same processing. This interface can therefore be considered as an abrupt interface.

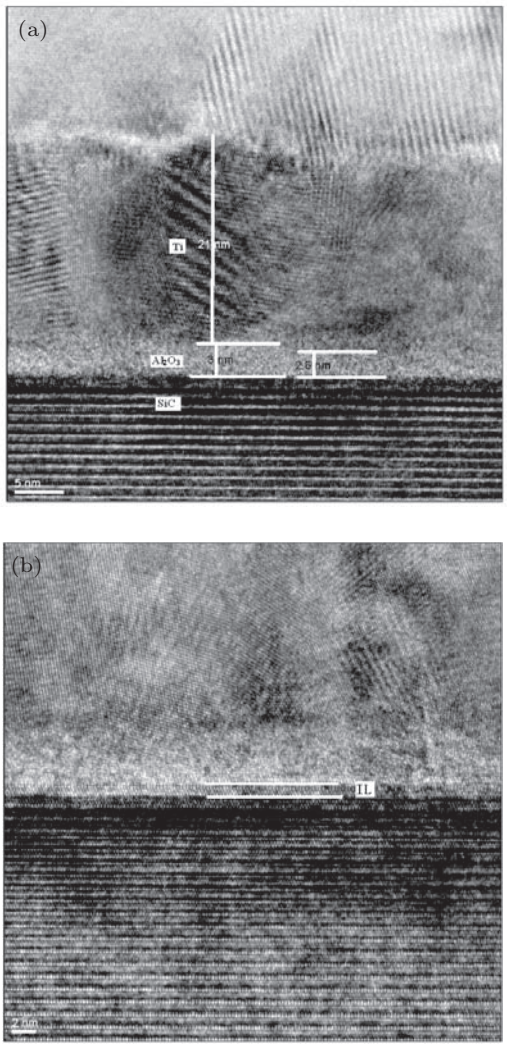


Fig. 2. HRTEM image of the gate/Al_2O_3/SiC for (a) HRTEM images of various layers and (b) a HRTEM image of the Al_2O_3/SiC interface.

3.2. The high-frequency *C–V* characteristics of SiC MIS capacitors

Figure 3 gives the high-frequency *C–V* test results of the circular capacitor, and also the ideal *C–V* curves calculated using Matlab according to the equations given in Ref. [12] for comparison. The flat-band voltage $V_{\rm fb}$ of 8 V is calculated from this figure.

The relationship between flat-band voltage and interface charge can be described as

$$V_{\rm fb} = V_{\rm fb}^{*} - \frac{Q_{\rm eff}}{C_{\rm ox}}. \tag{1}$$

In Eq. (1), the ideal flat-band voltage $V_{\rm fb}^{*}$ can be expressed as

$$V_{\rm fb}^{*} = -\frac{W_{\rm m} - W_{\rm s}}{q}. \tag{2}$$

Here $W_{\rm s}$ is the work function of SiC, expressed by the following equation

$$W_{\rm s} = \chi + E_{\rm g}/2 - (kT/q)\ln\left(N_{\rm d}/n_{\rm i}\right). \tag{3}$$

In Eqs. (1)–(3), χ is the electron affinity of SiC (4 eV), $N_{\rm d}$ the doping concentration in the epitaxial layer (4×10^{15} cm^{-3}), $n_{\rm i}$ the intrinsic carrier concentration (3.0×10^{-7} cm^{-3}), and the forbidden bandgap of 4H–SiC, $E_{\rm g}$ is 3.0 eV. The work function of the gate metal Ti, $W_{\rm m}$, is 3.8 eV.

By combining Eqs. (1), (2) and (3), $V_{\rm fb}^{*}$ is calculated to be −0.38 V, and the amounts of fixed charge and trapped charge at the interface of Al_2O_3/SiC are all 1×10^{14} cm^{-2}.

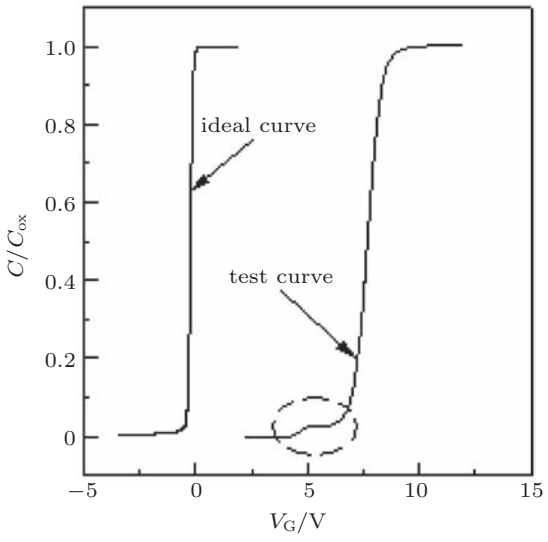


Fig. 3. A comparison of the *C–V* characteristics at 10 kHz.

In particular, note that there is a step or ledge marked by a dashed ellipse on the test curve at $V_{\rm G}$ smaller than $V_{\rm fb}$ in Fig. 3. This behaviour is similar

to quasi-static C–V. The frequency is not high enough to eliminate the contribution of interface states to the total capacitance in the depletion regime.[13,14] The increase in frequency will weaken this ledge, and this ledge occurs whatever the shape of the tested graph.

Additionally, in comparison with the ideal curve, the measured curve increases slowly when the surface state changes from surface depletion to flat-band. This phenomenon is mainly caused by the presence of an interface trap. In order to achieve the same surface-band bending as the ideal curve, more charges or a larger voltage is needed to fill in the interface trap, or more accurately the test curve is flattened as the device surface is in the depletion state.

Figure 4 gives the best hysteretic property of the square capacitors measured at 10 kHz; the gate voltage is swept from −15 V to +15 V back to −15 V. The hysteretic property is slightly different in the different regions of the sample due to the uneven distribution of interface states in such a small fraction of the sample. Because a very small amount of bulk trap charge exists in the gate dielectric film, small charges will be captured by traps when the gate voltage is swept. The hysteretic voltage is only about 40 mV, as shown in this figure, which demonstrates that the Al_2O_3 film obtained in this experiment is of good quality.

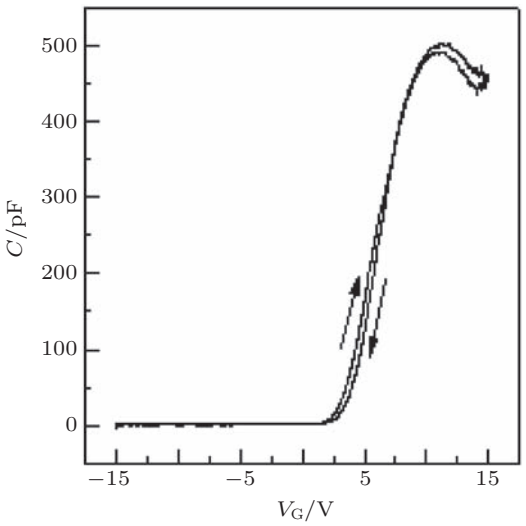


Fig. 4. The hysteretic characteristics of the C–V curve at 10 kHz.

3.3. The current conduction mechanism of Al_2O_3

In order to analyze the current conduction mechanism in the Al_2O_3 film, many conduction mechanisms have been evaluated:[15] FN tunneling, DT, Schottky emission (SE), FP emission, and so on. Additionally, the space–charge limited current and Ohmic's law will be the main factors for some specific conditions. DT is closely related to oxide thickness. For an oxide thickness lower than 2 nm, the DT phenomenon is more obvious. Because the dielectric constant of Al_2O_3 is larger than SiO_2, DT must be taken into consideration when the physical thickness of Al_2O_3 is less than about 5 nm.[16,17] The representative I–V curves for square and circular capacitors were chosen to analyze and fit with FP/SE, as shown in Figs. 6 and 7, respectively.

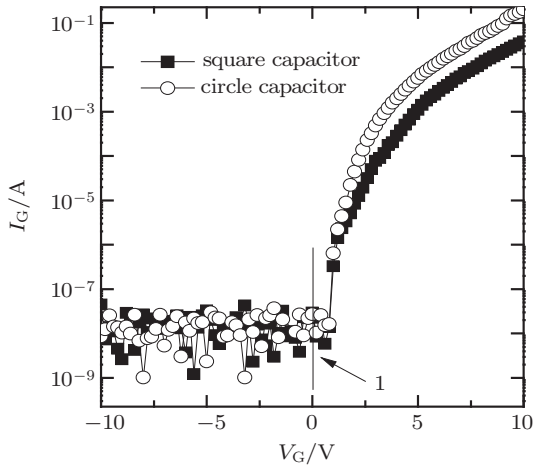


Fig. 5. A typical logarithmic plot of the I_G–V_G characteristics.

Figure 5 presents a typical logarithmic plot of I_G–V_G measured for circular and square capacitors. We can see from these two curves that in the initial stage of positively biased V_G ($0 < V_G < 1$ V), which is labeled 1, I_G does not vary as V_G changes, while I_G increases regularly with V_G increasing beyond a certain value. We believe that direct tunneling of electrons through the gate dielectric contributes to the current in this range. And this region will disappear with decreasing thickness of gate dielectric.[17] With increasing V_G, the gate leakage current comes from a combined effect of FN tunneling and SE.

Schottky emission is a field-assisted thermionic emission of an electron passing over a surface barrier. For a current running through an oxide following the SE mechanism, a plot of $\ln J$ versus $E^{1/2}$ must be in a linear form. The dynamic dielectric constant ε_r value can be extracted from the slope of the plot. Only a self-consistent dynamic dielectric constant can ensure that the current conduction is due to the Schottky effect or an FP emission. This means that the dynamic dielectric constant, calculated from the slope of the line in the Schottky plot, should lie between the optical dielectric constant ($\varepsilon_r \approx 2.9$) and the static dielectric constant ($\varepsilon_r \approx 10$).[18,19] From the slope of the line in Fig. 6(b) in the regime of 2.25 MV/cm $< E_{ox} <$ 6.25 MV/cm, $\varepsilon_r = 5/\varepsilon_r = 7$ is

inferred, and this ensures that SE is the dominant conduction mechanism in the investigated electric field. When the electric field is greater than 6.25 MV/cm, FN tunneling takes place and a detailed illustration is given in Fig. 8.

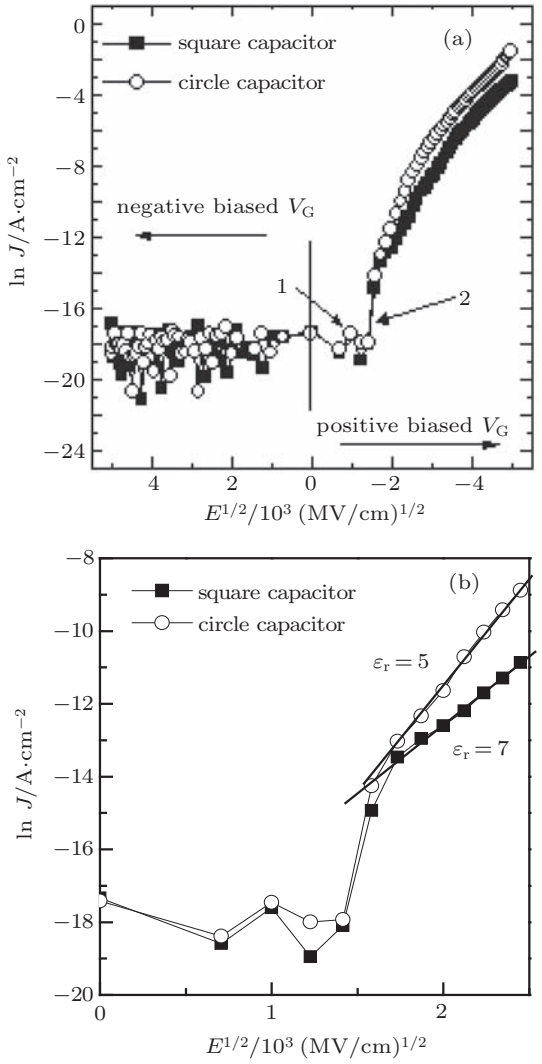


Fig. 6. Leakage current fitted with Schottky emission for (a) all regimes of V_G, and (b) a positively biased regime of V_G.

FP emission is a field-assisted thermal detrapping of a carrier from the bulk oxide into the conduction band. Therefore, it is a bulk-limited conduction process and occurs at high temperatures and high fields. From the linear portion of the FP plot ($\ln(J/E)$ versus $E^{1/2}$) in Fig. 7(b), the ε_r value does not lie between the optical dielectric constant and the static dielectric constant. Thus, FP is not a dominated current conduction mechanism within the investigated electrical field. Therefore, the gate leakage current is mainly influenced by SE in the investigated electrical field, but a small hopping at the starting point, as marked 2 in Figs. 6(a) and 7(a), is due to test error.

In the negatively biased V_G regime, the I–V relationship is generally consistent with SE (Fig. 6(a) or Fig. 7(a)). Therefore, gate leakage current is attributed to the combination of SE and FP mechanisms. This indicates that in the condition of electron injection from the gate electrode to the dielectric, the barrier height at the interface between the gate electrode and the gate dielectric, the gate electrical field strength, and the density and distribution of the interface states in the forbidden band at the interface of gate and Al_2O_3, will all influence the gate leakage current.

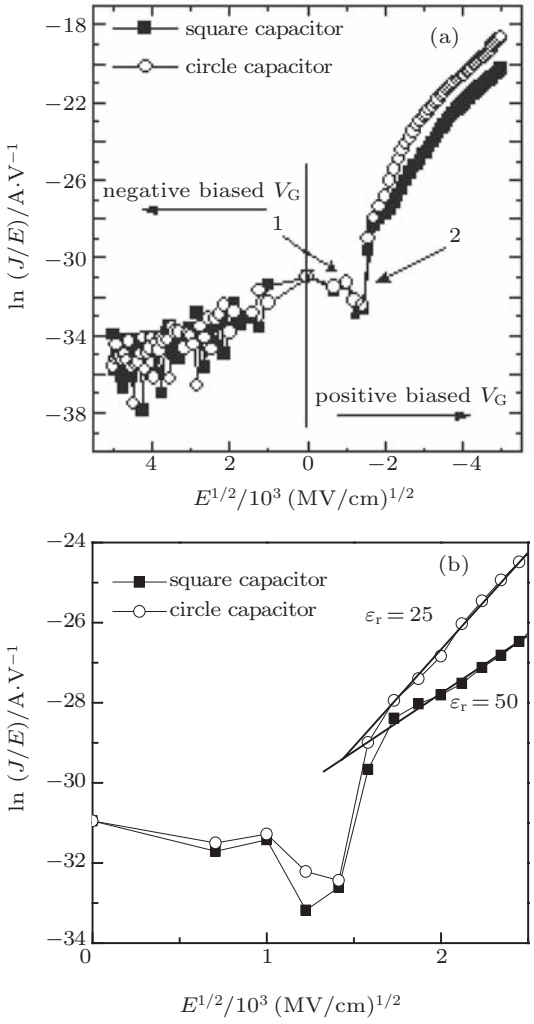


Fig. 7. Leakage current fitted with the FP mechanism for (a) all regimes of V_G, and (b) a positively biased regime of V_G.

The J–E response of the square capacitor in Fig. 7 is plotted again in Fig. 8. The leakage current density is 1×10^{-3} A/cm^2 at a lower electrical field of 8 MV/cm than that in other high-κ material such as

AlN, HfO_2, SiO_2/HfO_2, and Gd_2O_3,[5−9] which can be compared with the data given in Ref. [10]. For an $E_{ox} < 2.25$ MV, where $V_G < 1.0$ V, the gate dielectric barrier that electrons tunnel through is trapezoidal and the direct tunneling begins to take effect.[8] For an electrical field $E_{ox} > 25$ MV, the MIS capacitor will break down.

Figure 8(b) is a transformation of Fig. 8(a), and from this figure we can obtain a linear relationship between $\ln(J/E^2)$ and $1/E$. This further shows that the gate leakage current is dominated by FN tunneling at about 6.25 MV/cm $< E_{ox} <$ 25 MV/cm. The

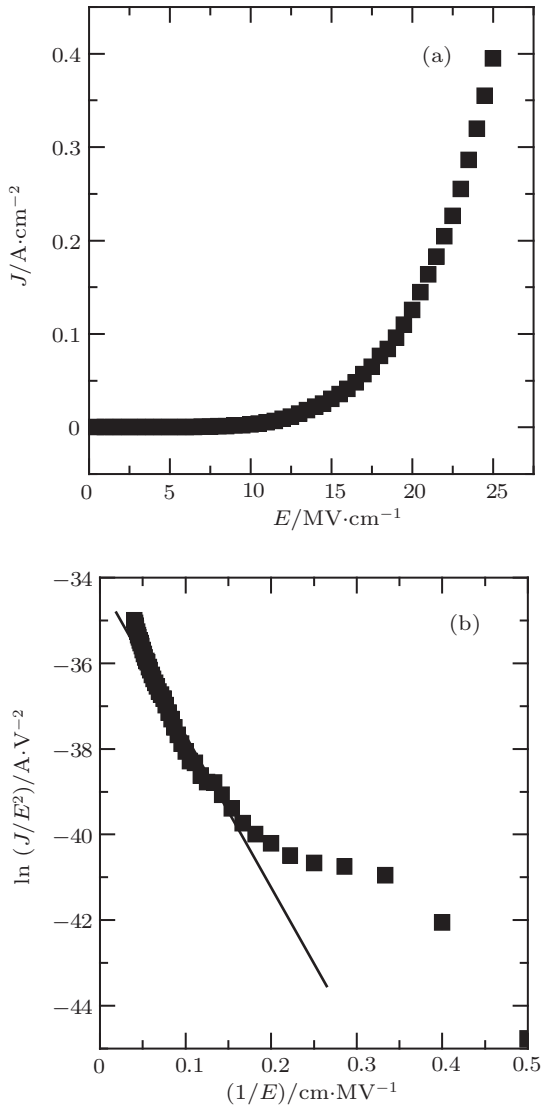


Fig. 8. $J \sim E$ and $\ln(J/E^2) \sim 1/E$ plots for the square capacitor for (a) $J \sim E$ characteristics, and (b) $\ln(J/E^2) \sim 1/E$ characteristics.

FN tunneling can be expressed by[12]

$$J = AE^2 \exp(-B/E), \tag{4}$$

where J is the current density in A/cm^2, E is the effective oxide field in V/cm, $E = V_{ox}/t_{ox}$, and t_{ox} is the physical thickness of the gate dielectric film. The pre-exponent A and the slope B are given by

$$\begin{aligned} A &= \left(\frac{q^3}{8\pi h}\right)\left(\frac{m_{sic}}{m_{ox}}\right)\left(\frac{1}{\phi_b}\right) \\ &= 1.54 \times 10^{-6}\left(\frac{m}{m_{ox}}\right)\left(\frac{1}{\phi_b}\right)\ (\mathrm{A/V^2}), \end{aligned} \tag{5}$$

$$\begin{aligned} B &= 8\pi\,(2m_{ox})^{1/2}\,\phi_b^{3/2}/3hq \\ &= 6.83 \times 10^7\left(\frac{m_{ox}}{m}\right)^{1/2}\phi_b^{3/2}\ (\mathrm{V/cm}), \end{aligned} \tag{6}$$

where e is the electronic charge, m_{ox} is the electron mass in the oxide, $m_{ox} = 0.11$ m,[8] m is the free electron mass and ϕ_b is the barrier height of Al_2O_3/SiC. Combining Eqs. (4) and (6), we can obtain the barrier height of Al_2O_3/SiC ϕ_b, which is about 1.4 eV. And similar results can be obtained from the circular capacitors.

4. Summary

An SiC MIS structure has been fabricated with ultra-thin Al_2O_3 as the gate dielectric, deposited by the ALD method in the epitaxial layer of a 4H–SiC (0001) 8^0N–/N+ substrate. Microstructure and electrical characteristics analysis of the film and Al_2O_3/SiC interface show that the Al_2O_3 deposited has a good bulk characteristic and a good quality at the Al_2O_3/SiC interface. The breakdown electrical field of the Al_2O_3 film is 25 MV/cm, and the MIS capacitor has a fairly low gate leakage current ($I_G = 1 \times 10^{-3}$ A/cm^{-2}@$E_{ox} = 8$ MV/cm) under acceptable interface effective charge (1×10^{14} cm^{-2}). Further research has also shown that the barrier height of SiC/Al_2O_3 is 1.4 eV when the gate leakage current is dominated by FN tunneling. In addition, the gate leakage current is also influenced by the SE, FP and DT mechanisms. All of these show that the obtained Al_2O_3 film and the corresponding SiC MIS capacitor can meet the requirements of SiC MISFET devices.

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