Total ionizing dose effect in an input/output device for flash memory

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Input/output devices for flash memory are exposed to gamma ray irradiation. Total ionizing dose has been shown great influence on characteristic degradation of transistors with different sizes. In this paper, we observed a larger increase of off-state leakage in the short channel device than in long one. However, a larger threshold voltage shift is observed for the narrow width device than for the wide one, which is well known as the radiation induced narrow channel effect. The radiation induced charge in the shallow trench isolation oxide influences the electric field of the narrow channel device. Also, the drain bias dependence of the off-state leakage after irradiation is observed, which is called the radiation enhanced drain induced barrier lowing effect. Finally, we found that substrate bias voltage can suppress the off-state leakage, while leading to more obvious hump effect.

Keywords: input/output device, oxide trapped charge, radiation induced narrow channel effect, shallow trench isolation, total ionizing dose

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1. Introduction

Today more modern technologies having inherently more radiation hardness due to the thinning of the gate oxide, are available to circuit design. The thinner gate oxide has eliminated the significance of threshold voltage shifts since radiation induced charge builds up in the gate oxide.[1,2] Radiation tolerance in thin gate oxides is further enhanced by the increased likelihood of positive charge annihilation or compensation by tunneling electrons from the adjacent materials.[3] Although the gate oxide becomes thinner, the shallow trench isolation (STI) oxide does not scale down correspondingly. Typical STI dimensions for complementary metal oxide semiconductor (CMOS) technologies smaller than 0.18 μm ranged from 300 nm to 450 nm in depth and widths are the order of 280-nm wide.[4] Radiation induced charge trapped in the isolation oxide, particularly at the Si/SiO_2 interface along the trench oxide, creates a leakage path which becomes the dominant contributor to off-state leakage in n-channel metal-oxide-semiconductor field-effect-transistor (NMOSFET).[5,6]

As we know, flash memories are the most important series of non-volatile memory technologies nowadays, featuring high speed and good retention properties. In some applications, exposure to high fluxes of electrons can significantly reduce the system life due to the total ionizing dose (TID). Memory control circuit has been demonstrated to be the most sensitive part of commercial devices during TID experiments.[7,8] The data obtained in Ref. [9] indicates enhanced TID susceptibility in input/output (I/O) devices and circuits due to lowly substrate doping along STI sidewall. The I/O devices are a radiation hardness threat which can impact the performance of I/O driver circuits. Radiation induced narrow channel effect (RINCE) of I/O device was investigated by Faccio *et al.*[10] The I/O transistors used in high energy physics from different foundries were discussed by Gonella *et al.*[11] However, the drain bias dependence and substrate influence were not discussed.

Some works are aimed at the TID responses of submicron technology, including enclosed gate devices,[12] simulation of 0.18 μm[13] devices and bias dependence of I/O devices.[14] In our contribution,

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TID effects of I/O device for a 0.18 μm technology were discussed in detail. Increase of off-state leakage has shown the dependence of gate length, which can be explained by the parasitic transistor model. The RINCE is also observed for our samples. The drain bias dependence and substrate influence on the radiation response were analysed in the following sections.

2. Experimental details

All devices were fabricated in a 0.18-μm flash memory technology. The STI is introduced for isolation and the trench oxide thickness is about 390 nm. The I/O transistors with gate oxide of 6 nm were used for input and output circuit of flash memory. Different transistor sizes were chosen: width/length (W/L) =10 μm/10 μm, 10 μm/0.7 μm, 10 μm/0.35 μm, 0.22 μm/0.35 μm, and 0.22 μm/10 μm. All the samples were ceramic packaged. The operating voltage is 3.3 V.

Irradiation experiments were carried out at the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences by using ^{60}Co γ source, typically at a dose rate of 200 rad (Si)/s. During radiation exposure, the gate of the devices was biased at 3.3 V with all other terminals grounded (ON bias). The temperature was monitored and kept at room temperature. Electrical measurements were obtained prior to irradiation and after step stress irradiations up to 50, 80, 150, 300, and 500 krad (Si). Transfer (I_{ds}–V_{gs}) characteristics were measured under different drain bias for all devices and under different substrate voltage bias conditions for transistors with W/L=10 μm/0.7 μm. These I–V curves were taken within half an hour following exposure.

3. Results and discussion

3.1. I_{ds}–V_{gs} versus TID

Figure 1 shows a series of transfer I–V curves measured on W/L=10 μm/0.7 μm n-channel transistor irradiated in steps up to 500 krad (Si) under ON bias condition. As shown in Fig. 1, after total dose radiation level of 80 krad (Si), subthreshold leakage current slightly increases and subthreshold "hump" effects are observed. At 150 krad (Si), the leakage current curve is nearly flat. When the total ionizing dose accumulated to 500 krad (Si), the drain current at V_{gs} = 0 V is approximately 6 orders of magnitude higher than the corresponding pre-irradiation value. Positive charge trapped in the lateral STI oxide formed a conductive channel through which leakage current can flow between source and drain, and the parasitic lateral transistors turn on.[5] The hump disappears gradually as the increase of leakage current of parasitic transistor. Degradation of the I/O device after ionizing irradiation will lead to large leakage current and incorrect I/O voltage. Thus, the circuit designer has to carefully evaluate the impact of these effects on the I/O circuit, especially where timing shifts could induce communication failure.

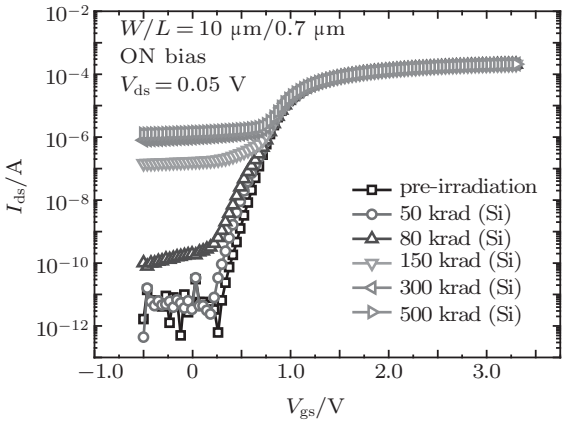


Fig. 1. The TID response for transistor with W/L = 10 μm/0.7 μm.

Figure 2(a) is a plot of the off-state leakage (I_{ds}@V_{gs} = 0 V) as a function of total dose for transistors with different sizes. The results clearly show that transistor channel length affects the radiation induced off-state leakage. During irradiation, a larger increase in off-state leakage is observed for the transistors with length of 0.35 μm and 0.7 μm, which shows a value of 10^{-6} A at 500 krad (Si). For the 10-μm channel length transistors, the leakage current remains relatively low, which increases to 10^{-7} A at 500 krad (Si). In a word, the larger increase of off-state leakage was observed for the shorter channel lengths. Figure 3 gives a view of NMOS after TID radiation with two parasitic leakage paths, which can be modeled by two parasitic NMOSFETs in parallel with the main transistor device controlled by the thin gate oxide. The three MOSFETs in Fig. 3 have the same gate length, which is the drawn length of the device. The two parasitic transistors have a gate width $W_{parasitic}$ and an effective gate oxide thickness $T_{ox,parasitic}$, which depend on the portion of the interface at the STI sidewall which gets inverted upon dose level of radiation and charge buildup in the isolation oxide. The off-state leakage is dominated by the parasitic device. It is well known that the larger

the length is, the smaller of current for the transistor is.[15] After irradiation, the parasitic transistor is turned on. The shorter channel length leads to larger increase of leakage.

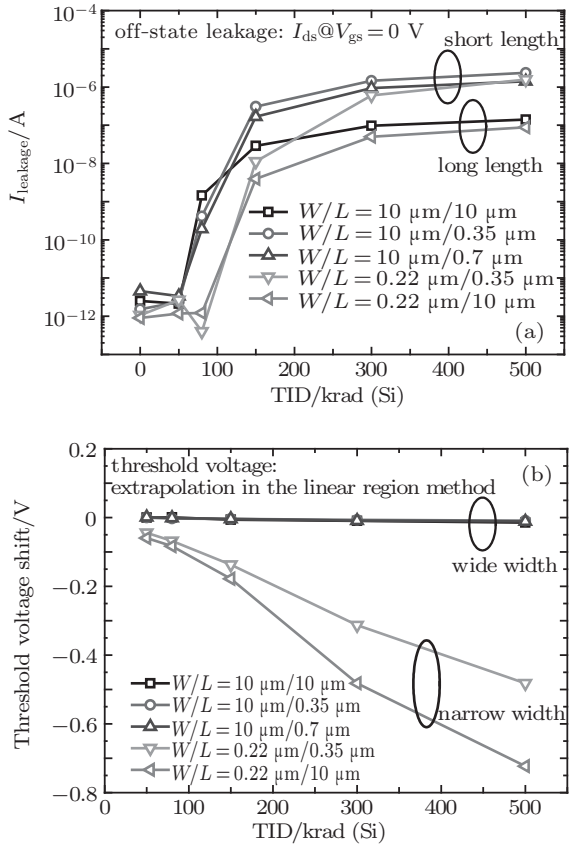


Fig. 2. (a) Increase of off-state leakage and (b) threshold voltage shift after irradiation.

Figure 2(b) shows threshold voltage shift with TID for different size transistors. The threshold voltage shift is more pronounced for narrow transistors, which is −0.5–−0.7 V at 500 krad (Si). Relatively small threshold voltage shift was observed for wide channel transistors, which is only −0.03 V at 500 krad (Si). The narrow transistor shows worse characteristic degradation, which is called radiation induced narrow channel effect. The observed degradation, especially important in narrow transistors, is due to radiation induced edge effects.[10,11] In the presence of positive charges trapped in the STI oxide, the depletion or inversion condition near the STI sidewall is formed. At the STI corners, where the parasitic depletion regions meet the gate control depletion region, the two regions overlap each other. The thickness of parasitic transistor depletion region increases with radiation dose, and extends from both sides of STI oxide to the centre of the body. The depletion charge under the gate is actually induced by the gate together with the two parasitic depletion regions so that the channel charge can be considered to be "shared" by the gate and oxide trapped charge in STI oxide.[16] For the narrow transistor, the charge balance at the edge of STI not only determines the threshold voltage of the parasitic transistor, but also influences the electric field of the main transistor. The RINCE is expected to increase its importance in modern technologies with smaller sizes.

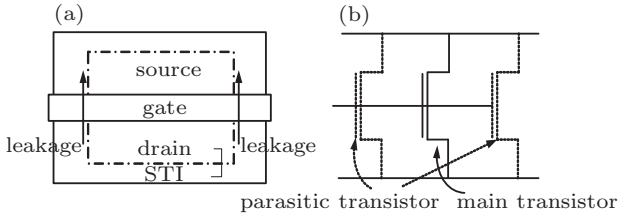


Fig. 3. (a) illustration of drain to source leakage path and (b) main and parasitic sidewall transistors.

3.2. Drain bias dependence

Figure 4 illustrates the post-irradiation I_{ds}–V_{gs} characteristics for transistors with W/L =

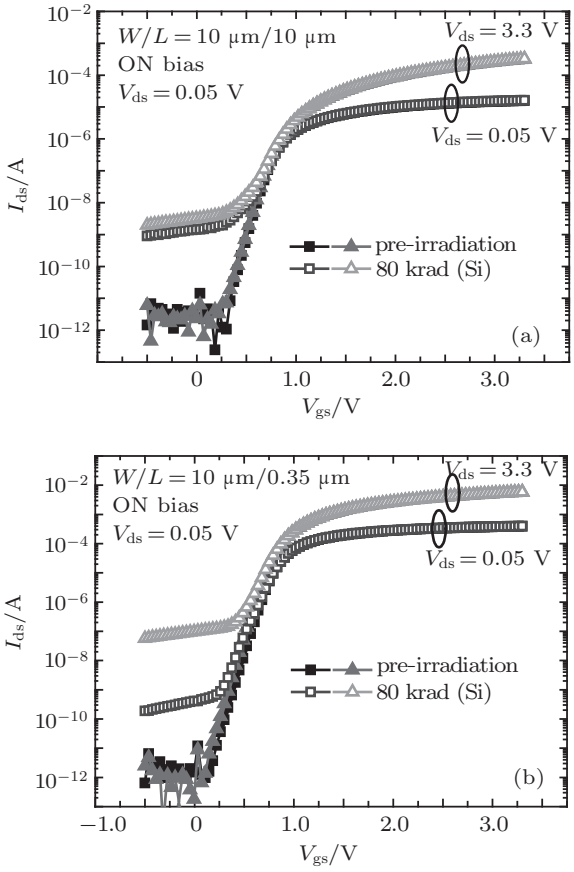


Fig. 4. The I_{ds}–V_{gs} characteristics for transistor with (a) W/L = 10 μm/10 μm and (b) W/L = 10 μm/0.35 μm under different drain biases at 80 krad (Si).

10 μm/10 μm and 10 μm/0.35 μm under different drain biases at 80 krad (Si). The pre-irradiation I_{ds}–V_{gs} curves were shown in the picture for comparison. The pre-irradiation current–voltage curve does not show any off-state leakage current increase with drain bias. For the long channel device, the off-state leakage current is 10^{-9} A at $V_{ds} = 0.05$ V. The leakage current changes relatively up to $V_{ds} = 3.3$ V, after which leakage current increases to 2×10^{-9} A. At a total dose of 80 krad (Si), the off-state leakage current of device with short channel length increases sharply with drain bias voltage. The off-state leakage current at $V_{ds} = 3.3$ V is more than 3 orders of magnitude higher than the corresponding value at $V_{ds} = 0.05$ V. The device's off-state leakage current increases with the drain bias voltage, which indicates drain induced barrier lowing (DIBL) effect caused by charge sharing with the source and drain junctions.[17] The oxide trapped charge at the trench sidewalls enhances the DIBL by depleting the edges of the channel.

As discussed before, the gate length of the parasitic device is the same as that of the main transistor. As shown in Fig. 5, at a dose level of 80 krad (Si), there is in an exponential relationship between the off-state leakage current and the drain voltage for a short channel device (0.35 μm). That is the DIBL effect. However, this dependence has not been shown for the long channel device (10 μm). The current of a long channel transistor has only changed from the linear region to the saturation region. As we know, the shorter the gate length is, the higher the DIBL is; the thicker the oxide is, the higher the DIBL.[18] The DIBL effect of parasitic device is more pronounced than in the main transistor due to the thick "gate oxide". The leakage current is negligible under $V_{ds} = 0.05$ V, while exponentially increases with drain voltage, and the value is 10^{-8} A under $V_{ds} = 3.3$ V for the short channel device. That is to say, the substrate along the STI sidewall is not in strong inversion region, which means that the parasitic device is in the subthreshold region. The exponential relationship between the off-state leakage current and the drain voltage weakened with the increase of radiation dose, which means that the parasitic device is in the strong inversion region.[18] The leakage change induced by DIBL is relatively smaller than the drive current in saturation region. The radiation enhanced DIBL effect leads to large increase of leakage. In practice, the radiation response of a submicron device should be paid more attention about the drain bias dependence, especially for the short channel device.

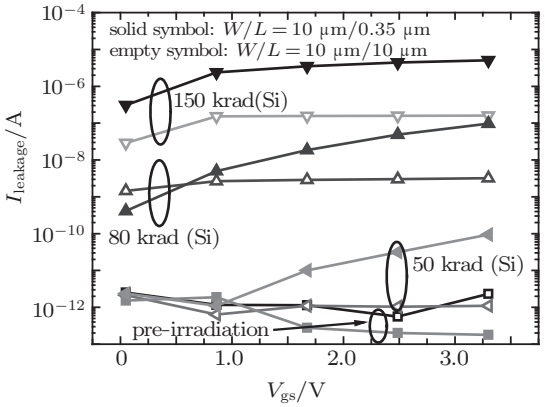


Fig. 5. Comparison of off-state leakage as a function of drain bias for devices under different dose levels and sizes.

3.3. Substrate bias dependence

Typical I_{ds}–V_{gs} characteristics for the different substrate bias voltages before and after irradiation are shown in Fig. 6. Little hump effect was observed before the irradiation, while obvious hump effect was observed after irradiation. After a total dose of 500 krad (Si), the device's subthreshold leakage current decreases with the decrease of negative substrate bias voltage. Using a negative back gate bias to harden against TID is well known in the SOI technology.[19] For bulk devices, larger negative bias voltage will make the devices harder against total ionizing radiation. Because of the large thickness of the shallow trench isolation oxide, the pre-irradiation threshold voltage of the parasitic field oxide transistor is relatively large, but as positive radiation-induced charges build up in the field oxide, it can cause a very large negative threshold-voltage shift. The threshold voltage shift of the transistor was extracted, and it has shown no changes after irradiation under different substrate biases. The curve is not shown here for briefness. Negative substrate bias voltage raises the threshold voltage in the isolation region and therefore tends to cut-off radiation induced parasitic leakage path. The isolation oxide region behaves qualitatively like a second transistor and has its own effective threshold voltage that is more strongly affected by the back bias. Thus, the threshold voltage of the main transistor has shown no change and the hump effect is pronounced. Figure 7 shows leakage current before and after irradiation with different substrate voltages. Leakage current was suppressed by negative substrate voltage (5 orders magnitude). Though the off-state leakage can be suppressed by the negative substrate bias, the

obvious hump effect is still an obstacle. Even worse, higher bias voltage will also tend to shift the device's threshold voltage.[20] To compensate for this, the device will typically be engineered so that the threshold voltage is within a preferred operational range when negative substrate bias voltage is applied.

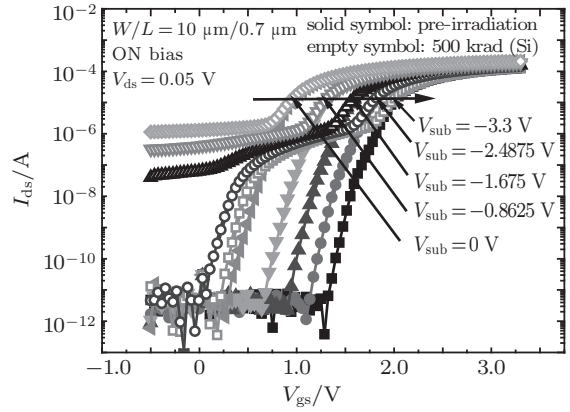


Fig. 6. I_{ds}–V_{gs} characteristics for transistor with $W/L =$ 10 μm/0.7 μm at different substrate voltages under 500 krad (Si).

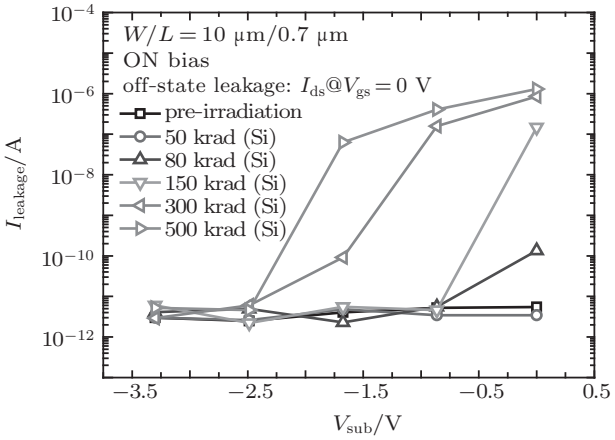


Fig. 7. Leakage current change with TID for different substrate bias voltages.

4. Conclusion

In summary, the radiation effects of I/O devices were discussed in detail. Off-state leakage has shown dependence on the gate length, which can be explained by the parasitic transistor model. The RINCE is observed for the narrow width device, which is induced by the influence of STI oxide trapped charge. When selecting the I/O circuit applied in the radiation environment, the transistor size should be taken into consideration. Off-state leakage has shown great dependence on the drain bias, especially for short channel devices, which is called the radiation enhanced DIBL effect. The higher drain bias leads to worse characteristic degradation. Also, negative substrate bias can suppress the off-state leakage, but leads to an obvious hump effect. The sensitivity of the I/O device under TID irradiation implies that the I/O circuit could be vulnerable to TID radiation.

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References

[1] Saks N S, Ancona M G and Modolo J A 1984 *IEEE Trans. Nucl. Sci.* **NS-31** 1249
[2] Saks N S, Ancona M G and Modolo J A 1986 *IEEE Trans. Nucl. Sci.* **NS-33** 1185
[3] Barnaby H J 2006 *IEEE Trans. Nucl. Sci.* **53** 3103
[4] Esqueda I S, Barnaby H J and Alles M L 2005 *IEEE Trans. Nucl. Sci.* **52** 2259
[5] Barnaby H J, Mclain M and Esqueda I S 2007 *Nucl. Instrum. Methods Phys. Res. Sect.* B **261** 1142
[6] Faccio F, Barnaby H J, Chen X J, Fleetwood D M, Gonella L, Mclain M and Schrimpf R D 2008 *Microelectron. Reliab.* **48** 1000
[7] Nguyen D N, Lee C I and Johnston A H 1998 *IEEE Radiation Effects Data Workshop Record* Newport Beach, CA, USA p. 100
[8] Nguyen D N, Guertin S M, Swift G M and Johnston A H 1999 *IEEE Trans. Nucl. Sci.* **46** 1744
[9] Mclain M, Barnaby H J, Holbert K E, Schrimpf R D, Shah H, Amort A, Baze M and Wert J 2007 *IEEE Trans. Nucl. Sci.* **54** 2210
[10] Faccio F and Cervelli G 2005 *IEEE Trans. Nucl. Sci.* **52** 2413
[11] Gonella L, Faccio F, Silvestri M, Gerardin S, Pantano D, Re V, Manghisoni M, Ratti L and Ranieri A 2007 *Nucl. Instrum. Methods Phys. Res. Sect.* A **582** 750
[12] Li D M, Wang Z H, Huangfu L Y and Gou Q J 2007 *Chin. Phys.* **16** 3760
[13] Wang S H, Lu Q, Wang W H, An X and Huang R 2010 *Acta Phys. Sin.* **59** 1970 (in Chinese)
[14] Liu Z L, Hu Z Y, Zhang Z X, Shao H, Chen M, Bi D W, Ning B X and Zou S C 2011 *Chin. Phys.* B **20** 070701
[15] Arora N 2007 *Mosfet Modeling for VLSI Simulation: Theory and Practice* (Singapore: World Scientific) pp. 84–86
[16] Liu Z L, Hu Z Y, Zhang Z X, Shao H, Chen M, Bi D W, Ning B X and Zou S C 2010 *Nucl. Instrum. Methods Phys. Res. Sect.* B **268** 3498
[17] Youk G U, Khare P S, Schrimpf R D, Massengill L W and Galloway K F 1999 *IEEE Trans. Nucl. Sci.* **46** 1830
[18] Deen M J and Yan Z X 1990 *IEEE Trans. Electron. Dev.* **37** 1707
[19] Davis G E and Hughes H L 1982 *IEEE Trans. Nucl. Sci.* **29** 1685
[20] Neamen D A 2003 *Semiconductor Physics and Devices: Basic Principles* 3rd edn. (New York: McGraw-Hill) pp. 499, 500