Impact of substrate bias on radiation-induced edge effects in MOSFETs

Hu Zhi-Yuan(胡志远)[a)b)†], Liu Zhang-Li(刘张李)[a)b)], Shao-Hua(邵 华)[a)], Zhang Zheng-Xuan(张正选)[a)], Ning Bing-Xu(宁冰旭)[a)b)], Chen Ming(陈 明)[a)b)], Bi Da-Wei(毕大炜)[a)], and Zou Shi-Chang(邹世昌)[a)]

[a)] *Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai* 200050, *China*

[b)] *Graduate University of the Chinese Academy of Sciences, Beijing* 100049, *China*

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This paper investigates the effects of gamma-ray irradiation on the Shallow-Trench Isolation (STI) leakage currents in 180-nm complementary metal oxide semiconductor technology. No hump effect in the subthreshold region is observed after irradiation, which is considered to be due to the thin STI corner oxide thickness. A negative substrate bias could effectively suppress the STI leakage, but it also impairs the device characteristics. The three-dimensional simulation is introduced to understand the impact of substrate bias. Moreover, we propose a simple method for extracting the best substrate bias value, which not only eliminates the STI leakage but also has the least impact on the device characteristics.

Keywords: ionizing radiation, shallow trench isolation, trapped charge, total dose effects

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1. Introduction

Radiation effects[1] and predictions[2,3] are major challenges when using semiconductor devices in radiation environments. Aggressive semiconductor scaling has reduced the susceptibility of most deep-submicron complementary metal oxide semiconductor (CMOS) technologies to ionizing radiation damage. This is due primarily to the fact that, to first order, radiation-induced defect buildup in gate oxides scales with the oxide film thickness.[4] Ultra-thin gate oxides employed in advanced CMOS technology nodes significantly eliminate the threshold shift since total ionizing dose radiation induced oxide-trapped charge.[5−7] However, the Shallow-Trench Isolation (STI) oxide used to isolate transistors still has a thickness of several 100 nm, therefore this oxide is expected to be very sensitive to radiation. The charge trapping in the sidewall of trench oxides results in excessive leakage by inverting the channel of the parasitic transistors in NMOS transistors.[8,9] This effect is illustrated schematically in Fig. 1, which shows that an MOS transistor can be equivalent to a main transistor with two parasitic transistors connected in parallel. Prior to radiation exposure, the leakage current of the parasitic transistors is low due to the relatively large effective gate oxide thickness (high threshold voltage of the parasitic devices) relative to the main transistor. However, after ionizing radiation, positive oxide-trapped charges are trapped in the STI oxide which causes the negative shift of threshold voltage. At a certain total dose level, these parasitic devices will turn on even with a zero gate bias. This parasitic current counts to the main transistor I–V characteristics and becomes the dominant contributor to off-state drain-to-source leakage current in n-channel MOSFETs.[10]

Niu *et al.*[11] provided a method for suppressing the parasitic leakage by applying a negative substrate bias during the operation. However, the substrate bias also has negative impact on the device characteristics, such as increasing the threshold voltage of the main transistor, thus decreasing the driven current. Consequently, it is imperative to find a proper substrate value, which not only completely eliminates the STI leakage but also has smallest influence on the device. In this work, we study the substrate bias on the impact of total ionizing effect in detail, from which a

†Corresponding author. E-mail: Zhiyuan.hu@gracesemi.com

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simple method for extracting the best substrate bias is proposed.

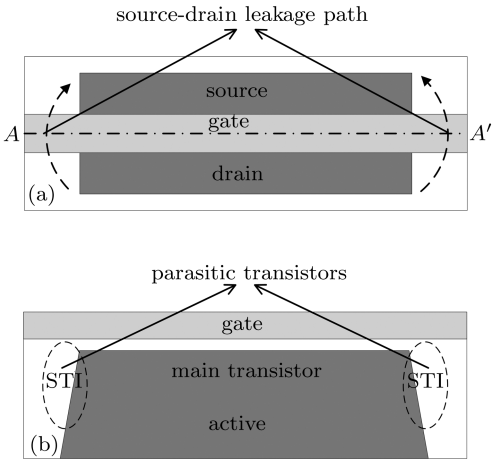


Fig. 1. (a) Diagram of NMOS layout and the drain-to-source leakage path at the channel edge. (b) Cross-section of (a) along the dashed line AA' indicates that an MOS transistor can be considered as a main transistor with two parasitic transistors connected in parallel.

2. Experimental details

The devices used in this work were fabricated in 180-nm CMOS technology. STI is introduced for field isolation filled by high density plasma oxide. The STI with very steep sidewalls (∼87°) has a thick oxide about 390 nm. Core NMOS transistors with different widths/lengths (including $W/L = 10$ μm/10 μm, 10 μm/0.5 μm, and 10 μm/0.18 μm) were selected as samples in our study. The gate oxide thickness is 3 nm. The source and drain are high N-type doped and the substrate is retrograde P-well. All the samples are ceramics packaged.

The experiments were conducted in Xinjiang Technical Institute of Physics and Chemistry, the Chinese Academy of Sciences, and ^{60}Co γ-ray was used as the radiation source. During the γ-ray irradiation, all the samples were biased with all terminals grounded except the gate kept at 1.8 V. The dose rate was typically around 205 rad(Si)/s, and the total dose levels achieved 800 krad (Si). Bias was removed from the transistors, and I–V measurements were taken by using an HP4140B parameter analyser at room temperature immediately (within 2 minutes) after irradiation. To ensure experimental results are immune to the annealing process, the time between irradiation exposures was controlled within half an hour.

3. Experimental results and discussions

3.1. The I_{DS}–V_{GS} characteristics

Figure 2 shows the experimental I_{DS}–V_{GS} characteristics as a function of total dose for the core NMOS. The devices were measured at $V_{SUB} = 0$ V and $V_{DS} = 0.05$ V. At 100 krad (Si), the I–V curves almost coincide with the pre-irradiation result. The radiation induced trapped charge trapping in the STI oxide is not enough to invert the trench sidewall channel, thus no leakage current degradation could be observed. However, the drain current at $V_{GS} = 0$ V (off-state leakage) reaches 1 nA at 200 krad (Si), which is almost 3 orders higher than the pre-value. At this time, a conductance path along the STI sidewall has been created through which leakage current flows. As the total dose level increases, the leakage current continues to increase and gradually saturates at approximately 10^{-7} A. We can easily conclude that the radiation tolerance of this (unhardened) CMOS technology is between 100 krad (Si) and 200 krad (Si) for the core NMOS.

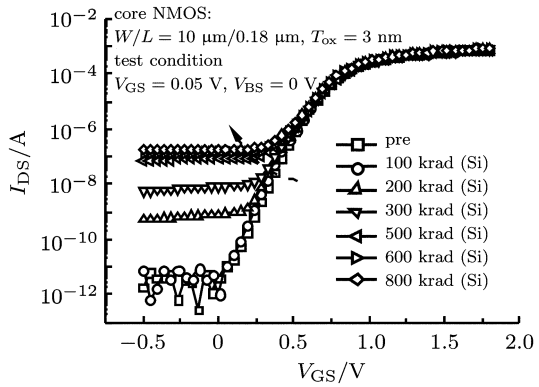


Fig. 2. The I_{DS}–V_{GS} characteristics before and after TID irradiation for core NMOS with $W/L = 10$ μm/0.18 μm.

It is interesting to observe that there is almost no hump effect in the subthreshold region. Previous work has shown a significant hump effect after irradiation.[11] Turowski *et al.*[12] used three-dimensional (3D) modeling with various sheet-charge values at the STI sidewall. They indicated that the sheet charge placed at the STI corner induced a significant subthreshold hump even at low dose level in a recessed STI structure, while the sheet charge placed at the deep trench oxide led to no hump effect. In other words, the charge trapped at the STI corner is

the major reason for the hump effect. So, almost no charge is trapped at the STI corner after irradiation for our test devices. This is not unexpected. As we know, the thickness of the corner oxide connecting the planar gate oxide and STI oxide is usually a little thinner than the gate oxide due to the lower oxide growth rate in this area. The gate oxide thickness is 3 nm, so the corner oxide thickness is less than 3 nm. It is well known that the total oxide trapped charge is proportional to oxide thickness. Due to the thin oxide thickness, there is little charge trapped at the corner. Radiation tolerance in thin oxide is further enhanced by the increased likelihood of positive charge annihilation or compensation by tunnelling electrons from the adjacent materials.[7] Consequently, no obvious subthreshold hump after irradiation is expected.

This conclusion also can be confirmed from another aspect. Niu *et al.*[11] pointed out that the charge trapped at the STI corner led to surface leakage (i.e., subthreshold hump) while the charge trapped in the deep trench resulted in deep leakage. The gate control was strong over the surface leakage but very weak over the deep leakage. As shown in Fig. 2, the leakage has a very weak dependence on the gate control for all dose levels. This means that the radiation induced parasitic leakage is the deep leakage, not the surface leakage, so the charge is trapped only in the deep trench and no charge is trapped at the corner. This is concordant with the above analysis. So, we think that the STI corner oxide thickness may play an important role in the radiation-induced subthreshold hump effect.

3.2. Effect of operating substrate bias

The radiation hardness of negative substrate bias operated n-MOSFETs is important practically. Many transistors in high speed digital circuits operate with a negative substrate-to-source bias, such as the series-connected driven transistors in a CMOS logic cell and all of the pass transistors for data selection or clock control. It has been previously reported that negative substrate bias during measurement can suppress the radiation-induced STI leakage in a 0.35-μm SiGe BiCMOS technology.[11] Figure 3 shows the $I_{\rm DS}$–$V_{\rm GS}$ curves in linear region ($V_{\rm DS}$ = 0.05 V) at a dose level of 500 krad (Si) for a series of substrate biases. At $V_{\rm SUB}$ = 0 V, the off-state leakage current reaches 10^{-7} A. This big leakage makes the transistor turn off incorrectly, thus increasing the static power consumption and even causing circuit functional failures. When we apply a negative substrate bias $V_{\rm SUB} = -0.45$ V, the leakage sharply decreases to less than 1 nA. But it is still 3-orders higher than the pre-irradiation value ($\sim 10^{-12}$ A). The negative substrate bias can efficiently suppress the STI leakage, but $V_{\rm SUB} = -0.45$ V seems to be insufficient to completely cut off the parasitic conduction paths. When the substrate bias decreases to −0.9 V, then no leakage current degradation is observed. As we know, radiation can introduce charge trapped in the STI oxide, thus shifts the threshold voltage of the parasitic transistors. At a certain dose level, the parasitic transistors will turn on even with a zero gate bias. The negative substrate, in fact, increases the threshold voltage of the parasitic transistor (body effect) and makes it more difficult to turn on after radiation. Therefore, we intuitively expect the observed radiation-induced STI leakage to be suppressed by a negative operating substrate bias. The radiation tolerance is less than 200 krad (Si) with $V_{\rm SUB}$ = 0 V while it increases to no less than 500 krad (Si) with $V_{\rm SUB} = -0.9$ V. Negative substrate bias, therefore, provides a means of radiation hardening. As the substrate bias decreases, the device should exhibit smaller leakage current degradation and better radiation tolerance.

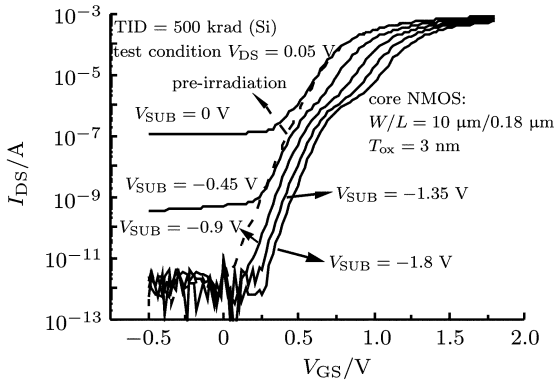


Fig. 3. The $I_{\rm DS}$–$V_{\rm GS}$ characteristics under different substrate bias values at 500 krad (Si) for core NMOS with W/L = 10 μm/0.18 μm.

Unfortunately, the negative substrate bias also has a negative impact on the device characteristics. First, it introduces a body effect which increases the threshold voltage of not only the parasitic transistor but also the main transistor. The increase of threshold voltage of the main transistor decreases the driven current for NMOS transistors, thus slows the speed of the circuit. Second, the negative substrate bias leads to obvious subthreshold hump effect, which worsens the characteristic subthreshold region. It should be pointed out that this hump effect is not due to the

charge trapped at the STI corner. The charge distribution should be unchanged with a negative operating substrate bias. This means, as discussed in Subsection 3.1, there is still no charge trapped at the STI corner when we apply a negative substrate bias. In fact, the negative substrate bias can enhance the coupling between the gate and the trapped charge in the deep trench, and thus provides better gate control over the leakage current (hump effect).[11] The body effect and the hump effect are more serious with a smaller negative substrate bias. Figure 3 has shown that $V_{\rm SUB} = -0.9$ V can eliminate the leakage degradation at 500 krad (Si), but it does not mean that $V_{\rm SUB} = -0.9$ V is required to eliminate the leakage degradation at 500 krad (Si). Maybe $V_{\rm SUB} = -0.8$ V or even -0.7 V is enough. So it is important to find an appropriate $V_{\rm SUB}$ which can not only completely suppress the radiation-induced STI leakage but also has smallest negative impact on the device characteristics.

3.3. The 3D simulation

In order to gain an understanding of the impact of the substrate bias, a 3D simulation is introduced. Figure 4 shows the 3D simulation of the NMOS transistor, including the silicon region and two sides bounded by trench isolation. The trench is 390-nm deep with overfilled geometry. The doping level of the p-well is obtained by simulation process. The gate oxide is 3 nm. The models include conventional drift diffusion model for transport and Shockley Read Hall model for generation–recombination. Parallel electric field dependence mobility is required to model the velocity saturation effect. Simulation of the $I_{\rm DS}$–$V_{\rm GS}$ curve is calibrated from the experimental result of preradiation. Non-uniform charge distribution is applied to the STI sidewall. Figure 5 shows the 3D simulation results for the test devices. The charge placed at the top STI corner is responsible for the hump effect while the charge located below this region causes a large off-state leakage current.[11,12] Since there is almost no hump effect after irradiation, no charge is placed at the top 40 nm (if charge is placed at this area, there will be a significant hump effect) and constant charge density is applied below this region (40 nm to 390 nm) in the simulation. It can be clearly observed that the off-state leakage gradually decreases with the negative substrate bias as shown in Fig. 5(a). The simulation indicates that $V_{\rm SUB} = -0.3$ V can completely suppress the off-state leakage at a dose level of 300 krad (Si). Figure 5(b) shows the potential along the STI sidewall. Only when $V_{\rm SUB} \leq -0.3$ V is the potential along the entire STI (except the top 40 nm region) below zero. The $V_{\rm SUB} > -0.3$ V leads to the potential of some region being above zero (at the middle of the STI sidewall). As discussed above, only the region below the top 40 nm leads to off-state leakage current. This means that when the potential along the whole deep trench is below zero, the off-state leakage current is suppressed. So, if we just apply a negative substrate bias to make sure that the potential along the whole deep trench sidewall is below zero, the radiation hardening can be achieved.

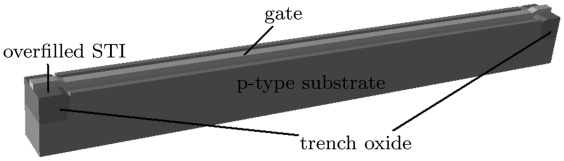


Fig. 4. Our baseline 3D model of an NMOS transistor bounded by the trench oxide on the two sides. The sheet charge is applied to the interface between the trench oxide and silicon. The trench is 390-nm deep with overfilled geometry.

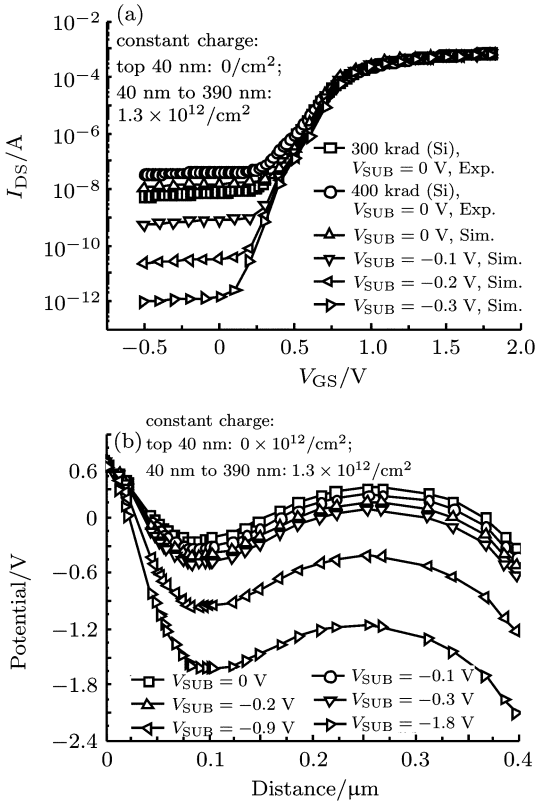


Fig. 5. Simulation of TID response under different operating substrate bias: (a) $I_{\rm DS}$–$V_{\rm GS}$ characteristics after irradiation; (b) potential along STI sidewall surface.

The simulation can tell us how much substrate bias is needed to completely suppress the radiation-

induced sidewall leakage. However, this method is complicated and the simulation needs much work. Moreover, it is also not accurate as we place constant charge along the entire deep trench, which is not the real case. So, if we can directly obtain this substrate bias value from the experimental results, it should be more applicable. In the next section, we will provide a method for extracting this value directly.

3.4. Extracting the best substrate bias value

The best substrate bias value should be able to completely suppress the STI leakage and be as small as possible (absolute value). In order to find out this value, the off-state leakage as a function of $V_{\rm SUB}$ is measured as shown in Fig. 6. During pre-radiation, there is no off-state leakage current even with a zero substrate bias. At this time, the substrate bias is not needed for leakage suppression. At a dose level of 500 krad (Si), significant leakage current is observed with $V_{\rm SUB} = 0$ V. But this leakage gradually decreases with the decrease of substrate bias. At a certain $V_{\rm SUB}$, this leakage can be completely eliminated. As the total dose level increases, the $I_{\rm DS}$–$V_{\rm SUB}$ curve shifts to the left. It indicates that a more negative substrate bias is needed to suppress the STI leakage. This is easily understood. A higher dose level will create more charge trapped in the STI oxide, thus lead to larger parasitic transistor threshold voltage shift. Consequently, a larger substrate bias (absolute value) is required to suppress this leakage current. In fact, it also means that a larger $V_{\rm SUB}$ results in a better radiation tolerance.

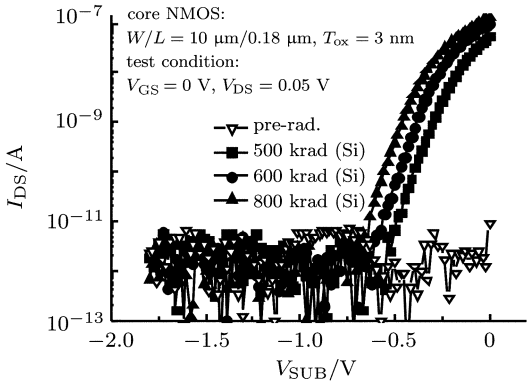


Fig. 6. The $I_{\rm DS}$–$V_{\rm SUB}$ characteristics before and after TID irradiation for core NMOS with W/L = 10 μm/0.18 μm.

Figure 7 shows the off-state leakage current as a function of $V_{\rm SUB}$ at a dose level of 500 krad (Si) for different transistor sizes. First, the shorter channel-length transistor shows larger off-state leakage current. It is well known that this leakage current is due to the parasitic transistor turning on after irradiation. The parasitic transistor has the same channel-length as the main transistor so the leakage is bigger in the short channel transistors as expected. Second, the short channel transistor requires a more negative substrate bias for suppressing the STI leakage, since the threshold voltage of the parasitic transistor is not the same in the devices with different channel-lengths pre-radiation. As we know, shorter channel transistor can exhibit a more severe drain induced barrier lowering effect, which eventually decreases the threshold voltage. As a result, for shorter channel transistors the threshold voltage of the parasitic transistor is smaller. For the transistors at the same total dose level, all the parasitic transistors should exhibit the same threshold voltage shift. Consequently, the parasitic transistor in shorter channel transistors has a smaller threshold voltage after irradiation. In order to turn off the parasitic transistor, the shorter-channel transistors surely require a more negative substrate bias.

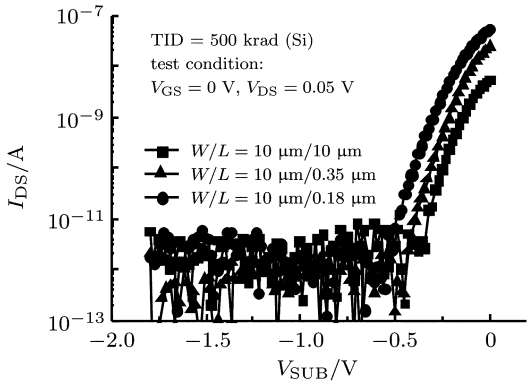


Fig. 7. The $I_{\rm DS}$–$V_{\rm SUB}$ characteristics at a dose level of 500 krad (Si) irradiation for core NMOS with W/L = 10 μm/10 μm, 10 μm/0.35 μm, and 10 μm/0.18 μm.

The test devices have an off-state leakage current of $\sim 10^{-12}$ A pre-irradiation. This current level is the same with the noise level of the measurement equipment. In order to obtain larger accuracy, we simply define the substrate bias corresponding to the leakage current dropping to 0.01 nA (it should be pointed out that this current value should be decided according to the actual requirement) after irradiation to the required $V_{\rm SUB}$ (abbreviated to $V_{\rm SUB,req}$) to completely suppress the radiation-induced STI leakage. $V_{\rm SUB,req}$ is the best substrate bias value which not only can completely suppress the STI leakage but also has

smallest negative impact on the device characteristics as discussed above. Similar to extracting the threshold voltage by the constant current method, the $V_{\rm SUB,req}$ as a function of total dose level for different transistor sizes is calculated as shown in Fig. 8. At the dose level between 0 krad (Si)∼100 krad (Si), $V_{\rm SUB,req} = 0$ V. As shown in Fig. 2, the device has almost no degradation at 100 krad (Si), so a negative substrate bias below this dose level is not required. When the total dose increases to 200 krad (Si) a negative substrate bias is needed for suppressing the STI leakage. We also know from Fig. 2 that significant leakage current degradation is observed at 200 krad (Si). With the increase of total dose level, the required $V_{\rm SUB,req}$ increases (absolute value). It can also be clearly observed that shorter channel-length transistors require more negative substrate bias, which is in agreement with Fig. 7. Moreover, we have shown in Fig. 3 that $V_{\rm SUB} = -0.9$ V can completely suppress the STI leakage at 500 krad (Si) for the NMOS transistor with $W/L = 10$ μm/0.18 μm. From Fig. 8, we know that $V_{\rm SUB} = -0.5$ V is enough. The $V_{\rm SUB} = -0.5$ V is surely a better choice than $V_{\rm SUB} = -0.9$ V as both values increase the radiation tolerance to 500 krad (Si) while the former has a less negative impact on the device characteristics.

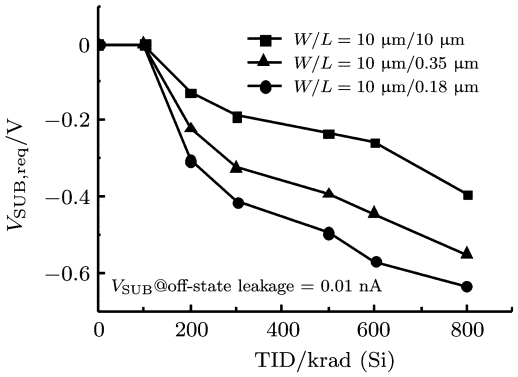


Fig. 8. The best substrate bias value for suppressing the STI leakage as a function of total dose level for different transistor sizes.

4. Conclusions

We have presented the experimental results of gamma-ray irradiation effects on the STI leakage currents in a 180-nm CMOS technology. The test devices do not show any subthreshold hump effect, which is contributed by the thin STI corner oxide. A negative substrate bias can effectively suppress the radiation-induced STI leakage. The 3D simulation indicates that the deep trench potential is responsible for this impact. A more negative substrate bias can give the device a better radiation tolerance. However, in order to minimize the impact of substrate bias on the device characteristics, the substrate bias should be as small as possible (absolute value). By studying the transistor $I_{\rm DS}$–$V_{\rm SUB}$ characteristics, a simple constant current method is proposed to find out the best substrate bias value.

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