A novel thin drift region device with field limiting rings in substrate*

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A novel thin drift region device with heavily doped N^+ rings embedded in the substrate is reported, which is called the field limiting rings in substrate lateral double-diffused MOS transistor (SFLR LDMOS). In the SFLR LDMOS, the peak of the electric field at the main junction is reduced due to the transfer of the voltage from the main junction to other field limiting ring junctions, so the vertical electric field is improved significantly. A model of the breakdown voltage is developed, from which optimal spacing is obtained. The numerical results indicate that the breakdown voltage of the device proposed is increased by 76% in comparison to that of the conventional LDMOS.

Keywords: field limiting ring, reduced surface field, reduced bulk field, breakdown voltage

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1. Introduction

The lateral double-diffused MOS transistor (LDMOS) has been widely used in intelligent power applications due to its compatibility with the very large integration process and easy integration with low-voltage devices.[1,2] In order to be feasibly isolated from the low-voltage devices, the LDMOS needs a thin layer and satisfies the reduced surface field (RESURF) principle.[3−5] For the conventional thin drift region LDMOS, the curvature of the N^+ contact at the drain causes the breakdown voltage (BV) to deteriorate sharply.[6] In order to improve the vertical BV of a thin drift region device, silicon-on-insulator (SOI) technology is used, which makes use the high critical breakdown electric field of the insulator.[7−9] However, the self-heating of the SOI can lead to a serious reliability problem and the operation conditions of the device are limited.[10−12] Additional electric field modulation achieved by introducing a new doping region can also improve the vertical BV. The device with an n^+-floating layer or an n-type buried layer embedded in the substrate to modulate the bulk electric field in the drift region has been presented and the BV is improved by above 70%. In the device with an n-type buried layer, the latter charge balance condition must be satisfied, and the process tolerance is small.[13] In the device with an n^+-floating layer, the parasitic transistor in the substrate is formed easily by the shielding effect of the electric field, which causes the BV to deteriorate.[14]

In this paper, a novel field limiting rings in substrate (SFLR) LDMOS is proposed for the first time. The heavily doped N^+ rings are employed to obtain a high breakdown voltage and a low on-resistance due to the transfer of voltage from the main junction to the SFLR junction. A model of the BV used to optimize the proposed device is presented.

2. Device structure and model

The schematic diagram of the cross section of the device with field limiting rings in the substrate is illustrated in Fig. 1. There are several heavily doped floating N^+ rings in the substrate underneath the drain. In the diagram, t_{sn} is the distance of the n-th N^+ ring from the surface of the device, r_n is the curvature radius of the depletion region outer boundary of the n-th ring junction, r_j and r_x are the junction depth

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and the x location of the SFLR, respectively, $L_{\rm d}$, $t_{\rm d}$ and $N_{\rm d}$ are the length, the thickness and the doping concentration of the drift region, respectively, $P_{\rm b}$ is the doping concentration of the buried layer underneath the channel, and $P_{\rm sub}$ is the substrate doping concentration.

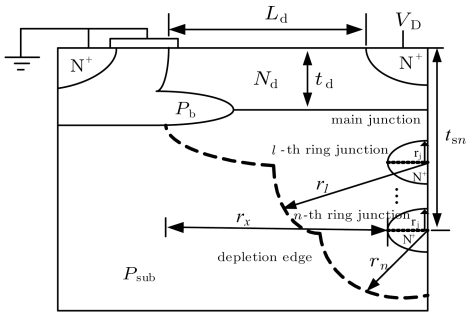


Fig. 1. Cross-section of SFLR LDMOS.

When the drift region is thin, the substrate of the device is almost depleted and the vertical voltage sustained by the drift region can be neglected. If all rings are absent, according to the theory of the abrupt pn junction, potential $\varphi_{\rm m}(y)$ and electric field $E_{\rm m}(y)$ in the substrate depletion region of the main junction can be expressed respectively as

$$\varphi_{\rm m}(y) = \frac{qP_{\rm sub}y_0^2}{2\varepsilon}\left(1-\frac{y}{y_0}\right)^2, \tag{1}$$

$$E = E_{\rm m}\left(1-\frac{y}{y_0}\right) = \frac{qP_{\rm sub}y_0}{\varepsilon}\left(1-\frac{y}{y_0}\right), \tag{2}$$

where $y_0 = \sqrt{2\varepsilon V_{\rm D}/(qP_{\rm sub})}$ is the thickness of the depletion region in the main junction, and ε is the permittivity of the silicon.

Now, we assume that only the first ring junction exists with a ring distance $t_{\rm s1}$ from the surface of the device, other ring junctions are absent. Solving the Poisson's equation of the first ring junction in the cylindrical coordinates under the boundary condition that the electrostatic potential and the electric field of the outer edge of the depletion region are both zero gives

$$E = \frac{qP_{\rm sub}}{2\varepsilon}\left(\frac{r_1^2-r^2}{r}\right), \tag{3}$$

$$V = \frac{qP_{\rm sub}}{2\varepsilon}\left[\frac{r_1^2-r^2}{2} - r_1^2\ln\left(\frac{r}{r_1}\right)\right]. \tag{4}$$

We assume the presence of the ring junction does not considerably perturb the depletion extension from the main junction, then the first ring junction voltage V_1 caused by the main junction is given by

$$V_1 = \frac{qP_{\rm sub}y_0^2}{2\varepsilon}\left(1-\frac{t_{\rm s1}}{y_0}\right)^2. \tag{5}$$

The voltage and the electric field of the first ring junction also satisfy the cylindrical coordinate Poisson's equations, which are written as

$$V_1 = \frac{qP_{\rm sub}}{2\varepsilon}\left[\frac{r_1^2-r_{\rm j}^2}{2} - r_1^2\ln\left(\frac{r_{\rm j}}{r_1}\right)\right], \tag{6}$$

$$E_{\rm r1} = \frac{qP_{\rm sub}}{2\varepsilon}\left(\frac{r_1^2-r_{\rm j}^2}{r_{\rm j}}\right), \tag{7}$$

where outer boundary r_1 can be obtained by solving Eqs. (5) and (6). The electric field peak of the main junction is reduced due to the transfer of the voltage to the first ring junction. The final electric field of the main junction is determined by the electric field difference between those caused by the drain and the first ring junction voltages, therefore, the final electric field peak at the main junction is given as

$$E_{\rm mf} = \frac{qP_{\rm sub}y_0}{\varepsilon} - \frac{qP_{\rm sub}}{2\varepsilon}\left[\frac{r_1^2-(r_{\rm j}+t_{\rm s1})^2}{r_{\rm j}+t_{\rm s1}}\right]. \tag{8}$$

Because of the screen effect of the first ring junction, we assume that the main junction voltage and the peak field do not change with the presence of the second ring junction. This approximation has been verified in the conventional device with field limiting rings in the drift region.[15] Thus, the second ring only has an effect on the first ring junction. The voltage and the edge electric field peak of the second ring junction in the case without the third ring junction are expressed as

$$\begin{aligned} V_2 &= \frac{qP_{\rm sub}}{2\varepsilon}\left[\frac{r_1^2}{2} + r_1^2\ln\left(\frac{r_{\rm j}+t_{\rm s2}-t_{\rm s1}}{r_1}\right) - \frac{(r_{\rm j}+t_{\rm s2}-t_{\rm s1})^2}{2}\right] \\ &= \frac{qP_{\rm sub}}{2\varepsilon}\left[\frac{r_2^2-r_{\rm j}^2}{2} + r_2^2\ln\left(\frac{r_{\rm j}}{r_2}\right)\right], \end{aligned} \tag{9}$$

$$E_{\rm r2} = \frac{qP_{\rm sub}}{2\varepsilon}\left(\frac{r_2^2-r_{\rm j}^2}{r_{\rm j}}\right). \tag{10}$$

The edge electric field peak of the first ring junction should be changed due to the presence of the second ring junction, which can be expressed as

$$E_{\rm r1f} = \frac{qP_{\rm sub}}{2\varepsilon}\left(\frac{r_1^2-r_{\rm j}^2}{r_{\rm j}}\right) - \frac{qP_{\rm sub}}{2\varepsilon}\left[\frac{r_2^2-(r_{\rm j}+t_{\rm s})^2}{r_{\rm j}+t_{\rm s}}\right]. \tag{11}$$

Following the same procedure, the voltages and the edge peak fields of the second and more ring junctions can be obtained easily. The breakdown voltage can be numerically calculated through the integral of the ionization equation.

The voltages and the electric field peaks of the main junction and all ring junctions are easily calculated according to the discussion above, and the optimal spacing is also obtained, with which the electric field peaks of the main junction and the ring junctions are simultaneously equal to the critical intensity $E_{\rm c}$,

$$E_{\rm c} = \left(\frac{6}{1.8 \times 10^{-35} \times r_{\rm j}}\right)^{1/7}.$$

It means that the avalanche breakdown will occur simultaneously at all vertical junctions.

3. Results and discussion

Figure 2 shows the electric field distributions on the surfaces of the SFLR and the conventional LDMOSs. There are only two electric field peaks at the drain and the source for the conventional LDMOS. An extra electric field peak is brought in for the SFLR LDMOS due to the electric field modulation effect caused by the $P_{\rm b}$ buried layer, which results in a more uniform electric field distribution by dramatically reducing the electric field peaks near the drain and the source.

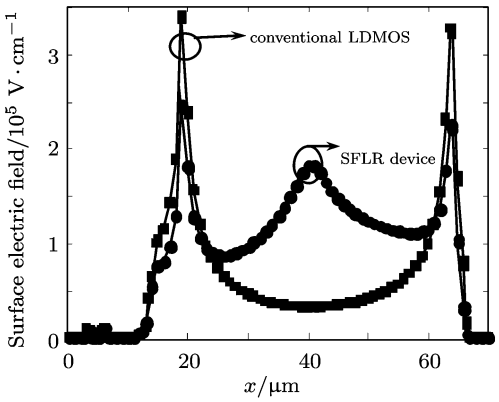


Fig. 2. Surface electric field distributions.

As shown in Fig. 3(a), there is only one electric field peak and the reverse bias voltage is sustained completely by the main junction $N_{\rm d}/P_{\rm sub}$ in the conventional LDMOS. As can be seen in Fig. 3(b), there are two new triangle-shape electric field peaks on the N^+ field limiting ring edge in the SFLR LDMOS besides the electric field peak at the main junction, and the drain voltage is sustained by the main and the field limiting ring junctions. The major portion of the reverse bias is sustained by the field limiting ring junction, as the field limiting ring number increases. So the potential is sustained by the main junction $N_{\rm d}/P_{\rm sub}$ in the conventional device, while the potential is sustained evenly by the main and the two-field limiting ring junctions in the SFLR LDMOS. Due to the modulation of the field limiting rings in the substrate and the improvement of the vertical breakdown voltage, the BV of the SFLR LDMOS reaches 600 V, while it is 340 V for the the conventional device.

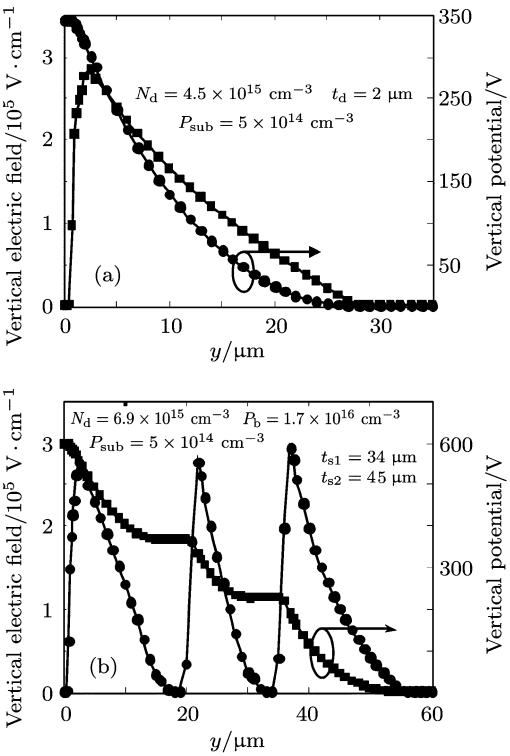


Fig. 3. Vertical electric field and potential distributions for (a) conventional and (b) SFLR LDMOSs.

In the SFLR LDMOS, more rings can be introduced underneath the drain in the substrate. It is obvious that the curves in Fig. 4 are characterized by both the linear and the saturation regions. In the linear region, because the rings can broaden the thickness of the depletion region in the substrate, the larger the number of the N^+ rings in the substrate, the higher the BV will be. The BV reaches nearly a saturated value when the number of the N^+ rings is increased to two. The saturated BV increases with the decrease of the substrate doping concentration. The SFLR LDMOS can be fabricated using the MOS process by adding three more steps, i.e., epitaxy, ion implantation, and epitaxy, to form the N^+ ring. Considering the cost

and the characteristics of the device, we suggest one or two rings for the device.

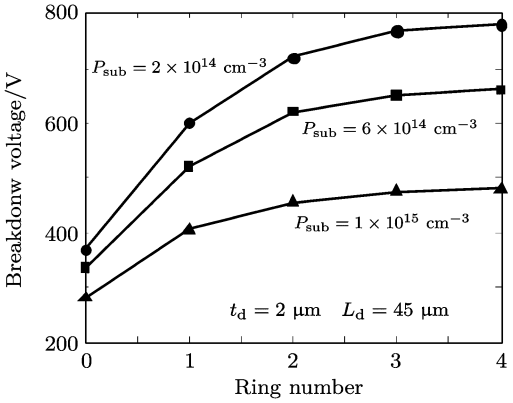


Fig. 4. Effects of ring number on breakdown voltage.

The breakdown voltage as a function of drift concentration N_d for different values of substrate concentration P_{sub} is shown in Fig. 5(a). The maximal breakdown voltage increases with the decrease of the substrate doping concentration, while the range and the magnitude of the optimal N_d value decrease. The breakdown voltage has a clear optimum. For a higher drift concentration, the drift region cannot be depleted fully, and thus a premature breakdown occurs, so the breakdown voltage is smaller. When the drift region concentration is low, the breakdown voltage increases with the increase of the drift region concentration. In general, the lower the substrate concentration, the higher the breakdown voltage. Figure 5(b) shows that for a fixed distance t_{s2} of the second field limiting ring, distance t_{s1} of the first field limiting ring has an optimum, which depends on the substrate and the drift region concentrations. With the increase of t_{s1}, the electric field peak at t_{s1} decreases, and that at t_{s2} increases. When the optimal value of t_{s1} is obtained, the electric field peaks at t_{s1} and t_{s2} are equal, and the maximum breakdown voltage is obtained, the reduced bulk field condition is satisfied. For reduced substrate concentration P_{sub} and increased drift concentration N_d, the optimal t_{s1} and the maximum breakdown voltage increase. The BV as a function of the ring location is illustrated in Fig. 5(c). For different values of P_{sub}, there is an optimal rang of r_x (optimal length of the ring is about 2–5 μm) with the maximum breakdown voltage. When r_x is small, the BV is decreased due to the difficulty in fully depleting the substrate under the rings. When r_x is large, the large curve effect of the ring junction causes the BV to decrease.

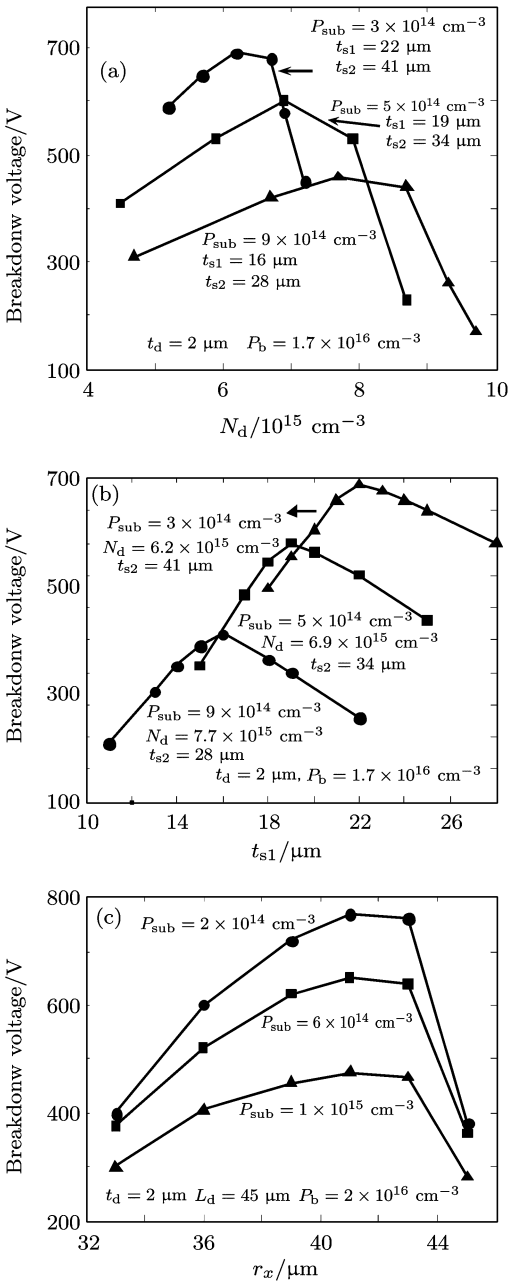


Fig. 5. Breakdown voltages versus (a) N_d, (b) t_{s1}, and (c) r_x.

In the practical device design, the critical factors are the arrangement and the distance from the device surface of the ring junction. The largest field will occur on the main junction edge and the field at the outset ring junction is relatively low when the SFLR is arranged in an equal spacing manner, which implies that both ring junctions have not been completely exploited. We may predict from the calculation results that the best design is a linearly decreased spacing, with which the electric field peaks are equal to each other at the main junction and the SFLR junctions and the maximum breakdown will be obtained as shown in Fig. 6. Distances t_{s1} and t_{s2} increase with

the decrease of the substrate concentration. If the distance of the SFLR is small or large, a high electric field occurs at the main junction or on the ring junction edge, leading to a lower breakdown voltage. A fair accordance between the analytical and the numerical results is found, showing the validity of the model presented.

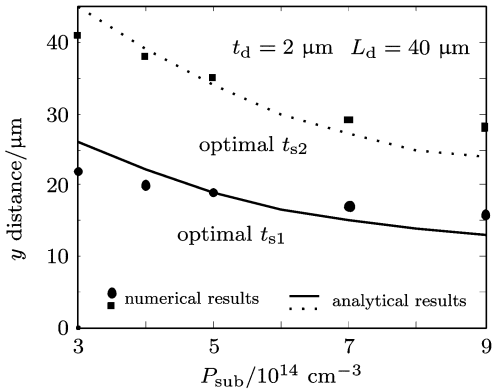


Fig. 6. Optimal ring distance t_{s1} and t_{s2} each as a function P_{sub}.

Figure 7 shows the dependences of the breakdown voltage and the on-resistance on the doping concentration of the drift region in the conventional and the SFLR LDMOSs. The breakdown voltage of the proposed device is increased by 76%. The doping

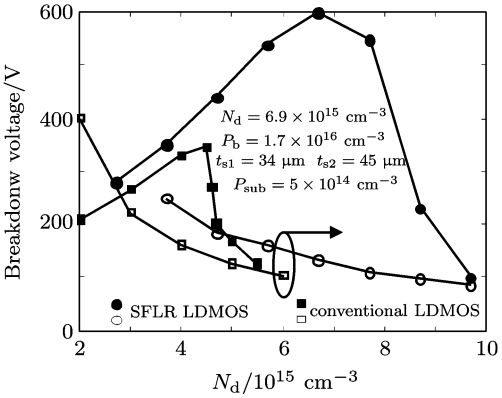


Fig. 7. Effects of N_d on breakdown voltage and on-resistance.

concentration of the drift region has an optimum value for each structure. However, the optimum N_d of the SFLR is about 70% higher than that of the conventional device owing to the auxiliary depletion effect of the SFLR, which causes the on-resistance of the SFLR device to reduce compared with that of the conventional LDMOS.

4. Conclusion

A new SFLR LDMOS structure is proposed. The electric field peak at the main junction is reduced, because the drain voltage is shared by the main junction and the field limiting ring junctions, which results in a significant improvement on the breakdown voltage. The electric field model is derived considering the device structural parameters. The analytical and the simulation results demonstrate an improvement on the trade-off between the BV and the on-resistance.

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