Suppressing the hot carrier injection degradation rate in total ionizing dose effect hardened nMOSFETs*

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Annular gate nMOSFETs are frequently used in spaceborne integrated circuits due to their intrinsic good capability of resisting total ionizing dose (TID) effect. However, their capability of resisting the hot carrier effect (HCE) has also been proven to be very weak. In this paper, the reason why the annular gate nMOSFETs have good TID but bad HCE resistance is discussed in detail, and an improved design to locate the source contacts only along one side of the annular gate is used to weaken the HCE degradation. The good TID and HCE hardened capability of the design are verified by the experiments for I/O and core nMOSFETs in a 0.18 μm bulk CMOS technology. In addition, the shortcoming of this design is also discussed and the TID and the HCE characteristics of the replacers (the annular source nMOSFETs) are also studied to provide a possible alternative for the designers.

Keywords: annular gate nMOSFETs, total ionizing dose effect, hot carrier effect, annular source nMOSFETs

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1. Introduction

The reliability of spaceborne integrated circuits (ICs) is dominated by environmental radiation induced effects and the intrinsic long-term degradation of the devices in the ICs.[1,2] The long-term intrinsic reliability issues, such as the negative bias temperature instability (NBTI), the hot carrier effect (HCE) and the time dependent dielectric breakdown (TDDB), have already been widely studied for the terrestrial ICs.[3−5] The issues also exist in the spaceborne devices and have also been widely considered.[6]

As the common rectangular gate nMOSFETs are sensitive to the total ionizing dose (TID) effect, annular gate nMOSFETs are frequently used in the spaceborne ICs. However, not only the TID effect but also the HCE is a main reliability issue for the nMOSFETs. The implication is that annular gate nMOSFETs may have a lifetime shorter than expected, because we have ignored their hot carrier injection (HCI) degradation.

Based on the one-dimensional (1D) NBTI reaction and diffusion (R–D) model, Kufluoglu and Alam[7] proposed a two-dimensional (2D) R–D model to explain why the hot carrier injection degradation time exponent of a rectangular gate nMOSFETs was 0.5. They further proposed based on a three-dimensional (3D) R–D model that the time exponent could reach 0.75 for very small annular gate nMOSFETs. They are the first to theoretically predict that annular gate nMOSFETs have a higher HCI degradation rate than that of rectangular gate ones. Even though the R–D model had been verified to be not suitable(or maybe needs to be revised) for describing the HCI degradation by Saha *et al.*,[8] Silvestri *et al.*[9] found experimentally that the time exponent (0.65) of annular gate nMOSFETs was actually larger than that (0.5) of rectangular gate ones. Their device simulation results further showed that the electric field peaks existed on the corners of the annular gate. The studies show that the non-uniformity of the electric field enhances the HCI degradation rate.

In this paper, in order to weaken the electric field peak induced HCI degradation rate, the source contacts are intentionally located only along one side of the annular gate to reduce the HCI degradation rate. As the most advanced radiation-hardened ICs in the market are still using the custom 150 nm process,[2] the TID effect and the HCI resistance of the design has been verified for I/O and core samples in a 0.18 μm bulk CMOS technology based on the commer-

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cial foundry. At the same time, the shortcoming of the design is also discussed. The TID and the HCI characteristics of the replacers (the annular source nMOSFETs) are studied to provide a possible alternative for the spaceborne IC designers.

2. Theory analysis

Along with the technology scaling down, the significant threshold voltage (V_{th}) shift caused by the TID has already been reduced, the drain (D) to source (S) leakage caused by the charge buildup in the shallow trench isolation (STI) has already become the main reliability threat.[10] Figure 1(a) shows the cross section along the cut line in Fig. 1(b), and Fig. 1(c) shows the leakage path under the gate. Due to the hole buildup in the STI and the N^+–P–N^+ structure under the gate, a weak inversion layer is produced along the edge of the STI, so the leakage will increase with the total dose increasing. Different from the rectangular gate nMOSFET, the annular gate nMOSFET breaks the N^+–P–N^+structure and further breaks the leakage path (as shown in Fig. 2), so the intrinsic leakage path does not exist in the annular gate nMOSFET, which then becomes the prior choice for the radiation-hardened-by-design (RHBD) ICs.

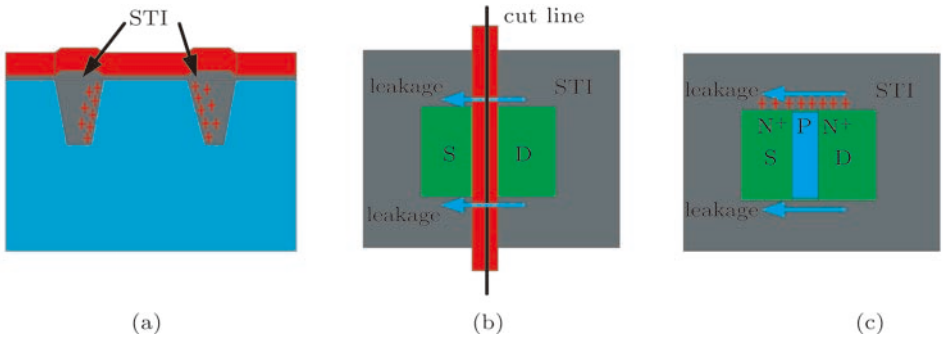


Fig. 1. (colour online) Intrinsic leakage path existing in the common rectangular gate nMOSFET: panel (a) shows the hole buildup in the STI, panel (b) shows the planform of the rectangular gate nMOSFET, and panel (c) shows the leakage path along the edge of the STI.

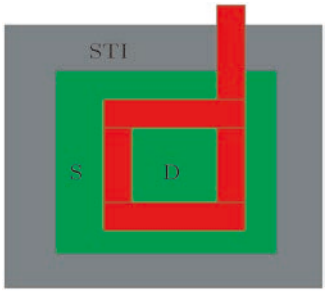


Fig. 2. (colour online) Annular gate nMOSFET without the intrinsic leakage path.

However, the gate has an unbalanced boundary with the source and the drain regions in the annular gate nMOSFET, and there are four corners in the annular gate configuration, which lead to the non-uniformity of the electric field in the channel. Especially, electric field peaks exist on the corners, which can enhance the HCI degradation rate.[9]

In the MOSFET, a portion of the hot carriers (heated by the electric field or the impact ionization) can overcome the surface barrier and be injected into the oxide layer. A fraction of the injected hot carriers can be trapped by the oxide traps, and interface traps can be produced at the SiO_2/Si interface by the hot carriers.

The interface traps can be produced by breaking the Si–O and the Si–H bonds.[11,12] The Si-O bonds can be broken by the injected hot holes (HHs)[12,13] and the Si-H bonds can be broken by the cold holes (CHs)[14] or the H^+ [15] during the reaction and diffusion process. According to different theories, the injected hot electrons (HEs) can lead to the anode hole (which is the CH) injection or the release of the H^+ from the oxide layer, then the CHs or the H^+ will come to the interface and break the Si–H bonds by the electrochemical reaction.[14,15] So the HHs and the HEs both seem to be very critical to the HCI degradation. However, experiments about the degradation of substrate HE and substrate HH injections show that the traps produced by the thermal holes are several orders of magnitude higher than that produced by the thermal electrons,[16] and the HCI degradation peaks in the HH injection regimes ($V_{gs} \approx V_{ds}/2$ for the older technology and $V_{gs} \approx V_{ds}$ for the advanced technology, where V_{gs} and V_{ds} are the gate to source and the drain to source voltages, respectively).[17,18] So the HHs play

a major role in the HCI degradation. The impact ionization rate can be regarded as an important criterion to evaluate the HCI degradation, because the HHs come mainly from the impact ionization.

The TCAD device simulations have the looking-inside capability to analyse the mechanism details for the HCI, so the device simulations have been performed to gain a deep insight into the annular gate nMOSFET. The device used for the simulation is shown in Fig. 3(a), the device structure is the layout used to fabricate the experimental core sample, and the doping profiles are based on our previous data used in the rectangular gate nMOSFETs.[19,20] In the simulation, V_{gs} and V_{ds} are elevated to the target voltage. Figure 3(c) shows the impact ionization rates along the gate inner borderline and 80 nm under the surface. Due to the symmetry, only half of the data are presented. The impact ionization rate peaks on the corner and the north (or the south) side, while along the east or the west side, the impact ionization rate is quite uniform, which is similar to that in the rectangular gate nMOSFETs. The result shows why the annular gate nMOSFETs are worse than the rectangular ones due to the HCI degradation.

In order to reduce the influence of the corner on the HCI degradation, the source contacts are alternatively designed to locate along two sides (east and west) or only along one side (east or west) in the simulation. Figure 4(a) shows that the impact ionization rate for the first alteration is almost unchanged, which indicates that this alteration cannot effectively change the HCI degradation rate compared with the original design. The second alteration significantly change the distribution of the impact ionization rate, which may introduce surprising improvement on the HCI degradation, as shown in Fig. 4(b).

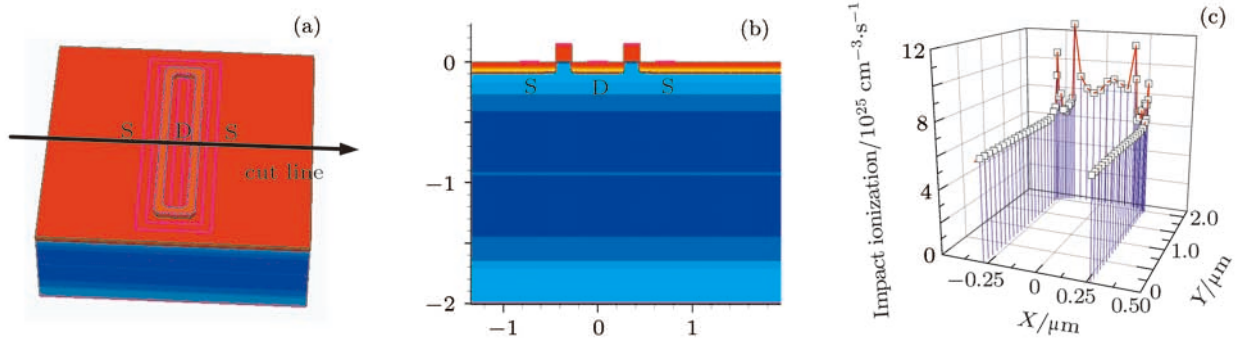


Fig. 3. (colour online) Device used for the simulation: panel (a) shows the whole device, panel (b) shows the cross section along the cut line. (c) Impact ionization rates along the inner borderline and 80 nm under the surface.

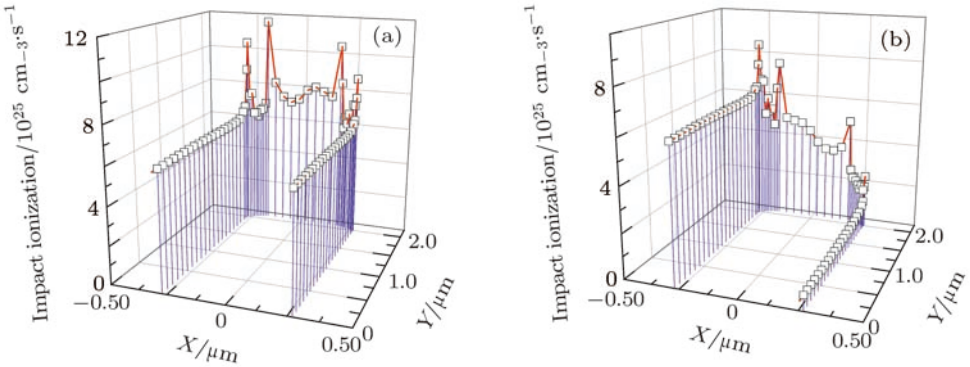


Fig. 4. (colour online) Impact ionization rates along the gate inner borderline for (a) source contacts located along the east and the west sides, and (b) source contacts located only along one side (east or west).

3. Experimental details

The nMOSFETs used in our experiments are manufactured by a domestic foundry using a 0.18 μm bulk silicon process. The gate oxide thickness (T_{ox}) is 3.8 nm for the core samples and 6.6 nm for the I/O ones, and the source/drain junction depth is 160 nm.

The TID tests are performed at the worst-case bias condition $V_{gs} = V_{dd}$, where V_{dd} is the supply voltage. The radiation dose rate is 0.6 krad(Si)/s and

the total doses are 100 krad(Si) and 300 krad(Si). The HCI tests are also performed under the worst-case stress condition. As the nMOSFETs used in the experiments are still manufactured in the deep submicron technology, the stress condition used in the experiments is still $V_{gs} = V_{ds}/2$. The source and the substrate are held at the ground potential, and the gate and the drain are both biased under the target voltage, V_{ds} is typically above normal operating voltage V_{dd} to speed up the tests. The $V_{ds} = 2.4$ V and $V_{gs} = 1.2$ V are used for the core samples, and $V_{ds} = 5.0$ V and $V_{gs} = 2.5$ V are used for the I/O ones. All the tests are performed at room temperature and temperature dependency is not studied in this paper.

4. Experimental results

The TID experimental results are shown in Figs. 5 and 6, where W is the gate width and L is the gate length. The results show that the new alteration does not change the good TID hardened characteristics for the annular gate nMOSFET. When the total dose is 300 krad(Si), there is still no leakage observed in the annular gate nMOSFETs (both the core and the I/O samples). However, the leakage current increases at least 5 orders of magnitude for the rectangular gate nMOSFET.

The HCI experimental results are shown in Fig. 7. For the core samples, the annular gate nMOSFETs even have better resistance against the HCI degradation than the rectangular gate ones (as shown in Fig. 7(a)). For the I/O samples, when the stress time is short, the negative V_{th} shift appears in the experiments, which indicates that due to the thicker oxide layer, the trapping of the HHs determines the degradation in the early period. With the acceptor interface trap increasing, the degradation is determined by the interface traps and the positive V_{th} shift appears and behaves as a power law with time.

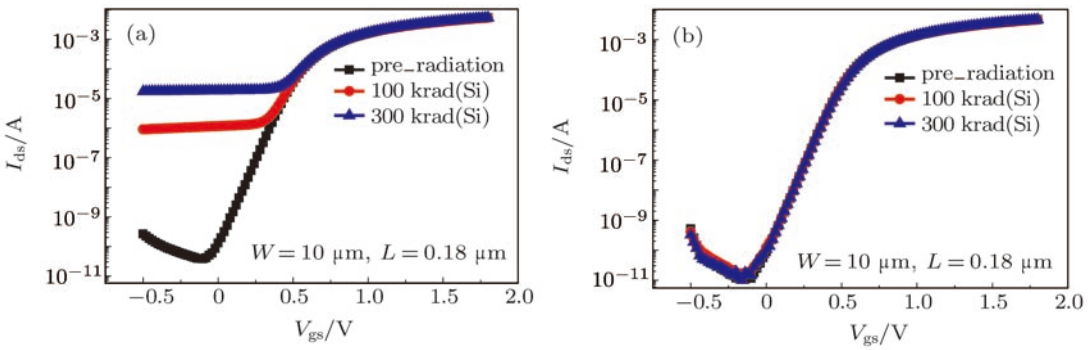


Fig. 5. (colour online) TID characteristics of rectangular (a) and annular (b) gate nMOSFETs for the core samples.

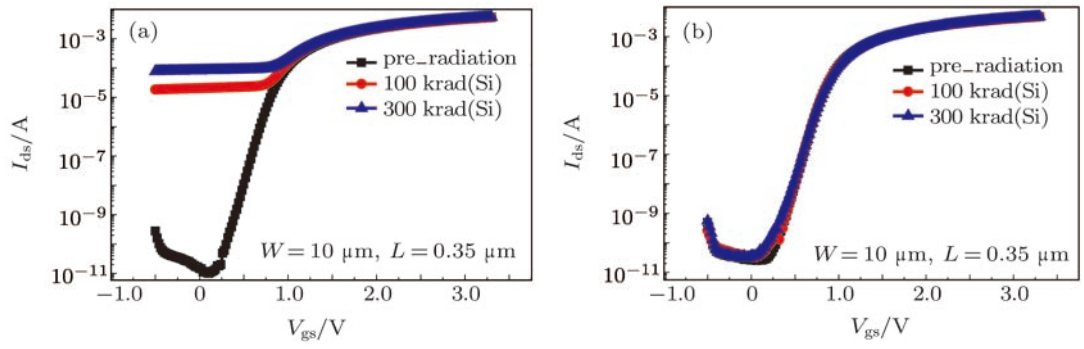


Fig. 6. (colour online) TID characteristics of rectangular (a) and annular (b) gate nMOSFETs for the I/O samples.

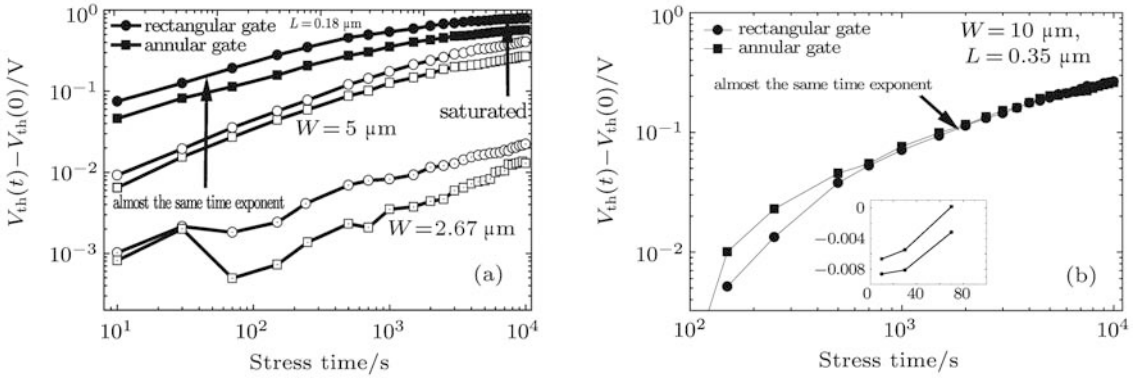


Fig. 7. HCI degradations for annular and rectangular gate nMOSFETs for (a) the core and (b) the I/O samples, the insert shows the results at small stress time.

The results show that all of the annular gate nMOSFETs do not present higher HCI degradation rates than that of the rectangular nMOSFETs, the time exponents for both the annular and the rectangular gate nMOSFETs (core and I/O, respectively) are almost the same, the larger time exponent does not appear. In order to verify that these characteristics are not only applicable to the bigger nMOSFETs, the experiments for the smaller ones are also performed. As shown in Fig. 6(a), even for the smallest annular gate nMOSFET (W = 2.67 μm, to meet the design rule), the same characteristics still appear in the HCI experiments.

5. Discussion

Even though the TID and the HCI experiments show that these annular gate nMOSFETs have good resistances against both the TID and the HCI threats, the performances of these nMOSFETs may degrade due to the source contacts located only along one side of the annular gate (even we have already tried to increase the width of the east or the west side under the permission of the design rule as show in Fig. 3(a)). As a possible alternative, the annular source nMOSFETs can also be used in the RHBD ICs , in which the intrinsic leakage path does not exist either as shown in Fig. 8. The linear ($I_{\rm dlin}$) and the saturated ($I_{\rm dsat}$) currents should be almost the same as those of the common rectangular gate ones, which is ascribed to the fact that both of them have similar gate configurations. As shown in Table 1, $I_{\rm dlin}$ and $I_{\rm dsat}$ of the annular gate nMOSFET are both smaller than those of the rectangular one, while $I_{\rm dlin}$ and $I_{\rm dsat}$ of the annular source nMOSFET are almost same as those of the rectangular one, which indicates that compared with the annular gate nMOSFET, the redesigned annular gate nMOSFET has the minor performance.

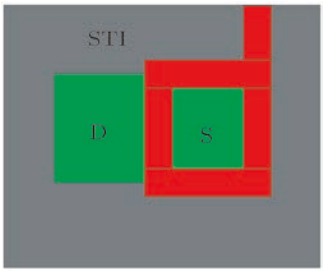


Fig. 8. (colour online) Annular source nMOSFET without any intrinsic leakage path.

Table 1. The $I_{\rm dlin}$ and $I_{\rm dsat}$ for the three types of nMOSFETs. The percentages in the bracket are the ratio of $I_{\rm dlin,dsat}$ (AG, AS) to $I_{\rm dlin,dsat}$ (CR). The W = 10 μm, L = 0.18 μm for the core sample, and L = 0.35 μm for I/O one.

Sample	$I_{\rm dlin}$/μA			$I_{\rm dsat}$/μA		
	CR[a)]	AG[b)]	AS[c)]	CR[a)]	AG[b)]	AS[c)]
Core	721.20	568.44(78.82%)	737.24(102.22%)	3780.64	3419.83(90.46%)	3786.40(100.15%)
I/O	355.95	294.37(82.70%)	373.44(104.91%)	4844.53	4372.47(90.26%)	4978.53(102.77%)

[a)] CR denotes common rectangular nMOSFETs.
[b)] AG denotes annular gate nMOSFETs.
[c)] AS denotes annular source nMOSFETs.

The TID and the HCI experimental results for the annular source nMOSFETs are shown in Figs. 9 and 10. The results indicate that the annular source nMOSFETs also have good TID and HCI resistances. Figure 10 further shows that for the core sample, the annular source nMOSFETs almost have the same HCI degradation characteristics as those of the common rectangular gate nMOSFETs. For the I/O samples, the annular source nMOSFETs have a little more HCI degradation, however the time exponent is almost the same due to their similar rectangular gate configurations. So, the HCI degradation rate of the annular source nMOSFET is also almost unchanged compared with that of the common annular gate nMOSFET. The annular source nMOSFET has a larger area than the annular gate nMOSFET (about 1.5 times larger according to our layout data). So, the selection depends on the trade-off between the area and the performance.

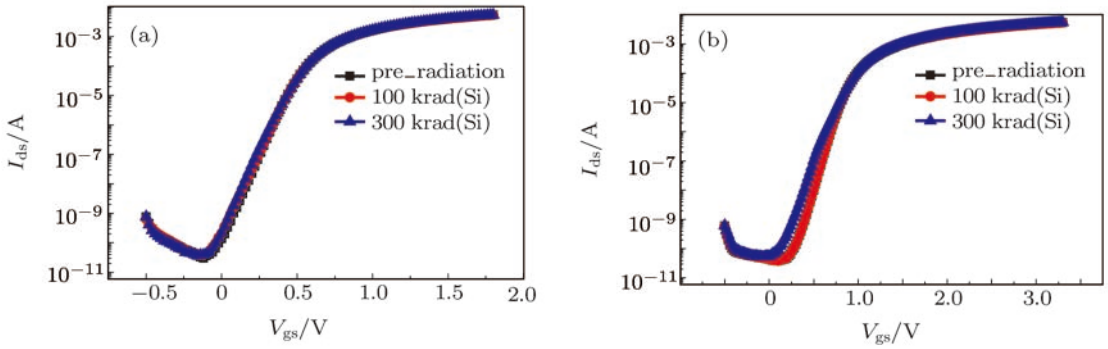


Fig. 9. (colour online) TID characteristics of annular source nMOSFETs for (a) core and (b) I/O samples.

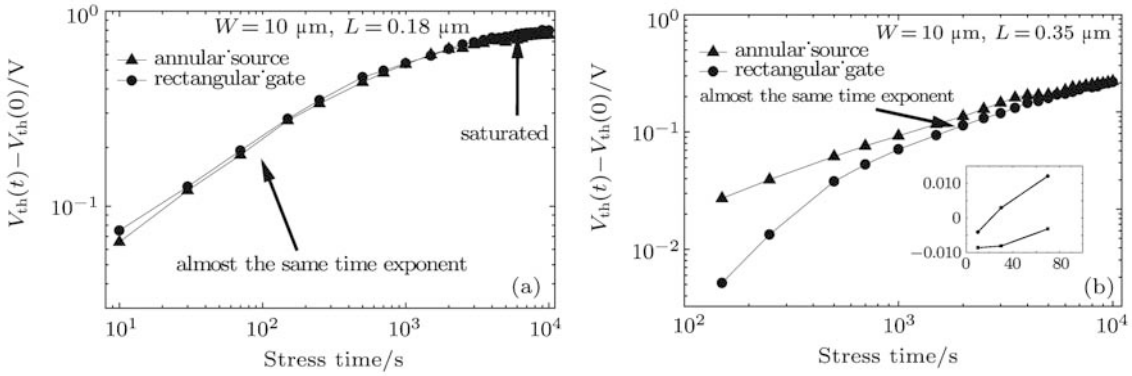


Fig. 10. HCI degradations of annular source nMOSFETs and rectangular gate nMOSFETs for (a) core and (b) I/O, the insert shows the results at small stress time.

6. Conclusion

In this paper, the reason for the annular gate nMOSFET to have good TID but bad HCE resistance is discussed in detail, and an improved design to locate the source contacts only along one side of the annular gate is used to weaken the HCI degradation. The good TID and HCI resistances are verified for the annular nMOSFETs in the I/O and the core samples in a 0.18 μm bulk CMOS technology. Both the annular and the common rectangular gate nMOSFETs have almost the same HCI time exponents, and a larger time exponent does not appear in our experiments even for the smallest device (meeting the foundry design rule). At the same time, the shortcomings of the annular gate nMOSFETs are also discussed, and the TID and the HCI characteristics of the replacer (the annular source nMOSFET) are also studied. The annular source nMOSFETs also have almost the same time exponents as the common rectangular ones due to their similar rectangular gate configurations.

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