Improved charge trapping flash device with Al_2O_3/HfSiO stack as blocking layer*

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In this paper, we investigate an Al_2O_3/HfSiO stack as the blocking layer of a metal–oxide–nitride–oxide–silicon-type (MONOS) memory capacitor. Compared with a memory capacitor with a single HfSiO layer as the blocking layer or an Al_2O_3/HfO_2 stack as the blocking layer, the sample with the Al_2O_3/HfSiO stack as the blocking layer shows high program/erase (P/E) speed and good data retention characteristics. These improved performances can be explained by energy band engineering. The experimental results demonstrate that the memory device with an Al_2O_3/HfSiO stack as the blocking layer has great potential for further high-performance nonvolatile memory applications.

Keywords: charge trapping flash, blocking layer, stack

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1. Introduction

For the increasing demands of scalable nonvolatile memory (NVM), charge trapping flash (CTF) memory based on localized charge storage has been widely investigated for sub-32 nm node generation.[1,2] However, for traditional SONOS-type or MONOS-type CTF devices, it is difficult to make the trade-off between erase speed and data retention.[3,4] If the tunneling oxide is thin, the erase speed is fast but the retention time is greatly reduced. To guarantee the retention time for ten years, the thickness of the tunneling oxide must be kept large enough so that the erase speed is reduced. As one of the solutions, the optimization of the blocking layer has attracted much attention in order to avoid electron tunneling from the blocking layer.[5,6] Replacing SiO_2 with a high-k material, such as HfO_2 and HfSiO, as the blocking layer of traditional SONOS-type or MONOS-type CTF devices increases the electric field across the tunnel oxide during the program/erase (P/E) operations. Therefore, it can achieve a faster P/E speed. However, they are not suitable for blocking layers due to the small energy band gap. However, with its large energy band gap but low permittivity, Al_2O_3 is used as a blocking layer to suppress charge leakage.[7] In order to utilize the advantages of the higher dielectric constant of HfSiO and the larger energy band gap of Al_2O_3, in this paper, we demonstrate a novel MONOS-type CTF device with a high-k Al_2O_3/HfSiO stack as the blocking layer. As compared with a device with a single HfSiO blocking layer or an Al_2O_3/HfO_2 stack as a blocking layer, fast P/E speed and good data retention characteristics are achieved simultaneously in the proposed structure.

2. Experiment

P-type, (100) orientation silicon wafers with 1 Ω·cm–10 Ω·cm resistivity were used as the starting substrate. After standard cleaning, a 4-nm tunnel oxide (SiO_2) was thermally grown by dry oxidation at a temperature of 900 °C. Then, a 7-nm Si_3N_4 trapping layer was formed on the SiO_2 tunnel oxide by using low pressure chemical vapour deposition (LPCVD). On one wafer (MH'ANOS: Al/HfSiO/Al_2O_3/Si_3N_4/SiO_2/Si), a 5-nm Al_2O_3 film was formed on the Si_3N_4 trapping layer by atomic layer deposition (ALD), followed by the co-sputtering of Hf and Si targets in an Ar+O_2 ambient to form a 10-nm HfSiO film. On one control wafer (MH'NOS:

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Al/HfSiO/Si_3N_4/SiO_2/Si), a 15-nm HfSiO film was deposited on Si_3N_4 by co-sputtering Hf and Si in an Ar+O_2 ambient. On the other control wafer (MHANOS: Al/HfO_2/Al_2O_3/Si_3N_4/SiO_2/Si), a 5-nm Al_2O_3 film was formed on Si_3N_4 by ALD, followed by sputtering Hf in an Ar+O_2 ambient to form a 10-nm HfO_2 film. The thicknesses of the HfO_2 and HfSiO films were controlled by adjusting the sputter-deposition rate. Subsequently, post deposition annealing (PDA) was performed at 1000 °C for 2 min. Finally, a 200-nm Al gate was deposited be using an e-beam evaporator as a gate electrode. The memory characteristics were investigated by using an Agilent C-V 590 and a Keithley 4200 semiconductor characterization system at room temperature. The schematics of these gate stacks are shown in Fig. 1. The band offset, the band gap and the dielectric constant can be estimated by referring to Refs. [8] and [9].

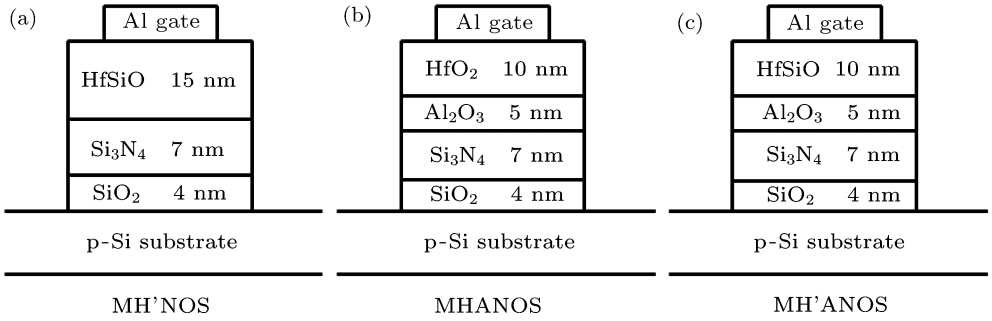


Fig. 1. Gate stacks of (a) MH'NOS, (b) MHANOS, and (c) MH'ANOS devices.

3. Results and discussion

3.1. P/E speed characteristics

In Figs. 2(a) and 2(b), P/E speed characteristics of the MH'ANOS and MH'NOS devices are displayed for several gate voltages. From the comparison, a similar P/E speed is observed when a 5-nm Al_2O_3 is added to replace part of the HfSiO blocking layer.

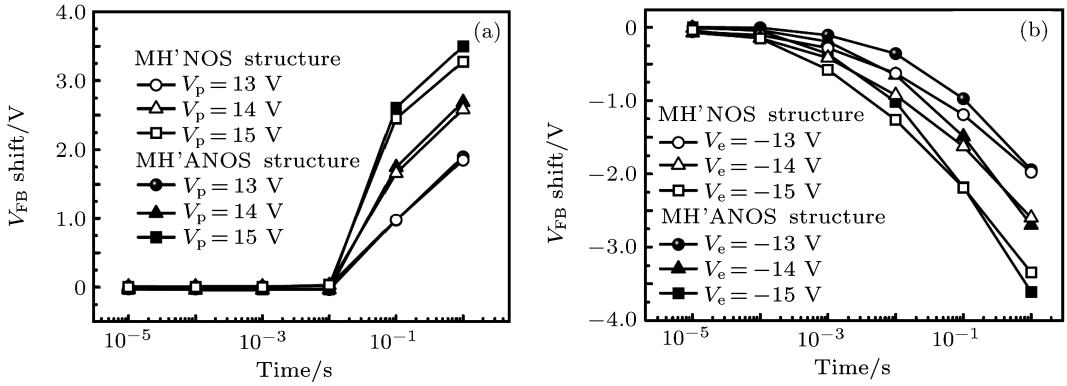


Fig. 2. (a) Program and (b) erase characteristics for MH'ANOS and MH'NOS devices.

For the program operation, by inserting the Al_2O_3, which has a smaller dielectric constant than HfSiO, the equivalent oxide thickness (EOT) of the gate stack is increased, thus the injecting field is reduced at the same program voltage, resulting in a lower program speed. However, due to the larger conduction band offset (ΔE_c) between Si_3N_4 and Al_2O_3 than that between Si_3N_4 and HfSiO, as shown by the energy band diagram under the program bias condition in Fig. 3(a), the insertion of Al_2O_3 layer provides a more efficient barrier for the electrons moving towards the top dielectric and thus increases the program speed. Due to the two factors mentioned above, there is a slight difference in the program speed between the MH'ANOS device and the MH'NOS device. Similarly, the erase speeds of these two devices can be

analysed by the differences of both dielectric constants and energy band diagram under the erase state, which is shown in Fig. 3(b).

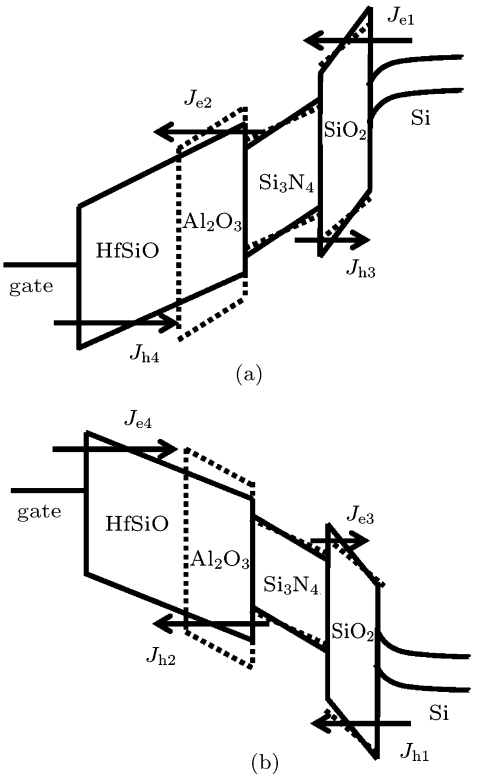


Fig. 3. Energy band diagram under (a) program and (b) erase state for MH'ANOS (dotted line) and MH'NOS (solid line) devices.

Figures 4(a) and 4(b) show the P/E speed characteristics under different gate voltages for the MH'ANOS and MHANOS devices. Compared with the MHANOS device, the MH'ANOS has a fast P/E speed. For example, as shown in Fig. 4(b), about 1.5-V flat-band voltage shift $\Delta V_{\rm FB}$ can be achieved in the MH'ANOS structure in about 30-ms erase time at $V_{\rm e} = -15$ V erase voltage. However, a 100-ms erase time is needed for the MHANOS structure.

For the erase speed of the Al_2O_3/HfSiO and Al_2O_3/HfO_2 blocking layer structures, due to the similar dielectric constants of HfSiO (Hf-rich) and HfO_2, the influence of dielectric constants on the electric field and the operation speed can be neglected. The improved erase efficiency of the MH'ANOS structure can be explained by the energy band diagram under erase state, as shown in Fig. 5(b). Due to the larger barrier formed by HfSiO than by HfO_2, more injected electrons from the control gate are suppressed for the Al_2O_3/HfSiO stack as a blocking layer. Therefore, an improved erase

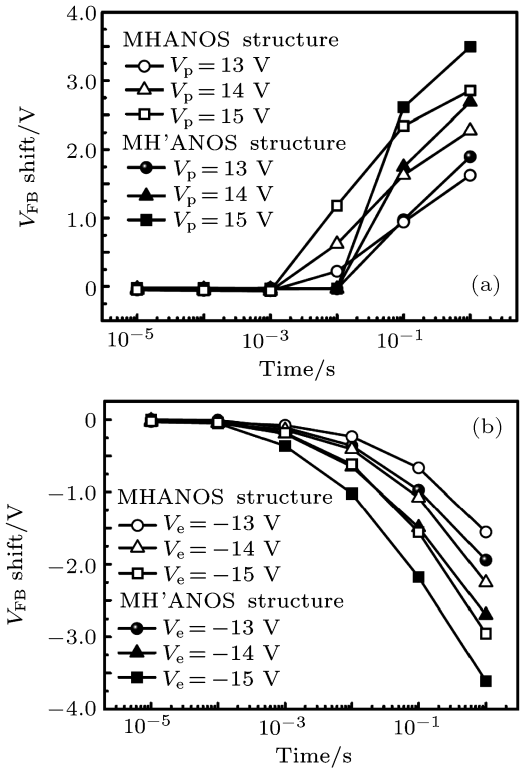


Fig. 4. (a) Program and (b) erase characteristics for MH'ANOS and MHANOS devices.

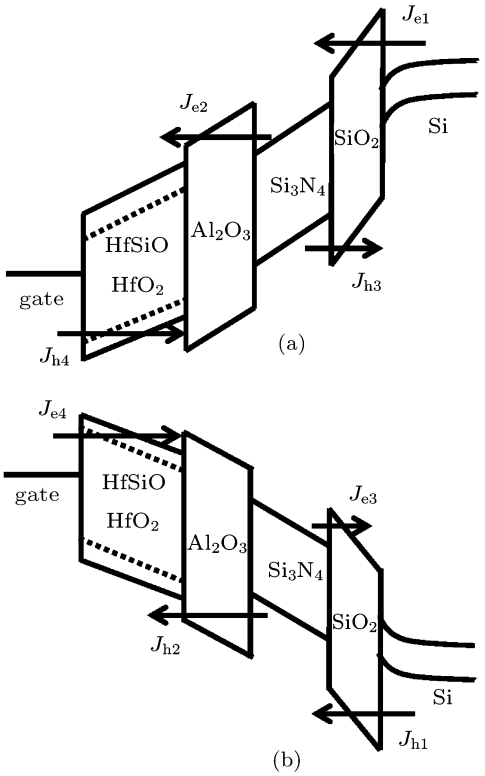


Fig. 5. Energy band diagram under (a) program and (b) erase state for MH'ANOS (solid line) and MHANOS (dotted line) devices.

speed is obtained for the MH'ANOS structure. Meanwhile, the enhancement of the program speed can be explained by the energy band diagram under the state of program operation similarly as shown in Fig. 5(a).

3.2. Retention properties

Data retentions are also measured and shown in Fig. 6, where the MH'ANOS structure shows the best data retention characteristic among the three devices. In our experiment, we compare the retention properties of these samples at room temperature (RT) by tracing the flat-band voltage shift of the programmed device as a function of time. As shown in Fig. 6(a), compared with the MH'NOS device with single HfSiO blocking layer, the MH'ANOS device, with an Al_2O_3/HfSiO stack as the blocking layer, has good data retention. It can be attributed to the insertion of Al_2O_3 layer, which provides a more sufficient barrier to suppress leakage through the blocking layer and thus improves data retention. Furthermore, for the retention characteristics of both the structures each with using the stack as blocking layer in Fig. 6(b), the improvement of MH'ANOS over MHANOS can be attributed to the larger ΔE_c between Al_2O_3 and HfSiO than that between Al_2O_3 and HfO_2, which makes the trapped electrons difficult to leak through the blocking layer. The insets show the schematic energy band diagrams of MH'NOS, MHANOS and MH'ANOS structures at the retention state.

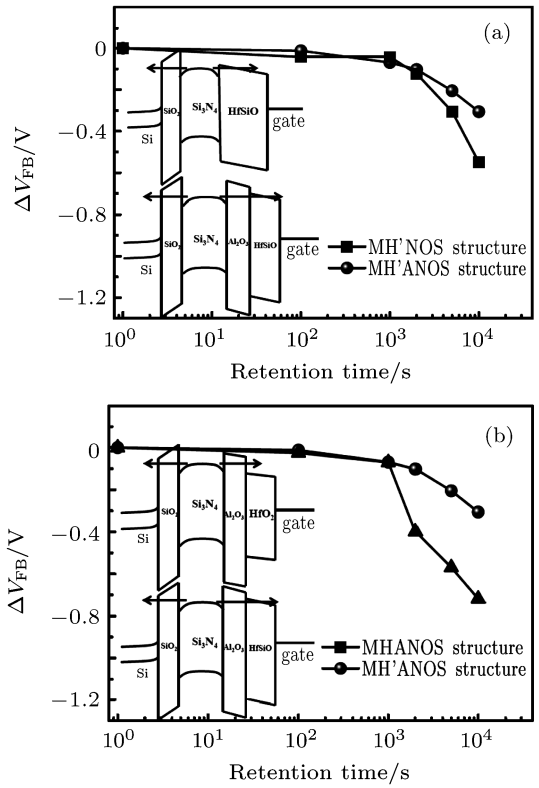


Fig. 6. Retention characteristics (a) for MH'NOS and MH'ANOS devices, (b) for MHANOS and MH'ANOS devices. The insets show the schematic energy band diagrams of MH'NOS, MHANOS and MH'ANOS structures at the retention state.

4. Conclusions

In this paper, we present a CTF memory device with a high-k Al_2O_3/HfSiO stack as a blocking layer. Compared with a single HfSiO layer and an Al_2O_3/HfO_2 stack as the blocking layer, the structure with an Al_2O_3/HfSiO stack as the blocking layer has a fast P/E speed and good data retention simultaneously. The improved performances can be explained by the energy band analysis. The presented results demonstrate that the novel high-k stack as blocking layer with the advantages of higher dielectric constant and larger energy band gap has strong potential in further scalable high-performance nonvolatile flash memory applications.

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