# Enhanced etching of silicon dioxide guided by carbon nanotubes in HF solution*

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This paper describes a new method to create nanoscale $SiO_2$ pits or channels using single-walled carbon nanotubes (SWNTs) in an HF solution at room temperature within a few seconds. Using aligned SWNT arrays, a pattern of nanoscale $SiO_2$ channels can be prepared. The nanoscale $SiO_2$ patterns can also be created on the surface of three-dimensional (3D) $SiO_2$ substrate and even the nanoscale trenches can be constructed with arbitrary shapes. A possible mechanism for this enhanced etching of $SiO_2$ has been qualitatively analysed using defects in SWNTs, combined with $H_3O^+$ electric double layers around SWNTs in an HF solution.

**Keywords:** carbon nanotube, silicon dioxide, HF wet etching, defects and electric double layers

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## 1. Introduction

New techniques for fabricating nanometer-scale structures have become critically important for advances in nanoscience and technology.[1−6] Conventional photolithography is approaching its limit and cannot meet the resolution requirements for nanodevices in the near future.[7] Therefore, new alternative techniques for nanocscale fabrication are always attractive.[4−6] In the last few years, new nanostructures have included single-walled carbon nanotubes (SWNTs) and aligned SWNT arrays.[8−10] Considering the nanosized structure of SWNTs, it is a promising route to make use of SWNTs for nanofabrication. It has been reported that multi-walled carbon nanotubes can be used as a reactive ion etch mask for nanofabrication on silicon substrates[11] and SWNTs can serve as a template for performing polymer imprint lithography to produce nanometer-size patterns.[12] In view of the importance of silicon dioxide lithography in developing nanoelectronic devices, how to realize the nanofabrication of silicon dioxide by using SWNTs is an important issue. It has been reported that with some oxygen and iron catalyst nanoparticles, the carbon nanotubes by reducing the silicon dioxide at 900 °C can produce nanotrenches on the substrate.[13] Recently, Liu *et al.* demonstrated a method to etch nanoscale trenches on silicon dioxide using carbon nanotubes in an alkaline solution at 50 °C for several hours. They suggested a concept to explain the etching, i.e., there is an electric double layer around carbon nanotubes that can increase the local $OH^-$ concentration near SWNTs.[14] Here we present a new method to create nanoscale $SiO_2$ pits or channels using SWNTs in an HF solution at room temperature in a very short time. A pattern of nanoscale $SiO_2$ channels on a planar substrate surface can be prepared using aligned SWNTs arrays. In addition, based on the same technique, the nanoscale $SiO_2$ patterns can also be created on the surface of three-dimensional (3D) $SiO_2$ and even create nanoscale trenches with arbitrary shapes. A possi-

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ble mechanism for enhanced etching is proposed using defects on SWNTs, combined with the electric double layers around SWNTs.

## 2. Experiment

Random SWNT networks or horizontally aligned SWNT arrays were grown by chemical vapour deposition (CVD)[15,16] on a 400-nm-thick silicon dioxide layer. The samples were firstly degassed at 150 °C for about 1 hour under high vacuum ($10^{-3}$ Pa–$10^{-4}$ Pa). Two approaches were found to achieve the nanoscale patterns, as shown in Fig. 1. One method is that the sample was directly etched in the HF aqueous solution (HF:$H_2O$=1:10) for several minutes at room temperature and then rinsed in deionized water. Another method is that a thin layer of $SiO_2$ (e.g., 30 nm) was deposited on SWNTs before etching in HF solution. The main purpose of this step is to introduce a larger amount of defects in the SWNTs. The deposition of 30-nm $SiO_2$ was performed by radio-frequency magnetron sputtering with a power of 100 W in Ar and $O_2$ atmospheres at 2 mTorr (1 Torr = $1.33322 \times 10^2$ Pa). The morphologies of the $SiO_2$ surface was studied by atomic force microscope (AFM, DI: MultiMode Nanoscope IIIa).

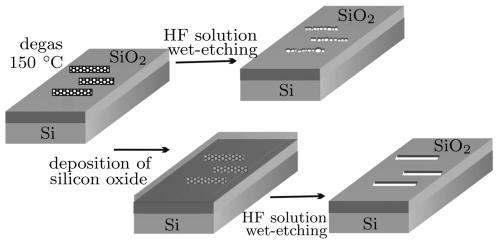



**Fig. 1.** Schematic diagram of the formation of nanoscale pits (top) and channels (bottom) guided by the SWNTs.

## 3. Results and discussion

After degassing, the SWNT sample was directly etched in HF solution. It was observed that the nanoscale pits lined up on $SiO_2$, as shown in Fig. 2(a), while the SWNTs were released from the surface of $SiO_2$ during etching. The average spacing of those pits is only about several tens of nanometer. A close-up of the pits is shown in Fig. 2(b). The depth of a pit is about 3.4 nm and the diameter is less than 50 nm, (Fig. 2(c)).

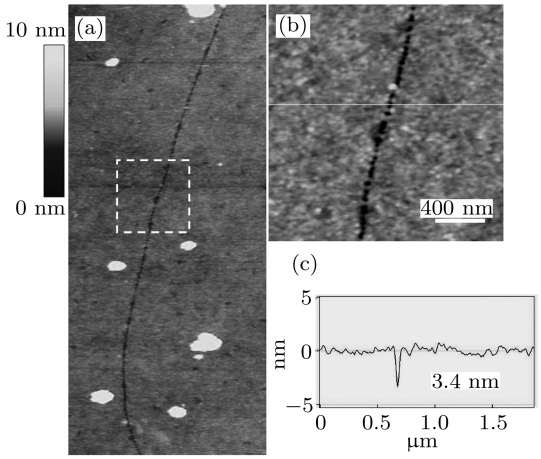



**Fig. 2.** AFM images of the pits on the $SiO_2$ guided by an individual SWNT after enhanced etching in HF solution. (a) Low-resolution image of the pits; (b) close-up image of the area denoted by the white box in panel (a); (c) cross-sectional profile of a pit taken from the white line in panel (b).

It is obvious that there is a higher etching rate underneath nanotubes where the pits appeared. In water, the HF molecules are reversibly electrolyzed as follows:

$$2HF + H_2O \leftrightarrow H_3O^+ + HF_2^-. \quad (1)$$

When the $HF_2^-$ ions meet silicon dioxide, the following reaction happens:

$$3HF_2^- + SiO_2 + 3H_3O^+ \rightarrow H_2SiF_6 + 5H_2O. \quad (2)$$

As reported, either OH– or $H_3O^+$ ions in the solution can be adsorbed on the graphene surface.[17] We thus inferred that $H_3O^+$ dissociated in HF solution would be adsorbed by the hydrophobic SWNTs to form an electrical double-layer. The adsorbed $OH^-$ would form a more ordered structure at the graphene-water interface than that of $H_3O^+$ does.[17] Although nanoscale $SiO_2$ trenches can be formed in a strong alkaline solution,[14] as shown by the following experiments, it is difficult to etch $SiO_2$ in an HF solution by SWNTs solely with the help of the electrical double-layer. The contribution of defects in SWNTs should be taken into account to explain the enhanced etching of $SiO_2$. These defects in SWNTs may speed the rate of the electrochemical reaction.[18−20] From Fig. 2(b), the average distance between two adjacent pits is about 40 nm ∼ 60 nm, which is in qualitative agreement with the defect density in as-grown carbon nanotubes.[21] Accordingly, we speculated that these discontinuous nanoscale pits may result from the defects in SWNTs, together with the effect of the electrical double-layer. The defects in SWNTs

will enhance the effects of the electrical double-layer around SWNTs. The extrinsic defects in SWNTs induced by argon irradiation can increase the double-layer capacitance.[22] If we introduced more defects into SWNTs, continuous nanoscale grooves can be achieved.

To verify this idea, we created defects by depositing silicon dioxide on SWNTs by magnetron sputtering. The sputtering of $SiO_2$ will produce a lot of defects in SWNTs since the $SiO_2$ particles in magnetron sputtering have about 100 times more energy than that produced by thermal evaporation.[23] As reported recently by Dimiev *et al.*, a large amount of defects can be introduced into graphenes by sputtering a thin layer of metal.[23] The sputtering of silicon dioxide on SWNTs is more convenient for the following etching process. As we expected, the continuous nanoscale trenches network formed on the $SiO_2$ guided by SWNTs after etching for 90 seconds (Fig. 3(a)). Such trenches appear as dark lines in AFM images, the different contrast of the trenches may be correlated with the thicknesses of the corresponding SWNTs. In Fig. 3(b), we observe an SWNT left in the bottom of a trench with a depth of about 8 nm. It is believed that as long as the SWNTs remain in the trench, the depth of the $SiO_2$ nanotrench would increase until the $SiO_2$ is completely etched. However, if we extended the time of etching, it was found that the depth almost remain unchanged. This is because the SWNTs are easy to be released from the $SiO_2$ surface during the etching process.

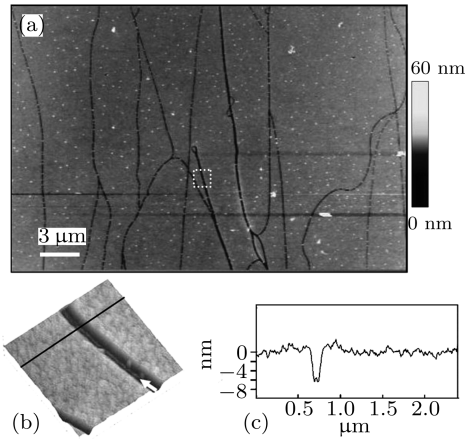



**Fig. 3.** Formation of nanoscale trenches guided by SWNTs after being sputtered on $SiO_2$. (a) AFM image of a nanotrench pattern; (b) enlarged AFM image of a trench from the square area included by dashed lines in panel (a). In this nanotrench, an SWNT is clearly visible as marked by a white arrow; (c) cross-sectional profile taken from the black line in panel (b).

For the $SiO_2$ channels, a key parameter is the resolution of these channels, which depends on the width of the channel. In our work, the width of individual channel in the opening is about 100 nm, so the resolution between channels is also about 100 nm. The distance between two carbon nanotubes in our sample is usually above 1 μm, so now we cannot achieve the minimum distance between two channels. To decrease the distance between two channels, a possible method is to produce the ultra-high density well-aligned carbon nanotube array.[24,25]

The correlation between the depth of trenches and the diameter of the SWNT was further investigated. Four SWNTs were positioned by scanning electron microscopy (SEM), as marked in Fig. 4(a) by numbers 1, 2, 3, and 4, respectively. The diameters of these SWNTs are shown in Fig. 4(b). The trenches corresponding to these four SWNTs were created after etching for 1 minute, as shown in Fig. 4(c). The depth of each trench was measured by AFM (Fig. 4(d)). It is clear that the larger the diameter of SWNT, the deeper the trench. The diameter of SWNTs also plays an important role in the effect of enhanced etching.

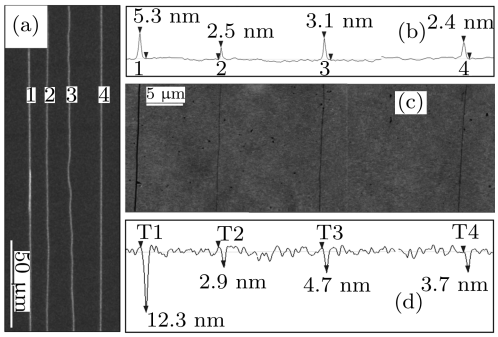



**Fig. 4.** The correlation between the depth of trenches and the diameter of the SWNT. (a) An SEM image with four SWNTs marked by the numbers; (b) AFM profile of the same nanotubes as marked in (a), where the values are the measured diameters of the nanotubes; (c) AFM image displaying four trenches marked by T1, T2, T3, and T4; (d) AFM profile of the trenches with measured depth values as marked.

Future microelectronic package schemes and micro-systems may require patterning fine features on grossly non-planar substrates. As we know, it is difficult in conventional lithography to achieve patterns on 3D substrates. Surprisingly, patterning on 3D substrates can be also realized using our methods. The trenches formed on the $SiO_2$/Si substrates, no matter how the surface morphology changed during the etching. Figure 5 shows three trenches along stepped

surfaces marked by $S_1$, $S_2$, $S_3$, $S_4$, and $S_5$, as shown in Fig. 5(a). The trenches extended continuously across the whole stepped surface. A cross-sectional profile of the stepped surface is shown in Fig. 5(b), indicating heights of the steps that the trenches crossed. With the etching process further continued, the trenches will disappear on the bottom surface, as seen in Fig. 5(c), where the $SiO_2$ was completely removed and the silicon substrate emerged. This phenomenon shows again that the nanoscale $SiO_2$ patterns can be created on the surface of 3D non-planar $SiO_2$.

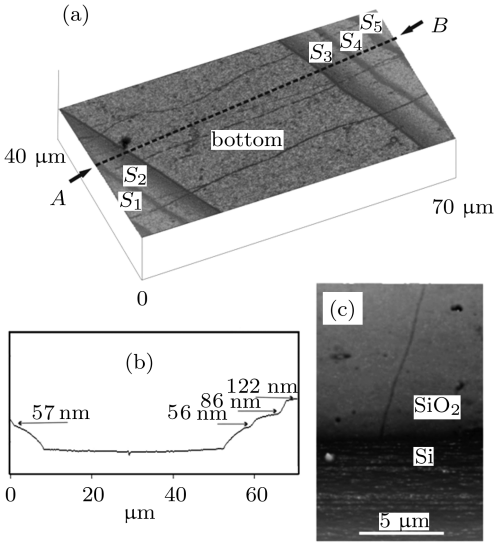



**Fig. 5.** Nanotrenches formed on a non-planar surface. (a) Trenches extending continuously across steps marked by $S_1$, $S_2$, $S_3$, $S_4$, and $S_5$. (b) cross-sectional profile of the stepped surface along the direction from $A$ to $B$, as indicated in panel (a). The values indicate the heights of the locations denoted by the arrows; (c) a trench disappears on the bottom where the $SiO_2$ is completely etched.

The designed shape of channels is critical for applications in nanoelectronics. In this work, we make sure that the channels were fully guided by the carbon nanotubes. Theoretically, an arbitrary shape of channels can be created if the shape of carbon nanotube can be controlled. We conducted preliminary tests to control the shape of an individual carbon nabotube. As an example, we firstly push an SWNT using AFM probe and make it curved, as shown in Fig. 6(b). The sample was then dipped in the HF aqueous solution. After etching, a curved nanotrench formed along this SWNT. This experiment also ruled out the possible impacts of chemical bonding or contaminations between SWNTs and the silicon dioxide surface since the trench can be still formed even though the SWNT has been pushed away from its original position [Figs. 6(b) and 6(c)]. To obtain a complicated designed shape, we think it would be better to control the shape of the carbon nanotube by a suitable design of growth process or transfer–printing technique.[24]

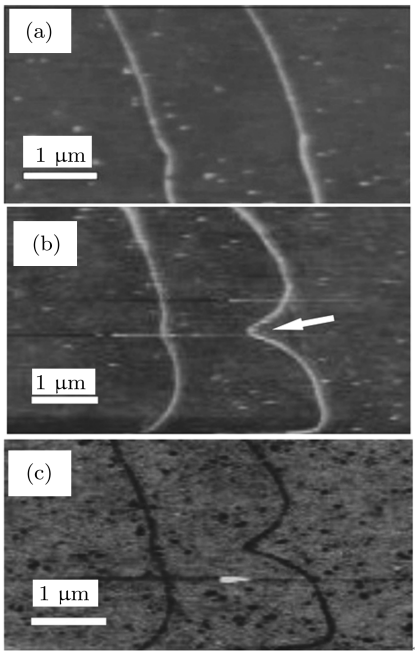



**Fig. 6.** Nanoscale trenches with arbitrary shapes. (a) Two parallel SWNTs on the $SiO_2$; (b) AFM image of curved SWNTs formed by AFM tip; (c) the curved trenches guided by the SWNTs.

## 4. Conclusion

We present a promising method to create nanoscale $SiO_2$ pits or channels using SWNTs in an HF solution at room temperature within a few seconds. A pattern of nanoscale $SiO_2$ channels on a planar substrate surface can be prepared using aligned SWNTs arrays. Employing the same technique, nanoscale $SiO_2$ patterns, and even nanoscale trenches with arbitrary shapes, can also be created on the surface of 3D $SiO_2$. A possible mechanism for enhanced etching of $SiO_2$ is proposed using defects on SWNTs, together with $H_3O^+$ electric double layers around SWNTs in an HF solution. Our technologies for nanocscale fabrication will have important applications in nanoelectronics. Both the phenomena and the possible mechanism involved in these technologies will arouse theoretical interest.

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