Partial-SOI high voltage P-channel LDMOS with interface accumulation holes*

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A new partial SOI (silion-on-insulator) (PSOI) high voltage P-channel LDMOS (lateral double-diffused metal-oxide semiconductor) with an interface hole islands (HI) layer is proposed and its breakdown characteristics are investigated theoretically. A high concentration of charges accumulate on the interface, whose density changes with the negative drain voltage, which increase the electric field ($E_{\rm I}$) in the dielectric buried oxide layer (BOX) and modulate the electric field in drift region . This results in the enhancement of the breakdown voltage (BV). The values of $E_{\rm I}$ and BV of an HI PSOI with a 2-μm thick SOI layer over a 1-μm thick buried layer are 580V/μm and −582 V, respectively, compared with 81.5 V/μm and −123 V of a conventional PSOI. Furthermore, the Si window also alleviates the self-heating effect (SHE). Moreover, in comparison with the conventional device, the proposed device exhibits low on-resistance.

Keywords: interface charges, breakdown voltage, partial-SOI, accumulation holes, self-heating effect

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1. Introduction

P-channel LDMOS (lateral double-diffused MOSFET) with a high breakdown voltage in both off- and on-states are widely employed in level shifters for multioutput driving circuits such as those for display panels and motor drivers.[1−5] This is because an HV P-channel LDMOS in p-SOI suffers from a low vertical breakdown voltage ($V_{\rm B,V}$) and the self-heating effect (SHE). The former problem can be solved by enhancing the electric field of the buried layer with the ENDIF (enhanced dielectric layer field) rule,[6−13] in which introducing interface charges to increase $E_{\rm I}$ is one of the most effective methods. Moreover, partial-SOI (PSOI) technology can increase BV and reduce SHE due to its Si window.[14−16]

In this paper, a new high voltage P-channel LDMOS on partial-SOI is proposed and its breakdown characteristics are discussed. The value of $B_{\rm B,V}$ is improved because of the enhancement of $E_{\rm I}$ as well as the modulation effects of the Si window on the electric field in the SOI layer. The SHE and $R_{\rm on}$ in HI PSOI are investigated as well.

2. Structure and mechanism

A field plate, a field limiting ring and a reduced surface field (RESURF) are adopted to optimize the lateral BV, its BV lies on its vertical BV ($V_{\rm B,V}$) and is composed of $V_{\rm S}$, $V_{\rm I}$ and $V_{\rm sub}$, which are the voltages shared by the top Si, the buried dielectric oxide and the substrate layers, respectively. By making use of $\varepsilon_{\rm I}E_{\rm I} = \varepsilon_{\rm S}E_{\rm S} + Q_{\rm in}$ on the interface of the dielectric oxide buried layers $E_{\rm I}$ of SOI/PSOI can be written as[17]

$$E_{\rm I} = \left[V_{\rm d} - V_{\rm sub} + \frac{t_{\rm s}q\sigma_{\rm in}}{2\varepsilon_{\rm s}}\right]\frac{\varepsilon_{\rm S}}{\varepsilon_{\rm I}t}, \tag{1}$$

$$E_{\rm S} = \left[V_{\rm d} - V_{\rm sub} + \frac{t_{\rm I}q\sigma_{\rm in}}{\varepsilon_{\rm I}}\right]\frac{1}{t}, \tag{2}$$

where $E_{\rm S}$ is the electric field of Si on the interface, $\sigma_{\rm in}$ is accumulation charge density on the interface, $\varepsilon_{\rm S}$ and $\varepsilon_{\rm I}$ are the permittivities of Si and the dielectric buried layer, $V_{\rm d}$ and $V_{\rm sub}$ are negative drain and

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substrate voltage, and $t = 0.5t_{\rm S} + \varepsilon_{\rm S}t_I/\varepsilon_{\rm I}$ is defined as the characteristic thickness of SOI, respectively. From Eqs. (1) and (2), the BV of PSOI is obtained as

$$BV = V_{\rm B,V} = E_{\rm S}t + \frac{q\sigma_{\rm in}t_{\rm I}}{\varepsilon_{\rm I}} + V_{\rm sub}. \quad (3)$$

As regards the p-type drift region (the high electric potential), the dielectric buried layer and the substrate (the low electric potential), as an MIS-like structure, and $\sigma_{\rm in}$ has the expression as

$$\sigma_{\rm in} = \sqrt{\frac{2\varepsilon_{\rm S}k_0Tp_{\rm n0}}{q^2}\exp\left(\frac{q(V_{\rm d} - V_{\rm sub} - \varphi_{\rm S})}{k_0T}\right)}, \quad (4)$$

where $p_{\rm n0} = n_{\rm i}^2/N_{\rm d}$ is the equilibrium minor carrier concentration of the drift region, $N_{\rm d}$ is the impurity concentration in the drift region and k_0, T, $n_{\rm i}$, and $\phi_{\rm S}$ are the Boltzmann constant, the absolute temperature ($T = 300$ K at room temperature), the intrinsic carrier concentration of Si and the surface potential on the interface of top Si layer and dielectric buried layer, respectively.[18] From Eq. (3), $\sigma_{\rm in}$ increases exponentially with $\phi_{\rm S}$ and should effectively enhance $E_{\rm I}$ and the BV as shown by Eqs. (1) and (2). Each addition of $\sigma_{\rm in}$ to 1×10^{12} cm^{-2} can enhance $E_{\rm I}$ of 46.4 V/μm. In the conventional PSOI, however, $\sigma_{\rm in}$ cannot be fixed because the extraction of the lateral electric field is actually ignored.

The cross section of the proposed HI PSOI LDMOS is illustrated in Fig. 1. A positive charge (holes) layer is made on the interface of the top Si layer and dielectric buried layer (SiO_2) in which equidistant high concentration n$^+$-regions (an HI cell has been shown in Fig. 1) are made, and there is a drain-Si window; $N_{\rm n+}$, $N_{\rm d}$, and $N_{\rm sub}$ are impurity concentrations in the interface n$^+$-regions, the drift region and the substrate layer, respectively. D, W, $L_{\rm d}$, and $L_{\rm W}$ are the lengths of the n$^+$-regions, the spacing of the two neighboring n$^+$-regions, the drift region and the Si window, respectively. $t_{\rm S}$, $t_{\rm I}$, $t_{\rm sub}$, and H are the thicknesses of the top Si, the dielectric oxide buried, the substrate layer and the n$^+$-regions, respectively.

Figure 1 shows that when a high negative voltage $V_{\rm d}$ is applied to the drain and substrate while the source and gate are grounded, the accumulated holes form islands in the spacing of a series of n$^+$-regions by compositive operation of the vertical, lateral electric field and Coulomb's forces. From Eqs. (1) and (2), the accumulated holes can enhance $E_{\rm I}$ from the conventional $\varepsilon_{\rm S}E_{\rm S}/\varepsilon_{\rm I} \approx 3E_{\rm S}$ to $(\varepsilon_{\rm S}E_{\rm S} + q\sigma_{\rm in})/\varepsilon_{\rm I}$ (the increment of $E_{\rm I}$ is $E_{\rm I} = q\sigma_{\rm in}/\varepsilon_{\rm I}$ as shown in Fig. 1) and therefore increase BV, shielding the Si layer $E_{\rm S}$ from a high electric field and avoiding Si layer premature breakdown. A Si window makes the substrate share voltage and modulates the electric field in the drift region. Moreover, it offers a heat conduction path. Both of the above result in a high BV and a low SHE for the HI PSOI.

In Refs. [16] and [17], the authors used dielectric trenches to prevent the extraction of holes by the lateral electric field. However, the island charges (holes) of HI PSOI are accumulated by the compositive operation of the electric field and the Coulomb forces. The fabrication process of HI PSOI is fully compatible with conventional CMOS/SOI technology, except for the arsenic implantation to form n$^+$-regions before twice bonding.

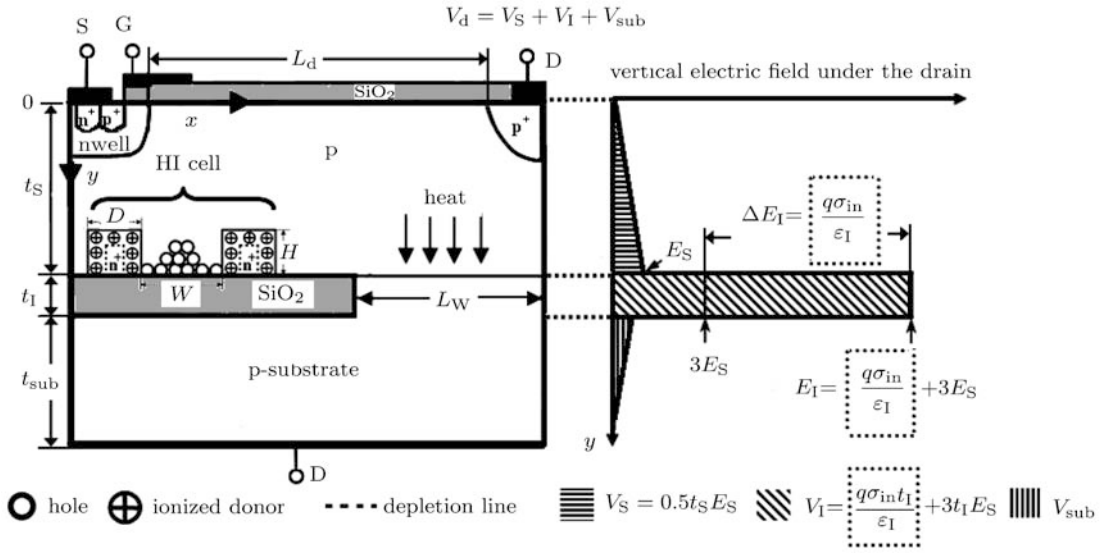


Fig. 1. Device structure with its mechanism and vertical electric field distribution under the source of an HI PSOI LDMOS.

3. Results and discussion

A two-dimensional device simulation[19] is employed to investigate the operation of the proposed HI PSOI LDMOS, the comparisons with conventional PSOI and SOI LDMOS are specified in Table 1.

Table 1. Device parameters used in the simulation.

Device parameters	HI PSOI	Con. PSOI	Con. SOI
Drift length, $L_{\rm d}$	30 μm–150 μm	30 μm–150 μm	30 μm–150 μm
Thickness of SOI layer, $t_{\rm S}$	2 μm	2 μm	2 μm
Thickness of buried layer, $t_{\rm I}$	1 μm	1 μm	1 μm
Thickness of p-substrate layer, $t_{\rm sub}$	30 μm	30 μm	30 μm
p-substrate concentration, $N_{\rm sub}$	(1∼10)×10^{14} cm^{-3}	(1∼10)×10^{14} cm^{-3}	(1∼10)×10^{14} cm^{-3}
Thickness of HI layer, H	0∼1.2 μm	–	
n^+-region length in HI layer, D	0∼2 μm	–	
Spacing of two neighbouring n^+-regions in the HI layer, W	1∼3.5 μm	–	
n^+-region concentration in HI layer, $N_{\rm n+}$	1×10^{19} cm^{-3}	–	

The hole distribution in the HI PSOI at breakdown with $t_{\rm S} = 2$ μm, $t_{\rm I} = 1$ μm, $t_{\rm sub} = 30$ μm, $L_{\rm d} = 80$ μm, $D = H = 0.5$ μm, $W = 2$ μm, $L_{\rm W} = 15$ μm, $N_{\rm d} = 5.5 \times 10^{15}$ cm^{-3}, $N_{\rm n+} = 1 \times 10^{19}$ cm^{-3}, and $N_{\rm sub} = 2 \times 10^{14}$ cm^{-3} is shown in Fig. 2. The hole concentration at the source is over 10^{18} cm^{-3} and is shown in Fig. 2(a), and holes are only located on the interface, whose density increases linearly and self-adaptively. The insert is the hole distribution in the HI cell under the source and the highest hole concentration occurs at the middle of the two neighboring n^+-regions because of the maximal Coulomb forces. Figure 2(b) gives the holes distribution in the HI cell under the source with different interface thicknesses and it is obvious that the accumulation layer is about 180 nm. From Eqs. (1) and (2), the interface hole accumulation should effectively enhance $E_{\rm I}$, weaken $E_{\rm S}$ and increase BV.

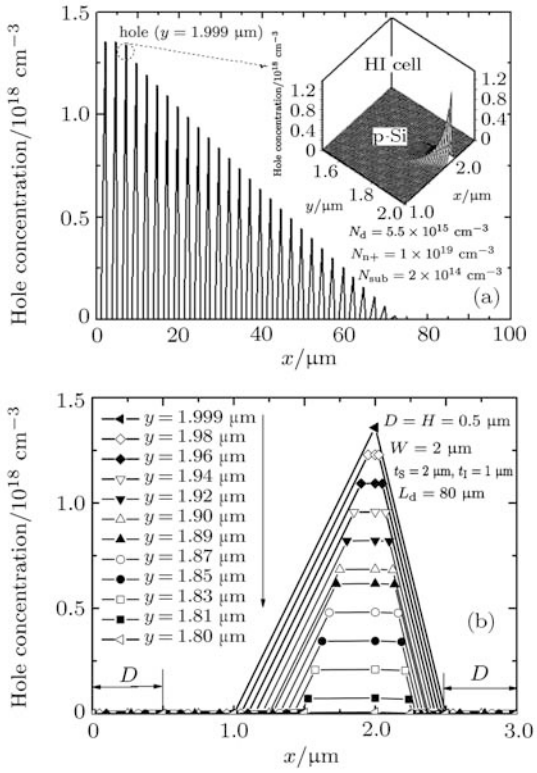


Fig. 2. Hole distribution in the HI PSOI LDMOS at breakdown ($t_{\rm S}$ = 2 μm, $t_{\rm I}$ = 1 μm, $t_{\rm sub}$ = 30 μm, $L_{\rm d}$ = 80 μm, $D = H$ = 0.5 μm, W = 2 μm, $L_{\rm W}$ = 15 μm, $N_{\rm d} = 5.5\times10^{15}$ cm^{-3}, $N_{\rm n+} = 1\times10^{19}$ cm^{-3}, and $N_{\rm sub} = 2\times10^{14}$ cm^{-3}). (a) Interface hole distribution. Inset is the hole distribution in the HI cell under the source. (b) Hole distribution in the HI cell under the source with different vertical distances.

The electric potentials and fields distributions at breakdown for the HI PSOI and the conventional PSOI are illustrated in Fig. 3. Figure 3(a) shows the surface potentials for the two structures. The surface potential of the HI PSOI increases almost linearly, then maintains a high potential in the whole drift region from the source to the drain, however, that of the conventional PSOI is concentrated in the source. This means that the electric field in the drift region is effectively modulated by the interface holes as shown in Fig. 2 for the HI PSOI, which can be seen obviously from the uniform equipotential contours of HI PSOI in comparison with that of the conventional PSOI concentrated on the head of the drift region in the insert of Fig. 3(a). Figure 3(b) shows the vertical electric fields and potential distributions for the two structures. It can be seen that $E_{\rm I}$ of HI PSOI increases from about 81.5 V/μm of the conventional PSOI to 580 V/μm due to the enhancement effect of the accumulation charges ($\Delta E_{\rm I}$ = 498.5 V/μm). Moreover, accumulation charges reduce the Si layer electric field on the

interface to 1.2 V/μm and completely shields the Si layer. In simulation by MEDICI, the BV of −582 V for HI PSOI compared to −123 V and −123 V for the conventional PSOI and SOI, respectively. For the HI PSOI structure, above 95 % of the BV is shared by the dielectric buried layer ($V_{\rm I} = t_{\rm I}E_{\rm I} = -580$ V) shown in Fig. 3(b). It can be concluded that the interface holes can assuredly enhance $E_{\rm I}$, shield the Si layer and increase BV.

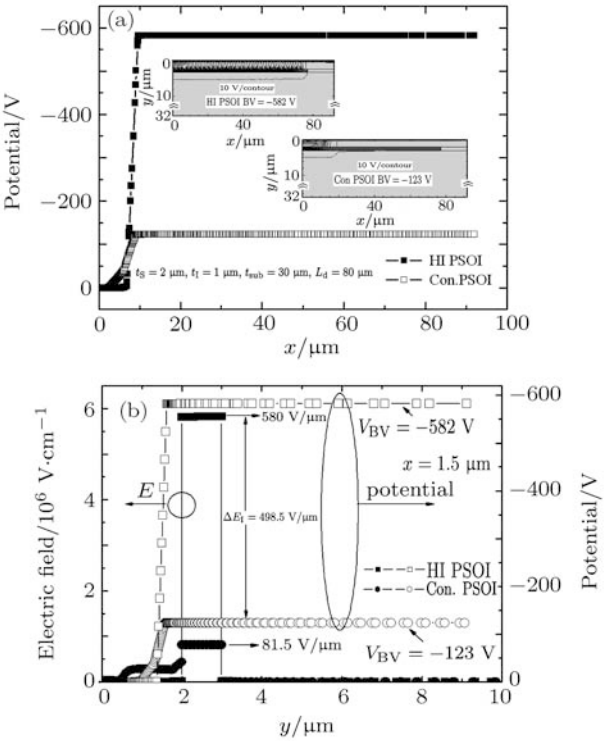


Fig. 3. Electric fields and potential distributions at breakdown for the HI PSOI, the conventional PSOI $t_{\rm S}$ = 2 μm, $t_{\rm I}$ = 1 μm, $t_{\rm sub}$ = 30 μm, $L_{\rm d}$ = 80 μm, and $N_{\rm sub}$ = 2×10^{14} cm^{-3} for all. $N_{\rm d}$ is 5.5×10^{15} cm^{-3}, 1×10^{15} cm^{-3} for the two structures, $L_{\rm W}$ = 15 μm for PSOI. $D = H$ = 0.5 μm and W = 2 μm for the HI PSOI. (a) Surface potential (y = 0.001 μm) distributions. The inset shows the equipotential contour distributions of the HI PSOI and the conventional PSOI. (b) Vertical electric fields and potential distributions under the source (x = 1.5 μm).

Figure 4 demonstrates the relationship of the interface $E_{\rm S}$ (y = 1.999 μm) and $E_{\rm I}$ (y = 2.001 μm), the hole concentrations and surface potential $\phi_{\rm S}$ (y = 1.999 μm) in the HI cell under the source with $V_{\rm d}$. Figure 4 shows that the self-adaptive holes and the surface potential gradually increase with $V_{\rm d}$, which induces a sustaining enhancement of $E_{\rm I}$ and, simultaneously, $E_{\rm S}$ is less than 10 V/μm, until the high BV reaches −582 V. However, because of the lack of interface charges, $E_{\rm I}$ of the conventional PSOI is always limited by the formula of $E_{\rm I} = 3E_{\rm S}$ from Eq. (1) and Fig. 1, and $E_{\rm S}$ rapidly reaches the Si critical electric field (30 V/μm) when BV is −123 V. Hole islands can enhance $E_{\rm I}$ and weaken $E_{\rm I}$, self-adaptive change simultaneously.

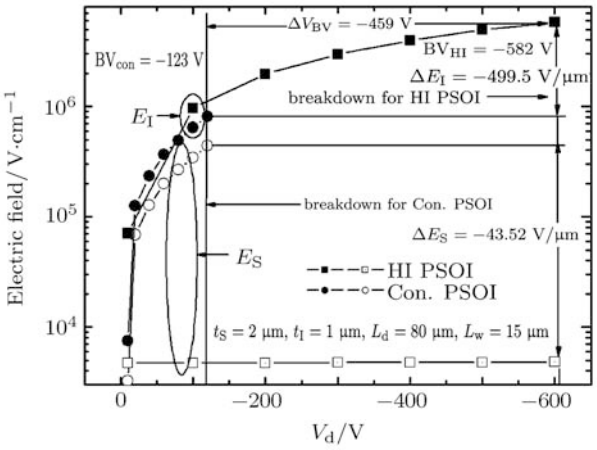


Fig. 4. Dependences of the interface electric fields of silicon layer (y = 1.999 μm) and dielectric buried layer (y = 2.001 μm), the hole concentrations and surface potential $\phi_{\rm S}$ (y = 1.999 μm) in the HI cell under the source on the applied voltage $V_{\rm d}$. The device parameters are the same as those in Fig. 3 and x = 1.5 μm for all.

Figure 5 gives the dependence of voltages and hole concentrations on Si window length $L_{\rm W}$ under the source for HI PSOI. For HI PSOI, although $V_{\rm sub}$ slowly increases because the depletion layer extends into the substrate, BV decreases with the increase of $L_{\rm W}$ as shown in Fig. 5, the number of the islands and $Q_{\rm in}$ reduce with an increase of $L_{\rm W}$, resulting in the falls of $E_{\rm I}$ and $V_{\rm I}$. From Fig. 1 and Eqs. (1) and (2), the enhancement of BV by interface charges $\Delta V(\sigma_{\rm in})$ for HI PSOI can be derived as

$$V(\sigma_{\rm in}) = V_{\rm I} - 3t_{\rm I}E_{\rm S}.$$

$V(\sigma_{\rm in})$ is about 99% of $V_{\rm I}$ for all the $L_{\rm W}$ from 0 to 50 μm whereas the percentage of $V(\sigma_{\rm in})$ for BV decreases with the fall of $L_{\rm W}$, and $\Delta V(\sigma_{\rm in})$/BV is above 90% at $L_{\rm W}$ = 15 μm.

In order to obtain a maximum BV$_{\rm max}$, the total charges in the drift region should satisfy the RESURF principle. Figure 6 shows the influences of different structural parameters on BV with a constant $L_{\rm W}$ of 15 μm. It can be seen from Fig. 6 that there is a a maximum BV=−582 V with $D = H$ = 0.5 μm and W = 2 μm. Comparing parameters H, W, and D, the influence of H on BV$_{\rm max}$ is more distinct. The maximal BV increases with the increasing $L_{\rm d}$. When D or H is 0 μm, the HI PSOI becomes a conventional

PSOI (BV=−123 V).

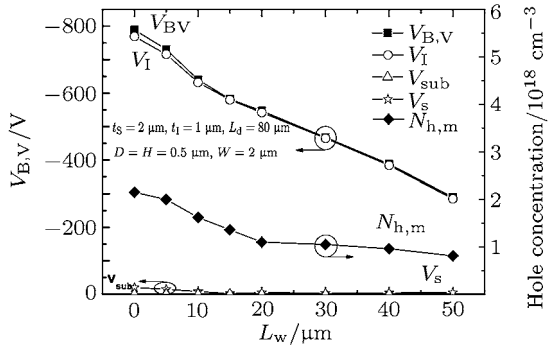


Fig. 5. Influences of silicon window length L_W on voltage and hole concentration under the source. The device parameters are the same as those in Fig. 3 except L_W.

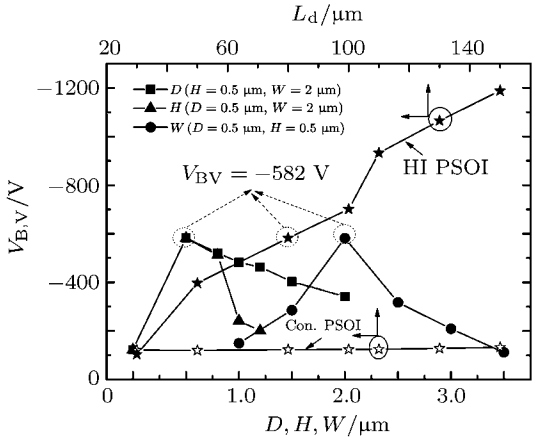


Fig. 6. Influences of device parameters on breakdown voltage with a constant L_W of 15 μm (t_S = 2 μm, t_I = 1 μm, t_{sub} = 30 μm for all. L_d = 80 μm for D, H and W. $D = H$ = 0.5 μm and W = 2 μm for L_d. $N_{sub} = 2\times10^{14}$ cm^{-3} for all.)

Figure 7 gives the surface temperature and three-dimensional temperature profile of the three devices as a function of V_g and V_s in the on-sate condition. The substrate temperature is 300 K and the gate voltage (V_g) is −20 V for all simulations. At the power of 1 MW/μm, with a V_s of 60 V, the drain surface temperature of HI PSOI is the lowest, whose maximal temperature T_{max} is 315.72 K, but that of the conventional SOI is the highest whose T_{max} is 315.78 K. Moreover, T_{max} conventional SOI and conventional PSOI are situated under the source, whereas HI SOI is the middle part of the structure, which is very clear in Figs. 7(b) and 7(c). The proposed HI PSOI has a higher BV and a lower SHE from the above simulations.

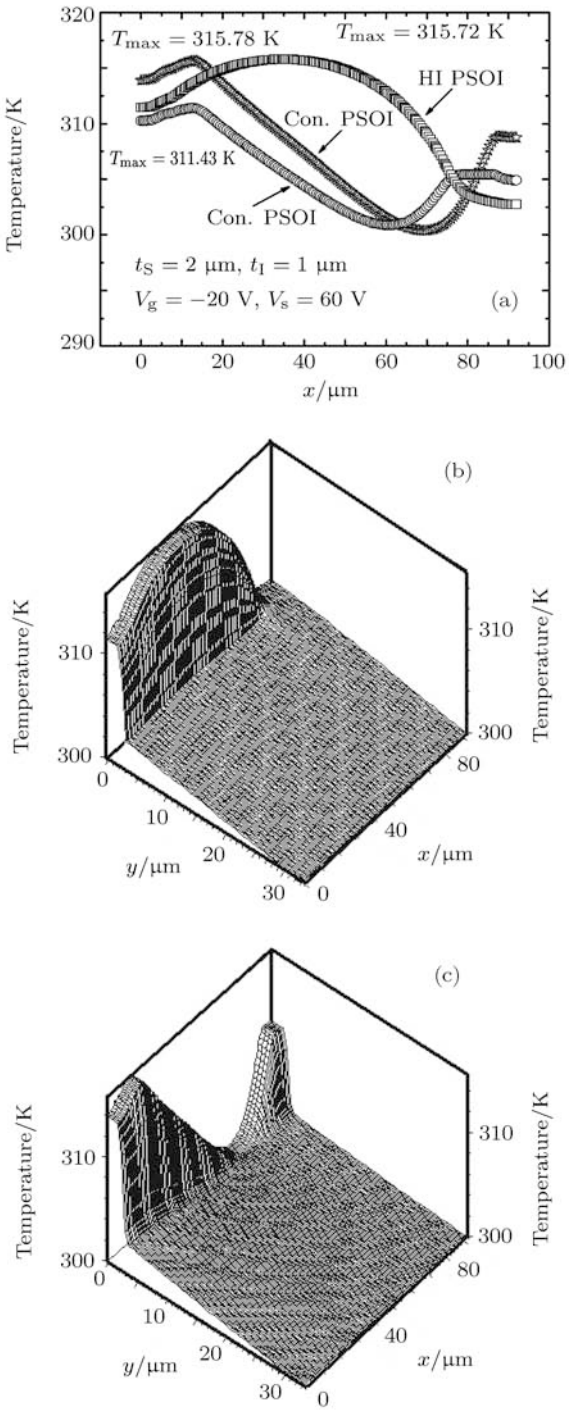


Fig. 7. Thermal characteristics with V_s = 60 V and V_g = −20 V. The device parameters are the same as those in Fig. 3. (a) Surface temperature profiles (y = 0.001 μm) of the HI PSOI, the conventional PSOI and SOI. (b) Three-dimensional temperature profiles of the HI PSOI. (c) Three-dimensional temperature profiles of the conventional SOI.

The on-state characteristics between the HI PSOI and the conventional PSOI have been compared. The simulation results are shown in Fig. 8 and tabulated in Table 1. It is clear that the HI PSOI has an superior current handing capability. The simulated HI

PSOI has a R_{on} of 2.65 Ω·mm^2 at $V_{gs} = -20$ V, $V_{ds} = -20$ V while the corresponding values in the conventional PSOI are 6.7 Ω·mm^{2}for the same bias. It is calculated to be 60.4% lower compared to that of its counterpart. The improvement in the on-state characteristics must be due to the fact that higher concentration n+-implanted layer implemented in the drift region results in the heavy dopant in the drift region, which reduces the on-resistance of the HI PSOI.

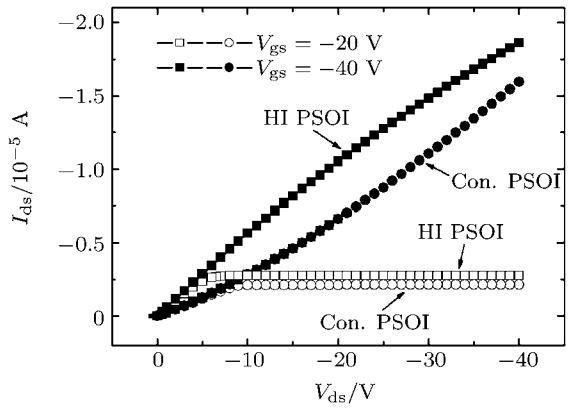


Fig. 8. On-state characteristics of the HI PSOI and conventional PSOI; the threshold voltage (V_{th}) for both devices is −16 V.

Table 2. DC performance comparison between the HI PSOI and conventional PSOI.

Device		$V_{B,V}$/V	R_{on}/Ω·mm^2
HI PSOI	$V_{gs} = -40$ V	−582	2
	$V_{gs} = -20$ V		2.65
Conventional PSOI	$V_{gs} = -40$ V	−123	3
	$V_{gs} = -20$ V		6.7

4. Conclusion

A novel P-channel interface hole island (HI) structure of a PSOI HV device is proposed in this paper. HI PSOI provides a new method to accumulate the interface holes, whose physical mechanism is analysed in detail. HI PSOI effectively utilizes the accumulated interface holes to enhance the electric field of the buried dielectric and stimulate the electric field of the top silicon layer and so increase BV while alleviating the SHE by a silicon window under the drain, and R_{on} is reduced by 60.4% compared with those of a conventional PSOI LDMOS. HI PSOI is a potential device for applications in high voltage and power integrated circuits due to their favourable performances and easy fabrication.

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