Analytical base–collector depletion capacitance in vertical SiGe heterojunction bipolar transistors fabricated on CMOS-compatible silicon on insulator*

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The base–collector depletion capacitance for vertical SiGe npn heterojunction bipolar transistors (HBTs) on silicon on insulator (SOI) is split into vertical and lateral parts. This paper proposes a novel analytical depletion capacitance model of this structure for the first time. A large discrepancy is predicted when the present model is compared with the conventional depletion model, and it is shown that the capacitance decreases with the increase of the reverse collector–base bias–and shows a kink as the reverse collector–base bias reaches the effective vertical punch-through voltage while the voltage differs with the collector doping concentrations, which is consistent with measurement results. The model can be employed for a fast evaluation of the depletion capacitance of an SOI SiGe HBT and has useful applications on the design and simulation of high performance SiGe circuits and devices.

Keywords: depletion capacitance, heterojunction bipolar transistors, thin film silicon on insulator, SiGe

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1. Introduction

Silicon on insulator (SOI) schemes are increasingly employed due to the need for electrically insulating active devices from the substrate, leading to reduced parasitic capacitances, low leakage currents, and improved immunity to substrate noise and crosstalk.[1] Si/SiGe BiCMOS technology is widely used for low power, high speed applications such as 3G wireless circuits, millimeter radar, optical communications, and so on.[2] Combining SiGe heterojunction bipolar transistors (HBTs) with SOI technology, especially thin film SOI, is attractive but invalid due to the limited Si volume available for collector construction. However, a novel vertical SiGe HBT structure for a thin SOI substrate has been proposed by IBM group,[3] and successfully integrated with STMicroelectronics' 0.13 μm millimeter wave SOI BiCMOS technology in 2008.[4]

It has been thoroughly demonstrated that SiGe HBTs on thin SOI show vertical and horizontal space charge extension through experimental studies and simulations.[5,6] This phenomenon has been analysed qualitatively,[7] but quantitative modeling remains an issue. Hence an accurate prediction of the base–collector space charge region is needed. In this paper, a novel analytical model of the base–collector depletion capacitance including vertical and horizontal expansion of the base–collector space charge has been developed in order to accurately model SiGe HBTs on thin SOI. A large discrepancy is predicted when the present model is compared with the conventional depletion model, and it is shown that the capacitance decreases with the increase of the reverse collector–base bias, and shows a kink as the reverse collector–base bias reaches the effective vertical punch-through voltage while the voltage differs with the collector doping concentrations.

2. Model of the base–collector depletion capacitance

A schematic cross section of the device is shown in Fig. 1, where the symmetry of the structure has been used to limit the analysis to a half device, with a similar analysis for the other half. The zero point of x axis is located at the base side edge of the base–emitter depletion region at zero bias, and the zero point of y axis at the middle of the emitter. The $W_{\rm epi}$ and $L_{\rm epi}$ are the width and length of collector respectively, $W_{\rm B}$ and $L_{\rm B}$ are the width and length of base respectively, $W_{\rm E}$ is the width of the emitter.

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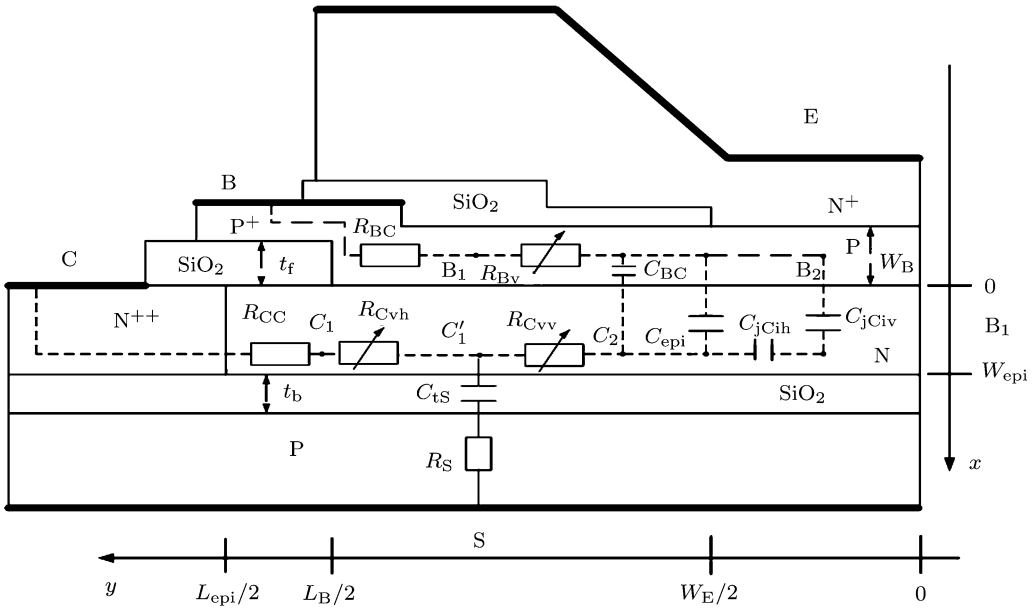


Fig. 1. Sketch of the HBT on thin SOI and associated collector simplified equivalent circuit.

The major differences between an HBT on bulk and an HBT on SOI are the collector thickness and the absence of a buried layer. The intrinsic collector space charge extension is lateral at $V_{\rm CB} = 0$ V for a fully depleted HBT, and vertical at $V_{\rm CB} = 0$ V while lateral at higher reverse bias for a partially depleted HBT where $V_{\rm CB}$ is the collector–base voltage. Electrons injected from the emitter flow vertically down in the collector and make a turn horizontally towards the n^+ reachthrough on the side. To model the two-dimensional space charge extension, the intrinsic base–collector junction vertical depletion capacitance $C_{\rm jCiv}$ and horizontal depletion capacitance $C_{\rm jCih}$ are introduced. Substrate capacitance $C_{\rm tS}$ and substrate resistance $R_{\rm S}$ model the SOI substrate. Other electrical parameters are the same as in the Mextram model,[8] $R_{\rm BC}$ and $R_{\rm CC}$ are the constant resistance at the external base and the collector, $R_{\rm Bv}$ and $R_{\rm Cv}$ are the low current resistance of the intrinsic base and the epilayer. The $C_{\rm BC}$ and $C_{\rm epi}$ are the collector region and the epilayer diffusion capacitance respectively.

2.1. Base–collector depletion width

It is noted that the variation of conduction band offset $\Delta E_{\rm c}$ with germanium content is minimal; the majority of the bandgap offset occurs in the valence band.[9] The conduction band offset can therefore be neglected for most practical purposes.

For a partially depleted collector, assume a flat dope in the epilayer and an abrupt base–collector junction for the derivation. In the case of partial depletion, the solution of the Poisson equation is classic:[10]

$$x = \sqrt{\frac{2\varepsilon_{\rm Si}(V_{\rm CiBi} + V_{\rm dc})}{qN_{\rm epi}}}, \tag{1}$$

where depletion and low injection approximations are made, the hole drift and diffusion currents, generation and recombination currents are ignored, the impurity atoms are assumed to be completely ionised, x is the depletion width, $\varepsilon_{\rm Si}$ is the dielectric coefficient of Si, $V_{\rm CiBi}$ is the intrinsic collector–base voltage, $N_{\rm epi}$ is the collector doping concentration, $V_{\rm dc} = V_{\rm T}\ln(N_{\rm epi}^2/n_{\rm i}^2)$ is the built in potential with $n_{\rm i}$ the intrinsic concentration of Si.

The depletion width increases with the increase of the reverse collector–base voltage, the effective vertical punch-through voltage $V_{\rm jPCi}$ is given according to the HICUM compact model definition[11]

$$V_{\rm jPCi} = \frac{qN_{\rm epi}}{2\varepsilon_{\rm Si}}W_{\rm epi}^2 - V_{\rm dc}. \tag{2}$$

Further increase of the collector voltage no longer influences the vertical potential distribution, the space charge region begins to expand horizontally and the voltage drop falls on the horizontal depletion region, which is the case for full depletion. Neglecting the effect of the substrate,[12] from Poisson's equation

$$\frac{{\rm d}E}{{\rm d}y} = \frac{qN_{\rm epi}}{\varepsilon_{\rm Si}} \tag{3}$$

and the boundary conditions

$$E(y) = 0, \tag{4}$$

$$-\int_0^y E(y)\mathrm{d}x = V_{\mathrm{CiBi}} - V_{\mathrm{jPCi}}, \tag{5}$$

we can obtain the horizontal depletion width

$$y = \sqrt{\frac{2\varepsilon_{\mathrm{Si}}(V_{\mathrm{CiBi}} - V_{\mathrm{jPCi}})}{qN_{\mathrm{epi}}}}. \tag{6}$$

In summary, the vertical and horizontal space charge region widths for a partially depleted HBT are listed below:

$$x = \begin{cases} \sqrt{\dfrac{2\varepsilon_{\mathrm{Si}}(V_{\mathrm{CiBi}} + V_{\mathrm{dc}})}{qN_{\mathrm{epi}}}}, & 0 \le V_{\mathrm{CiBi}} \le V_{\mathrm{jPCi}}, \\ W_{\mathrm{epi}}, & V_{\mathrm{CiBi}} > V_{\mathrm{jPCi}}, \end{cases} \tag{7}$$

$$y = \begin{cases} 0, & 0 \le V_{\mathrm{CiBi}} \le V_{\mathrm{jPCi}}, \\ \sqrt{\dfrac{2\varepsilon_{\mathrm{Si}}(V_{\mathrm{CiBi}} - V_{\mathrm{jPCi}})}{qN_{\mathrm{epi}}}}, & V_{\mathrm{CiBi}} > V_{\mathrm{jPCi}}. \end{cases} \tag{8}$$

For a fully depleted HBT, the collector space charge is lateral when $V_{\mathrm{CiBi}} = 0$, with a similar derivation, the vertical and horizontal depletion widths are given as

$$\begin{cases} x = W_{\mathrm{epi}}, & V_{\mathrm{CiBi}} \ge 0, \\ y = \sqrt{\dfrac{2\varepsilon_{\mathrm{Si}}(V_{\mathrm{CiBi}} - V_{\mathrm{jPCi}})}{qN_{\mathrm{epi}}}}, & V_{\mathrm{CiBi}} \ge 0. \end{cases} \tag{9}$$

2.2. Depletion capacitance

The base–collector depletion capacitance is due to variation of the space charge with the applied voltage. We can obtain the corresponding collector depletion charge Q_{tC} of a partially depleted SiGe transistor with thin film SOI under the depletion approximation,

$$Q_{\mathrm{tC}} = \begin{cases} qN_{\mathrm{epi}}\sqrt{\dfrac{2\varepsilon_{\mathrm{Si}}(V_{\mathrm{CiBi}} + V_{\mathrm{dc}})}{qN_{\mathrm{epi}}}}, & 0 \le V_{\mathrm{CiBi}} \le V_{\mathrm{jPCi}}, \\ qN_{\mathrm{epi}}W_{\mathrm{epi}} + qN_{\mathrm{epi}}\sqrt{\dfrac{2\varepsilon_{\mathrm{Si}}(V_{\mathrm{CiBi}} - V_{\mathrm{jPCi}})}{qN_{\mathrm{epi}}}}, & V_{\mathrm{CiBi}} > V_{\mathrm{jPCi}}. \end{cases} \tag{10}$$

With the definition of the depletion capacitance $C_{\mathrm{T}} \equiv \mathrm{d}Q_{\mathrm{t}}/\mathrm{d}V_{\mathrm{t}}$, and after full depletion, the vertical capacitance is constant and expressed as $\varepsilon_{\mathrm{Si}}/W_{\mathrm{epi}}$, the vertical and horizontal capacitance C_{jCiv} and C_{jCih} can be given as

$$C_{\mathrm{jCiv}} = \begin{cases} \dfrac{C_{\mathrm{jC0}}}{(V_{\mathrm{CiBi}}/V_{\mathrm{dc}} + 1)^{1/2}}, & 0 < V_{\mathrm{CiBi}} \le V_{\mathrm{jPCj}}, \\ \varepsilon_{\mathrm{Si}}/\mathrm{W}_{\mathrm{epi}}, & V_{\mathrm{jPCi}} < V_{\mathrm{CiBi}}, \end{cases} \tag{11}$$

$$C_{\mathrm{jCih}} = \frac{C_{\mathrm{jC0}}}{(V_{\mathrm{CiBi}}/V_{\mathrm{dc}} - V_{\mathrm{jPCi}}/V_{\mathrm{dc}})^{1/2}}, \ V_{\mathrm{jPCi}} < V_{\mathrm{CiBi}}, \tag{12}$$

where $C_{\mathrm{jC0}} = (qN_{\mathrm{epi}}\varepsilon_{\mathrm{Si}}/(2V_{\mathrm{dc}}))^{1/2}$. The space charge region extends vertically and approaches the $\mathrm{Si/SiO_2}$ interface with the increase of V_{CiBi} for partially depleted collector, therefore the whole depletion capacitance is the vertical part C_{jCiv} before full depletion. After full depletion, the space charge region expands horizontally as V_{CiBi} increases, the capacitance can be regarded as series of the vertical and horizontal part and given by $1/(1/C_{\mathrm{jCiv}} + 1/C_{\mathrm{jCih}})$. In summary, C_{jCi} for a partially depleted SOI SiGe HBT with abrupt base–collector junction can be expressed as

$$C_{\mathrm{jCi}} = \begin{cases} \dfrac{C_{\mathrm{jC0}}}{(V_{\mathrm{CiBi}}/V_{\mathrm{dc}} + 1)^{1/2}}, & 0 < V_{\mathrm{CiBi}} \le V_{\mathrm{jPCi}}, \\ \dfrac{1}{\dfrac{W_{\mathrm{eip}}}{\varepsilon_{\mathrm{Si}}} + \dfrac{(V_{\mathrm{CiBi}}/V_{\mathrm{dc}} - V_{\mathrm{jPCi}}/V_{\mathrm{dc}})^{1/2}}{C_{\mathrm{jC0}}}}, & V_{\mathrm{jPCi}} < V_{\mathrm{CiBi}}, \end{cases} \tag{13}$$

Apparently the capacitance model shows a kink at the transition point. This causes discontinuities in other important parameters such as the early voltage, the output conductance and the cut-off frequency.

For a fully depleted HBT, C_{jCi} is a series of the constant vertical capacitance $\varepsilon_{\mathrm{Si}}/W_{\mathrm{epi}}$ and the horizontal capacitance with $V_{\mathrm{CiBi}} \ge 0$, and can be given as

$$C_{\mathrm{jCi}} = \frac{1}{\dfrac{W_{\mathrm{epi}}}{\varepsilon_{\mathrm{Si}}} + \dfrac{(V_{\mathrm{CiBi}} - V_{\mathrm{jPCi}}/V_{\mathrm{dc}})}{C_{\mathrm{jC0}}}}, \quad V_{\mathrm{CiBi}} \ge 0. \tag{14}$$

From the derivation and analysis above, we observe that a fully depleted HBT is the limit of a partially depleted one, and analysis of the latter contains

that of the former. Therefore the illustrations and discussion below are focused on the partially depleted device.

3. Illustrations and discussion

For illustration, the transistor has a base width of 35 nm with B doping concentration of about 3×10^{18} cm^{-3}. The Ge is linearly graded up from 10% at the emitter junction side to 25% at the collector junction side of the base. The collector doping concentrations are 1×10^{17} cm^{-3}, 2×10^{17} cm^{-3} and 3×10^{17} cm^{-3}, and the collector width is 150 nm.

Figure 2 shows the effective vertical punch-through voltage versus collector width which depends on collector doping. The voltage increases with the increase of collector width and doping concentration, which is due to more holes afforded by the collector. More holes require more electrons to meet the charge neutrality condition, and therefore require larger electric field and larger effective vertical punch-through voltage.

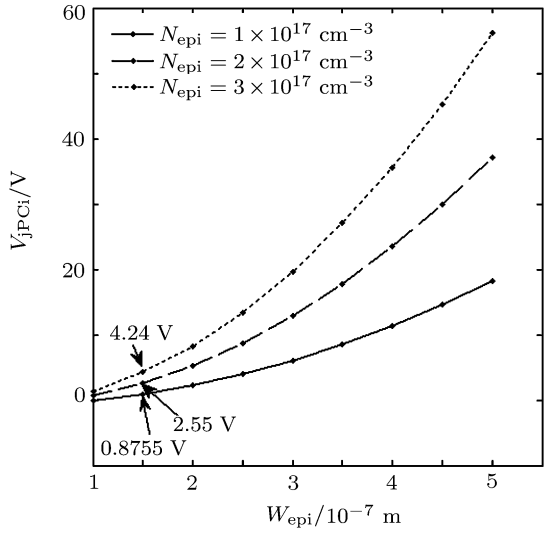


Fig. 2. Effective vertical punch-through voltage as a function of collector width with different collector doping concentrations.

For relatively small N_{epi}, the collector affords fewer holes, the base–collector space charge region extends further vertically to generate more holes to meet the charge neutrality condition, and reaches the Si/SiO_2 interface at relatively smaller reverse collector–base bias, as evidenced in Fig. 3, which plots x, y versus V_{CiBi} as a function of collector doping concentration. Note from the figure that with the increase of V_{CiBi}, the vertical space charge width increases for $V_{CiBi} \leq V_{jPCi}$, and is invariable for $V_{CiBi} > V_{jPCi}$, while horizontal width begins to increase for $V_{CiBi} > V_{jPCi}$. Apparently the direction of the electric field generated by the applied reverse collector–base bias is from collector to base, the same as that of the built-in potential, and larger reverse bias extracts more holes, hence the increase of the vertical space charge width. As the reverse collector–base bias increases for $V_{CiBi} > V_{jPCi}$, the excess electric field requires an increase of holes while the vertical part of the collector is fully depleted, hence the electric field falls on the horizontal part, and the horizontal expansion tendency begins to dominate.

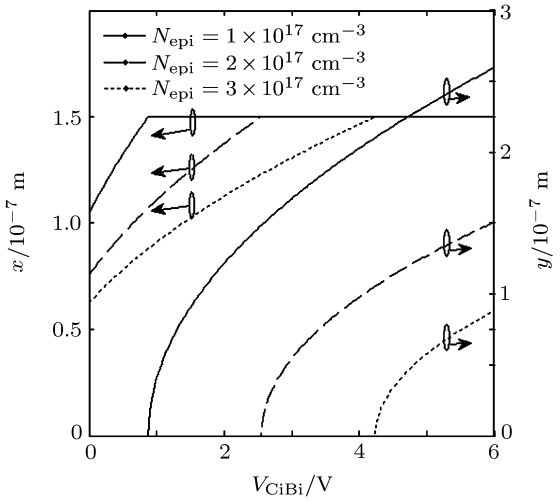


Fig. 3. Vertical and horizontal space charge region widths as a function of reverse collector–base bias with different collector doping concentrations

The relation between the base–collector depletion capacitance and the reverse collector–base voltage as a function of the collector doping concentration is plotted in Fig. 4.

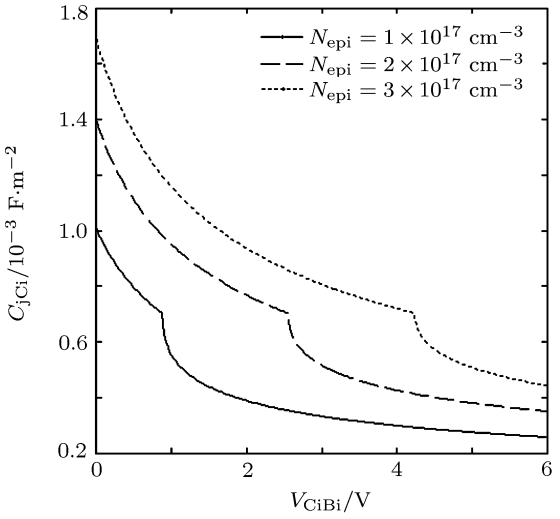


Fig. 4. Results of the base–collector depletion capacitance model, plotted for C versus V_{CiBi} as a function of N_{epi} for SOI SiGe HBT with $W_{epi} = 150$ nm, $N_B = 3 \times 10^{18}$ cm^{-3}.

It is observed that the capacitance decreases with the increase of $V_{\rm CiBi}$, and shows a kink as $V_{\rm CiBi}$ reaches the effective vertical punch-through voltage as evidenced by the discussion above. The capacitance is the vertical part due to vertical depletion when $V_{\rm CiBi} \leq V_{\rm jPCi}$ and the series of the vertical and horizontal part due to the horizontal extension as well as the vertical depletion when $V_{\rm CiBi} > V_{\rm jPCi}$. The discussion of the capacitance in the paper is consistent with the qualitative analysis and measurement reported in Ref. [7].

Figure 5 presents a comparison of the base–collector depletion capacitance between the SOI and standard SiGe HBT with the same collector doping concentration 1×10^{17} cm^{-3}.

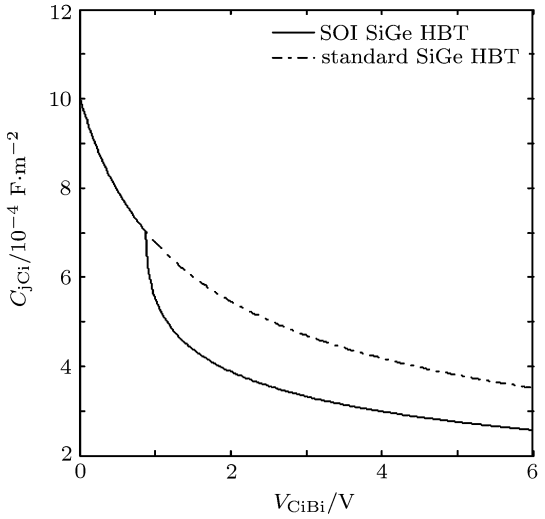


Fig. 5. Comparison of the base–collector depletion capacitance model for SOI and standard SiGe HBT.

As predicted, the capacitances agree well with each other before full depletion of the collector of the SOI HBT, and a large discrepancy is observed when $V_{\rm CiBi} > V_{\rm jPCiv}$ as the base–collector space charge region of the SOI HBT expands horizontally while that of the standard HBT continues the depletion vertically. The smaller capacitance with full depletion of SOI SiGe HBTs explains the inherent higher forward early voltage in comparison with standard devices.[3]

4. Conclusions

An analytical base–collector depletion capacitance model for vertical SiGe HBTs fabricated on CMOS-compatible SOI is developed. The model includes the vertical and horizontal expansion of the base–collector space charge and is applicable to abrupt junction devices under reverse bias conditions. A large discrepancy is predicted when the present model is compared with the conventional depletion model, and it is shown that the capacitance decreases with the increase of $V_{\rm CiBi}$, and shows a kink as $V_{\rm CiBi}$ reaches the effective vertical punch-through voltage while the voltage differs with the collector doping concentration, which is consistent with measurement results by STMicroelectronics. The presentation of the model is significant and has useful applications on the design and simulation of high performance SiGe circuits and devices.

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