Investigation of resistive switching behaviours in WO_3-based RRAM devices*

Li Ying-Tao(李颖弢)[a)b)], Long Shi-Bing(龙世兵)[b)], Lü Hang-Bing(吕杭炳)[b)], Liu Qi(刘 琦)[b)], Wang Qin(王 琴)[b)], Wang Yan(王 艳)[a)b)], Zhang Sen(张 森)[b)], Lian Wen-Tai(连文泰)[b)], Liu Su(刘 肃)[a)†], and Liu Ming(刘 明)[b)]

[a)] *Institute of Microelectronics, School of Physical Science and Technology, Lanzhou University, Lanzhou* 730000, *China*

[b)] *Laboratory of Nano-Fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*

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In this paper, a WO_3-based resistive random access memory device composed of a thin film of WO_3 sandwiched between a copper top and a platinum bottom electrodes is fabricated by electron beam evaporation at room temperature. The reproducible resistive switching, low power consumption, multilevel storage possibility, and good data retention characteristics demonstrate that the Cu/WO_3/Pt memory device is very promising for future nonvolatile memory applications. The formation and rupture of localised conductive filaments is suggested to be responsible for the observed resistive switching behaviours.

Keywords: resistive random access memory, resistive switching, nonvolatile, WO_3

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1. Introduction

To solve the scaling limitation of conventional flash memory, various new types of nonvolatile memory (NVM) such as ferroelectric random access memory (FRAM), magnetic random access memory (MRAM), and resistive random access memory (RRAM) have been proposed. Among all these choices, RRAM device shows a resistive switching between a high resistance state (HRS) and a low resistance state (LRS) by applying appropriate voltages and has attracted great interest due to its excellent scalability, simple structure, fast switching speed, long retention time, and nondestructive readout.[1,2]

So far, large numbers of material systems such as $Pr_{0.7}Ca_{0.3}MnO_3$,[3] GeTe,[4] GeSe,[5] Ag-Ge-S,[6] Cu-doped SiO_2,[7] and TiO_2,[8] have been reported to exhibit nonvolatile resistive switching characteristics. Compared with other material systems, binary transition-metal–oxide (TMO) materials attract more and more attention for application in RRAM devices since they have potential advantages such as simple structure, easy fabrication, and excellent compatibility with the current complementary metal–oxide–semiconductor (CMOS) technology.[7−12] In recent years, tungsten oxide, one of the most promising binary TMO materials, has been especially attractive for its application in RRAM devices because it exhibits advantages not only in its attraction for three-dimensional (3D) stacking, but also in its compatibility with back-end-of-line (BEOL) processing in CMOS integrated circuits.[9−11] Kozicki *et al.*,[9] for example, have recently reported a low power RRAM device based on Cu-doped WO_3. During the fabrication process, photodiffusion of copper into WO_3 is needed,[9] which will make it hard to be employed for applicability to semiconductor processes.[4]

In this paper, a WO_3-based RRAM device with simple Cu/WO_3/Pt sandwiched structure is fabricated. The resistive switching characteristics of the fabricated Cu/WO_3/Pt device are systematically investigated, including repeated resistive switching, switching voltages and currents, data retention, and the feasibility of multilevel operation. The effects of different electrode materials on the resistive switching characteristics, the time-dependent current of the Cu/WO_3/Pt device at a constant voltage, combined with the dependence of device areas on the resis-

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†Corresponding author. E-mail: liusu@lzu.edu.cn

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tance values of both HRS and LRS, indicate that the observed resistive switching characteristics of the $Cu/WO_3/Pt$ device should be ascribed to the formation and rupture of localised conductive filaments.

2. Experimental details

The WO_3-based RRAM devices were fabricated as follows. After chemically cleaning the p^+ silicon wafer, a 150-nm-thick SiO_2 film was thermally grown. Then, Ti as an adhesion layer and Pt as a common bottom electrode (BE), with thickness of 20 nm and 80 nm, respectively, were continuously deposited on the SiO_2/Si substrate by electron beam evaporation. Finally, 50-nm-thick WO_3 film as the storage medium and 50-nm-thick Cu as top electrode (TE) were deposited by electron beam evaporation. During this process, square-shaped device cells with different areas ranging from 100 μm×100 μm to 500 μm×500 μm were achieved and defined by photolithography and lift-off process. For comparison, devices with different top electrodes were also prepared for the switching-mechanism analysis. The electrical characteristics of the fabricated memory devices were measured by a Keithley 4200-SCS semiconductor characterisation system at room temperature. During these measurements, the bias voltage was applied on the Cu top electrode while the Pt bottom electrode was grounded. Except the dependence of HRS and LRS resistances on the device areas, all the tested devices had the same areas of 500 μm×500 μm.

3. Results and discussion

3.1. Resistive switching characteristics of the $Cu/WO_3/Pt$ memory device

The $Cu/WO_3/Pt$ device shows both bipolar and unipolar resistive switching behaviours, as shown in Figs. 1(a) and 1(b), respectively. In the bipolar switching (Fig. 1(a)), by sweeping the voltage to a positive voltage above the set voltage ($V_{\rm set}$), an abrupt increase of device current reaches to compliance current and the device switches from HRS to LRS, which is denoted as set process. While sweeping the voltage to a negative value, a sudden drop of device current is observed at the reset voltage ($V_{\rm reset}$), and the device switches to HRS again (denoted as reset process). In the unipolar switching (Fig. 1(b)), both set and reset processes can be achieved at positive bias voltage. During the set process, a compliance current ($I_{\rm comp}$) of 1 mA was applied to prevent the device from the permanent breakdown.

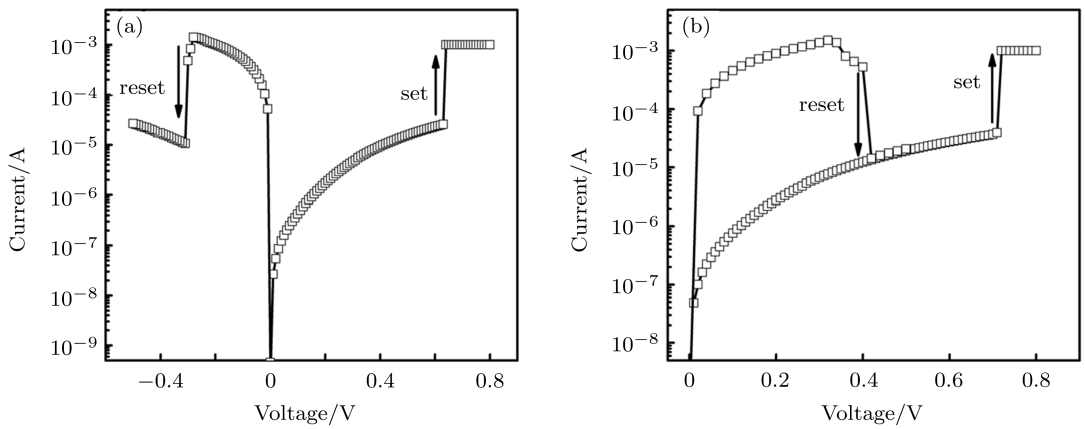


Fig. 1. Typical I–V characteristics of the $Cu/WO_3/Pt$ memory device in (a) bipolar switching behaviour and (b) unipolar switching behaviour.

Figure 2(a) shows the reproducibility of the unipolar switching with 10 switching cycles. It should be noted that the distributions of $V_{\rm set}$ and $V_{\rm reset}$ have an overlapping region in this case, as shown in the dashed region in Fig. 2(a), which may cause the wrong operation in the programming process. The reproducibility of the bipolar switching of the $Cu/WO_3/Pt$ memory device is also demonstrated, and several switching I–V curves are shown in Fig. 2(b). In the case of the bipolar switching, the device can successfully perform 100 resistive switching cycles in direct current (dc) sweeping mode without obvious deterioration, indicating that bipolar switching is more suitable for the $Cu/WO_3/Pt$ memory device. Therefore, the bipolar switching characteristics

of the Cu/WO_3/Pt memory device are focused in the following sections.

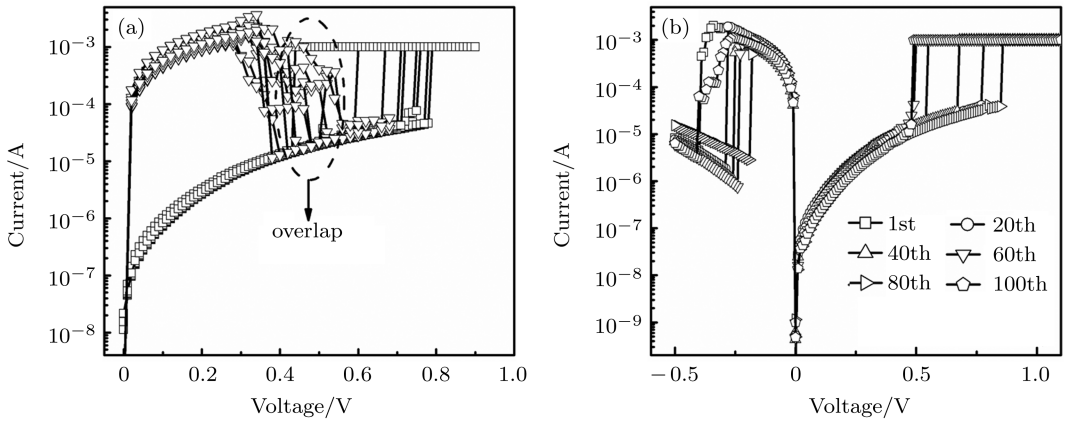


Fig. 2. Reproducible resistive switching characteristics of the Cu/WO_3/Pt memory device in (a) unipolar switching behaviour with 10 switching cycles, and (b) bipolar switching behaviour with 100 switching cycles. In the unipolar switching, an overlap between V_{set} and V_{reset} is observed. In the bipolar switching, after 100 repeated switching cycles, the shape of the I–V curve is similar to that in the first sweep, indicating good reproducible behaviour.

Figure 3(a) shows the distributions of HRS and LRS resistances (R_{HRS} and R_{LRS}) during 100 dc switching cycles. The resistance values are obtained by a 0.1 V reading voltage in each dc sweeping. Although both R_{HRS} and R_{LRS} show some fluctuations, no overlap between them is observed even after 100 successive switching cycles, and the resistance ratio of HRS to LRS is over 10^2 for the worst case and over 10^3 in general. Such a resistance ratio is large enough to distinguish these two states to store information ('1' and '0'). The distributions of both voltages (V_{set} and V_{reset}) during these cycles are shown in Fig. 3(b). It is noted that V_{reset} is distributed from –0.18 to –0.44 V, while V_{set} has a wide distribution from 0.26 to 0.93 V. The average value and standard deviation of these switching resistances and voltages are also indicated in Figs. 3(a) and 3(b), respectively. The variations of these switching parameters of the Cu/WO_3/Pt memory device are similar to other reported results,[7–9] which can be attributed to the random formation and rupture of conducting filaments.[12–15]

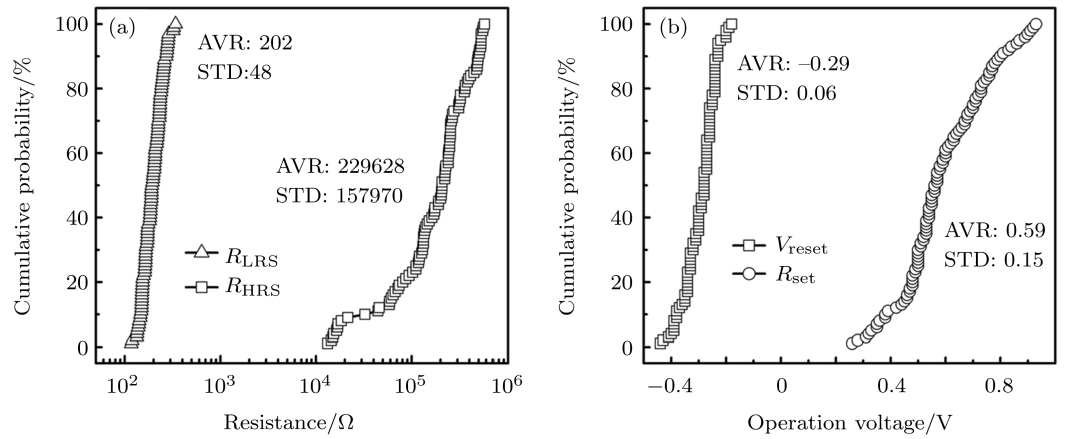


Fig. 3. Distributions of (a) R_{HRS} and R_{LRS}, and (b) V_{set} and V_{reset} of the Cu/WO_3/Pt memory device. AVR and STD represent average value and standard deviation of these switching parameters, respectively.

Previous works have shown that the reset current can be controlled through the external compliance current I_{comp}.[16–18] In our case, when we decrease the I_{comp} to a lower value of 0.1 mA during the set process, the Cu/WO_3/Pt memory device can also show bistable resistive switching behaviour and the resistance ratio is still close to 10^2, as shown in Fig. 4(a). From Fig. 4(a), we also observe that the reset current in this case can be reduced to 60 μA. The low reset current together with the low operation voltages as shown in Fig. 3(b), demonstrates that the Cu/WO_3/Pt memory device is suitable for low-power memory applications. The dependence of LRS resistance and reset current on I_{comp} of the Cu/WO_3/Pt memory device is shown in

Fig. 4(b). It can be seen that $I_{\rm comp}$ strongly influences LRS resistance and reset current, in which the LRS resistance decreases, while the reset current increases with increasing $I_{\rm comp}$. Based on the relationship between LRS resistance and $I_{\rm comp}$, the Cu/WO_3/Pt memory device exhibits the capability of multilevel operation.

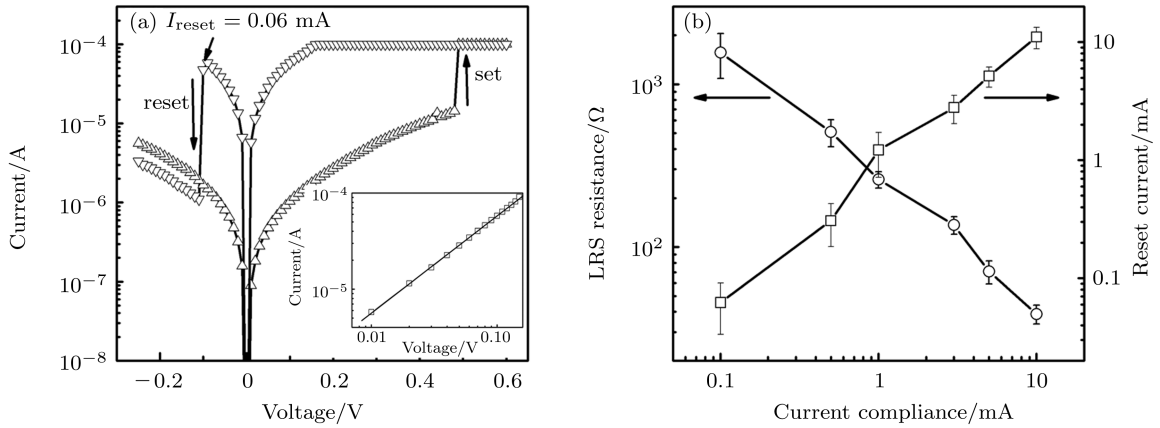


Fig. 4. (a) *I–V* curve of the Cu/WO_3/Pt memory device with a compliance current of 0.1 mA. The inset shows the *I–V* curve of the LRS in log–log scale. (b) Dependence of the LRS resistance and reset current on the $I_{\rm comp}$ values.

In addition, the retention characteristic of the Cu/WO_3/Pt memory device is also investigated. As can be seen from Fig. 5, the resistance values of both HRS and LRS exhibit little change over 10^5 seconds, indicating that this memory device is potentially suitable for nonvolatile memory applications.

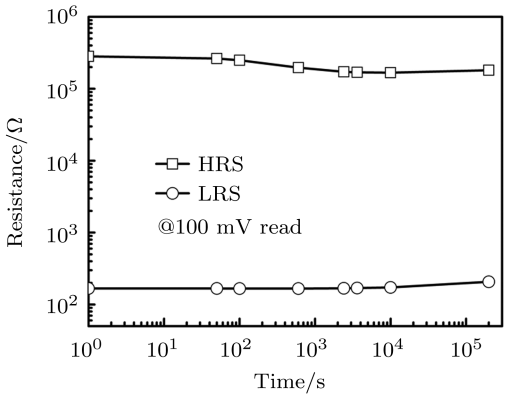


Fig. 5. Retention characteristics of the Cu/WO_3/Pt memory device at room temperature.

3.2. Resistive switching mechanism of the Cu/WO_3/Pt memory device

So far, several mechanisms and hypothetical models have been proposed to explain resistive switching phenomena. However, the intrinsic mechanisms in RRAM devices are still surprisingly divergent and not yet clearly understood. According to the experimental observations, the formation and rupture of conductive filaments is considered to be the most reasonable mechanism to explain the resistive switching of the Cu/WO_3/Pt memory device, since the *I–V* curve of the memory device for the LRS in the log–log scale clearly exhibits an ohmic conduction with a slope of 1, as shown in the inset of Fig. 4(a), which might serve as a clue to claim the resistive switching mechanism of the Cu/WO_3/Pt memory device as filament conduction.[13,18] In addition, the filament model suggests that $R_{\rm LRS}$ decreases, while the reset current increases with increasing $I_{\rm comp}$ values.[5,6,16–18] Similar phenomenon is also observed in our device as shown in Fig. 4(b), which might serve as another clue to validate the filament model. Based on the fact that the reset process of the Cu/WO_3/Pt memory device is polarity-independent, we believe that the rupture of conductive filaments is probably thermally dominated.[7,18]

To further understand the resistive switching mechanism of the Cu/WO_3/Pt memory device, Al, Cr, W-probe instead of Cu were used as top electrodes in the same device structure. Figure 6(a) shows the typical *I–V* curves of Al/WO_3/Pt, Cr/WO_3/Pt and W-probe/WO_3/Pt memory devices, and the comparison of resistive switching cycles between Cu/WO_3/Pt memory device and these three WO_3-based memory devices is shown in Fig. 6(b). From Fig. 6(b), it is clear that the reproducibility of the Cu/WO_3/Pt memory device is much superior to that of the Al/WO_3/Pt, Cr/WO_3/Pt and W-probe/WO_3/Pt memory devices. Therefore, it can be concluded that electrode materials play an important role in resistive switching of

WO_3-based RRAM devices. Because Cr and Cu have the similar work function, it is suggested that the energy barrier at the electrode/WO_3 interface might not play an important role in the resistive switching characteristics. It is well known that Cu is an electrochemically active metal and can be regarded as a fast diffuser to migrate in WO_3 film.[9] When a positive voltage is applied to the easily oxidisable Cu anode, Cu can be electrochemically oxidised at the anode interface to form cations that are driven into the WO_3 film under the electrical field and finally reduced at the inert Pt cathode, forming a metallic conduction path. Al is also easily oxidised, but cannot easily move in WO_3 film, so we do not observe excellent resistive switching characteristics in Al/WO_3/Pt device. Based on these results, it is reasonable to suppose that electrochemical reactions and ion migration closely related to Cu electrode are responsible for the advantages of good reproducibility, low power consumption and multilevel operation in Cu/WO_3/Pt memory device, similar to the so-called conductive bridging RAM (CBRAM) devices.[5,6]

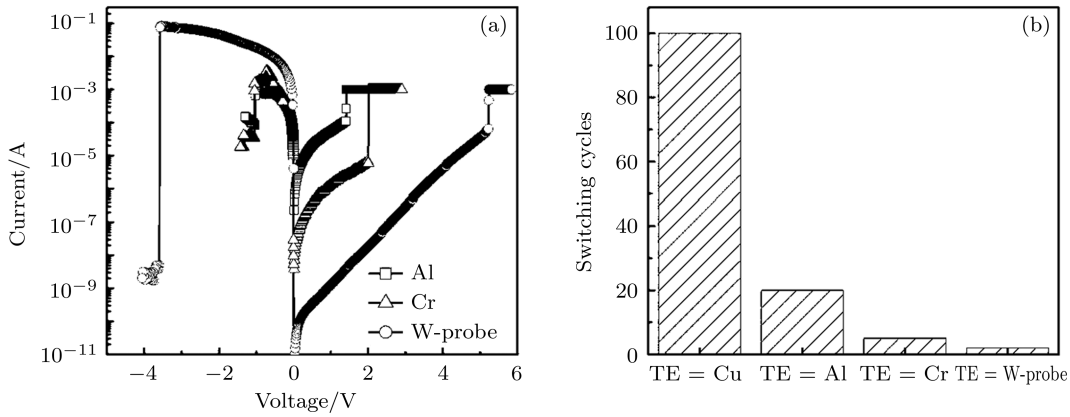


Fig. 6. (a) Typical I–V curves of Al/WO_3/Pt, Cr/WO_3/Pt and W-probe/WO_3/Pt memory devices. (b) Comparison of resistive switching cycles of WO_3-based memory devices with different top electrodes (TEs).

The time-dependent current of the device at a constant voltage is performed to further confirm the switching mechanism, as shown in Fig. 7. It can be seen that current jump is observed with the evolvement of treatment time during the set process. When a constant voltage of 0.3 V is applied on the Cu top electrode, the current increases abruptly at about 20 s with a current ratio over 10^2, indicating that the device switches from the HRS to the LRS due to the formation of single or multiple conductive filamentary paths. When the time continues increasing, the current shows a sudden increase in multiple discrete steps, as shown in the inset of Fig. 7. This phenomenon may be attributed to the formation of more conductive filaments. According to electrochemical redox process in solid electrolytes RRAM devices,[19,20] the set process is related to the amount of charges flowing through the device cell and the concentration of oxidised cations. With the increase of time, more cations migrate toward the Pt inert electrode under the electrical field where the reduction reaction happens, and thus can form more conductive filaments. Besides, the stepwise current switching phenomenon at a constant voltage in our case is similar to the simulation results for electrochemical reactions based on electrical field treatment by Chen *et al.*,[21] which provides sufficient evidence that the formation of conductive filaments is related to electrochemical reactions.

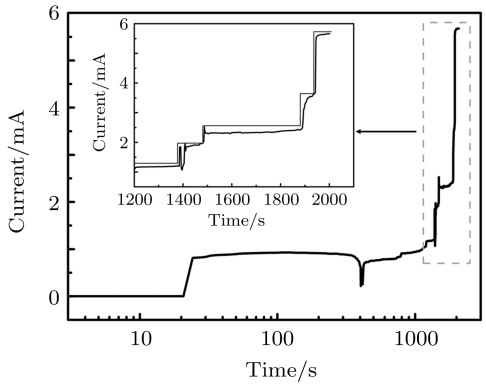


Fig. 7. Current versus time characteristic of the Cu/WO_3/Pt memory device at a constant voltage of 0.3 V. Clear stepwise current switching is observed during the set process. The inset shows the I–t curve of the dashed square region. The folded line can better depict these steps.

The dependence of the resistance on device area of the Cu/WO_3/Pt memory device is shown in Fig. 8(a). It is found that the resistance of the HRS increases with decreasing device area, but the resistance of the LRS shows little dependence on device area. The formed localised filament may be responsible for the area insensitive property of the LRS resistance.[13,18] The localised filament is further confirmed in Fig. 8(b). A memory device with initial HRS is first switched from the HRS to the LRS under a positive voltage. Then, the top electrode is cut into two parts (Part 1 and Part 2). In order to compare with the uncut device, the I–V characteristics of these two parts are measured. As expected, Part 1 is LRS, while the resistance value of the Part 2 is comparable to the value of the HRS, as shown in Fig. 8(b). These results suggest that the resistive switching from HRS to LRS occurs on the side of Part 1, which is a strong indication that the conductive path is localised.

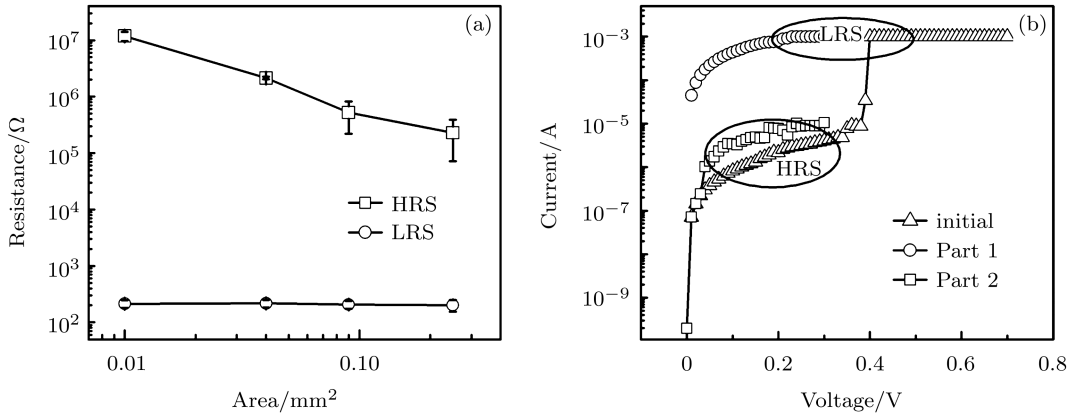


Fig. 8. (a) Device area dependence of HRS and LRS resistances of the Cu/WO_3/Pt memory device. Different device areas of 0.01 mm^2, 0.04 mm^2, 0.09 mm^2, and 0.25 mm^2 are measured to demonstrate the correlation between resistance and device area. (b) I–V characteristics of a Cu/WO_3/Pt memory device with initial HRS. After switching the device cell from the HRS to the LRS, the top electrode is cut into two parts, and the I–V curves of Part 1 and Part 2 are respectively measured to demonstrate the localised resistive switching.

4. Conclusions

An RRAM device with Cu/WO_3/Pt structure is demonstrated for nonvolatile memory applications. The devices show excellent resistive switching characteristics, such as good endurance, low power, and reliable data retention. The effects of different top electrode materials on the resistive switching characteristics, combined with the time dependence of the current at a constant voltage, imply that electrochemical reactions play an important role in the resistive switching of the Cu/WO_3/Pt memory device. The dependence of device areas on the HRS and LRS resistances provides further evidence that the resistive switching mechanism is related to the formation and rupture of localised conductive filaments. The advantages of reproducible resistive switching, low power consumption, multilevel storage possibility and good retention make Cu/WO_3/Pt memory device potentially suitable for future nonvolatile memory applications.

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