Improved performance of 4H-SiC metal-semiconductor field-effect transistors with step p-buffer layer*

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An improved 4H-SiC metal-semiconductor field-effect transistors (MESFETs) with step p-buffer layer is proposed, and the static and dynamic electrical performances are analysed in this paper. A step p-buffer layer has been applied not only to increase the channel current, but also to improve the transconductance. This is due to the fact that the variation in p-buffer layer depth leads to the decrease in parasitic series resistance resulting from the change in the active channel thickness and modulation in the electric field distribution inside the channel. Detailed numerical simulations demonstrate that the saturation drain current and the maximum theoretical output power density of the proposed structure are about 30% and 37% larger than those of the conventional structure. The cut-off frequency and the maximum oscillation frequency of the proposed MESFETs are 14.5 and 62 GHz, respectively, which are higher than that of the conventional structure. Therefore, the 4H-SiC MESFETs with step p-buffer layer have superior direct-current and radio-frequency performances compared to the similar devices based on the conventional structure.

Keywords: 4H-SiC, metal-semiconductor field-effect transistors, step buffer layer
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1. Introduction

Silicon carbide (SiC) is one of the materials for choice in advanced next-generation power electronics both for high frequency, high temperature and high voltage power-switching applications due to its excellent electrical and physical properties, i.e., wide band gap, high electron saturation velocity, high critical electric field, high radiation stability, and high thermal conductivity.[1−3] These properties have made SiC metal-semiconductor field-effect transistors (MESFETs) a promising candidate for microwave power applications. In recent years, SiC MESFETs are in the market, and the application areas are the commercial and military communication and radars.

As is known to all, the use of a p-buffer layer that isolates the semi-insulating substrate from the active channel is of vital importance and can significantly reduce the substrate trapping effects associated with the channel-substrate interface for MESFETs.[4] The performance and reliability correlate closely to the critical characteristics of off-state breakdown voltage and parasitic capacitance that are strongly dependent on the quality and behaviour of the p-buffer layer. Since the SiC material growth and the device fabrication technology are becoming quite mature, substrate trapping effects of SiC MESFETs can be alleviated by the introduction of high-purity semi-insulating substrate.[5] Hence the p-buffer layer of the device will play a critical role to improve the device performances, which needs to be carefully designed in order to provide the needed channel isolation while not hindering high-frequency device operation by introducing significant parasitic capacitance and drain leakage current. Although a large number of SiC MESFETs structures and various optimisations have been reported,[6,7] few studies of p-buffer layer configuration in SiC MESFETs have been performed up to now.

In this paper, an improved 4H-SiC MESFETs with step p-buffer layer is investigated using a two-dimensional (2D) device simulation program, ATLAS. The thinner p-buffer layer in ungate channel region is employed to obtain low parasitic series resistance, while the thicker p-buffer layer underneath the gate terminal is adopted to maintain a larger aspect ratio of gate length to channel thickness (L_g/a). The direct-current (DC) and radio-frequency (RF) performances of the proposed 4H-SiC MESFETs have been studied in detail, and the simulation results are compared with those obtained from the conventional p-

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buffer layer device.

2. Device structure and physical model

2.1. Device structure

Schematic cross-sections of the proposed and conventional 4H-SiC MESFETs are shown in Figs. 1(a) and 1(b). To compare the characteristics of the proposed structure with the conventional one, the basic parameters of the structure, except for the p-type buffer layer configuration, are left unchanged and described as follows. The layer stack consists of four layers: an ideal high-purity semi-insulating (HPSI) substrate, a p-type buffer layer, an n-type active layer with 0.25 μm thickness and doping level $N_{\rm d} = 3.1 \times 10^{17}$ cm^{-3}, and an N$^+$ cap layer with a thickness of 0.2 μm and doping level $N_{\rm d} = 1.0 \times 10^{19}$ cm^{-3}. In order to completely remove the cap layer in the recessed etching, overetching of about 500 Å (1 Å=0.1 nm) is applied in the simulations. The gate length $L_{\rm g}$ is 0.5 μm, and the gate–source and the gate–drain spacings, $L_{\rm gs}$ and $L_{\rm gd}$, are 0.5 and 1.0 μm, respectively. The gate width W is 100 μm, and a temperature of 300 K is employed by default in the simulations. The step buffer layer structure consists of the p-doped layer ($N_{\rm a} = 4 \times 10^{16}$ cm^{-3}) with stepped thicknesses of 0.9 (a_1), 0.95 (a_2) and 1.0 μm (a_3). Step length in the gate–source region ($L_{\rm step}$) is 0.25 μm. As a result, the thickness of the channel layer underneath the gate is 0.2 μm (a_4). To have a meaningful comparison, the channel thickness of the MESFETs based on the conventional structure is also set at 0.2 μm, namely, a 1.0 μm thick p-type buffer layer with $N_{\rm a} = 4 \times 10^{16}$ cm^{-3}.

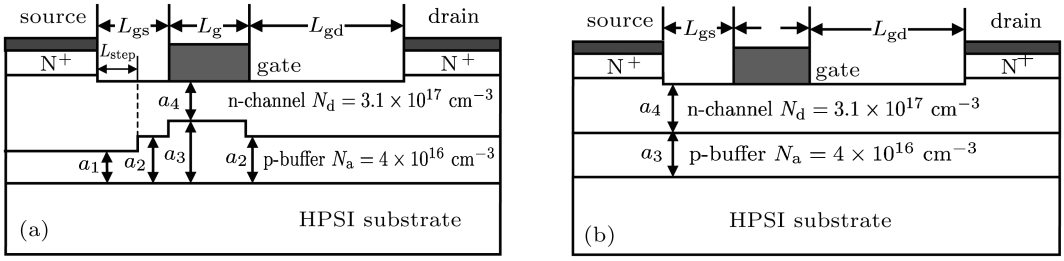


Fig. 1. Schematic cross-sections of 4H-SiC MESFETs with (a) step p-buffer layer structure and (b) conventional structure.

2.2. Physical models

The 2D numerical device characteristics are realised with Atlas from Silvaco. In addition to basic Poisson and the drift/diffusion equations, the different physical models used simultaneously in Silvaco are SRH (Shockley–Read–Hall) and Auger ones for generation and recombination, respectively, analytic and Fldmob for mobility, incomplete for incomplete ionisation of dopants, and finally, impact Selb for impact ionisation. Here traps in the HPSI substrate are not considered.

The mobility of the carriers in 4H-SiC is modeled using the Caughey–Thomas expression, which is used to specify doping- and temperature-dependent low field mobility.[8]

$$\mu_{\rm n,p} = \mu_{\rm 0n,p}^{\rm min} \left(\frac{T}{300\ {\rm K}} \right)^{\alpha_{\rm n,p}} + \frac{\mu_{\rm 0n,p}^{\rm min} \left(T/300\ {\rm K}\right)^{\beta_{\rm n,p}} - \mu_{\rm 0n,p}^{\rm min} \left(T/300\ {\rm K}\right)^{\alpha_{\rm n,p}}}{1 + \left(N/N_{\rm n,p}^{\rm crit}\right)^{\gamma_{\rm n,p}}}, \quad (1)$$

where N is the total impurity concentration and $N_{\rm n,p}^{\rm crit}$ is the doping concentration at which the mobility is halfway between the minimum and maximum values, namely the mobilities in highly doped and undoped materials. Both $\mu_{\rm 0n,p}^{\rm min}$ and $\mu_{\rm 0n,p}^{\rm max}$ are the mobility values at room temperature.[9] Exponents α, β and γ are fitting parameters.

Velocity saturation at high electric fields is modeled with the Canali model.

$$\mu_{\rm n,p}(E) = \frac{\mu_{\rm n_0,p_0}}{\left(1 + \left(\mu_{\rm n_0,p_0} E/\upsilon_{\rm sat}\right)^{\beta_E}\right)^{1/\beta_E}}, \quad (2)$$

here, E is the parallel electric field, β_E is a fitting parameter and $\mu_{\rm n0}$ and $\mu_{\rm p0}$ are the low field electron and hole mobilities respectively.

The simulator Atlas accounts for the impurity frozen-out with appropriate degeneracy factors $G_{\rm cb}$ and $G_{\rm vb}$ for conduction and valence bands respectively. The ionised donor and acceptor impurity concentrations are then given by[10]

$$N_{\rm d}^{+} = \frac{N_{\rm d}}{1 + G_{\rm cb} \exp\left(\dfrac{E_{\rm Fn} - (E_{\rm c} + E_{\rm db})}{kT}\right)}, \quad (3)$$

$$N_{\rm a}^{-} = \frac{N_{\rm a}}{1 + G_{\rm vb} \exp\left(\dfrac{(E_{\rm v} + E_{\rm ab}) - E_{\rm Fp}}{kT}\right)}, \quad (4)$$

where $E_{\rm db}$ is the donor energy level, $E_{\rm ab}$ is the acceptor energy level, $E_{\rm Fn}$ and $E_{\rm Fp}$ are the quasi-Fermi energy levels for electrons and holes, $E_{\rm c}$ and $E_{\rm v}$ are conduction and valence band edge energies, and $N_{\rm d}$ and $N_{\rm a}$ are net compensated n-type and p-type dopingcontents, respectively.

The effect of the recombination centres can be described by the conventional SRH recombination/generation expression

$$R_{\rm SRH} = \frac{np - n_{\rm i}^2}{\tau_{\rm p}(n + n_{\rm i}\exp(E_{\rm trap} - E_{\rm c})) + \tau_{\rm n}(p + n_{\rm i}\exp(E_{\rm v} - E_{\rm trap}))}, \quad (5)$$

where

$$\tau_{\rm n,p} = \frac{\tau_{\rm n0,p0}}{1 + (N/N_{\rm n,p})}, \quad (6)$$

here, $\tau_{\rm n}$ and $\tau_{\rm p}$ are electron and hole lifetimes, $n_{\rm i}$ is the effective intrinsic carrier concentration, n and p are electron and hole densities, $E_{\rm trap}$ is the difference between the trap energy level and the intrinsic Fermi level, and $N_{\rm n,p}$ expresses the characteristic parameter for electrons and holes, respectively. For the sake of simplicity a difference $E_{\rm trap} = 0$ was assumed during this analysis.

Auger recombination was also considered and calculated by introducing the coefficients $C_{\rm n}$ and $C_{\rm p}$ given in Ref. [11]

$$R_{\rm AU} = (C_{\rm n}n + C_{\rm p}p)(np - n_{\rm i}^2). \quad (7)$$

The temperature dependence of the band gap is modeled as

$$E_{\rm g}\,(T) = E_{\rm g}^{300} - 3.3 \times 10^{-4}(T - 300), \quad (8)$$

where $E_{\rm g}^{300}$ is the band gap energy at room temperature.

3. Results of analysis and discussion

3.1. DC Characteristics

In Fig. 2 we compare the simulated I–V characteristics of a conventional and step p-buffer layer structures under the gate bias ($V_{\rm gs}$) varied from to -8 V in a step of -4 V. It is noted that the proposed MESFETs provides a larger saturation drain current than the conventional MESFETs. As is seen from the figure, the saturation drain current ($I_{\rm dsat}$) at $V_{\rm gs} = 0$ V and $V_{\rm ds} = 40$ V is about 350 mA·mm^{-1} for the SiC MESFETs with step p-buffer layer, whereas it is only about 270 mA·mm^{-1} for the conventional MESFETs. This enhancement in the value of $I_{\rm dsat}$ is due to a wider channel region between source/drain and gate terminals, which results in low parasitic series resistance.

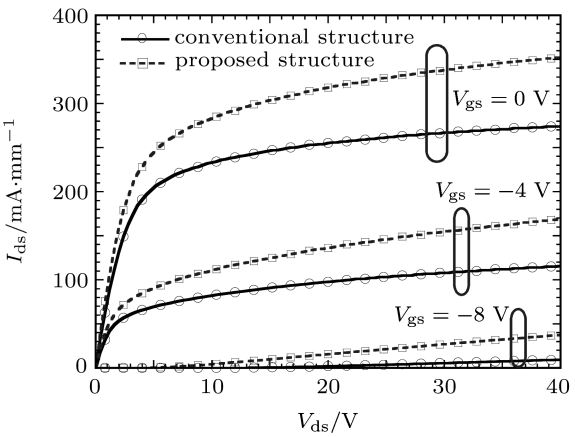


Fig. 2. I–V characteristics for the MESFETs with proposed and conventional structures.

The simulated three-terminal breakdown characteristics for both types of devices are illustrated in Fig. 3. It can be observed from the figure that the source–drain breakdown voltage ($BV_{\rm ds}$) of the proposed structure is about 90 V by exploiting the standard fixed threshold definition of the breakdown voltage ($I_{\rm ds} = 1$ mA·mm^{-1}), which is almost the same as that of the conventional structure. A further investigation shows that the breakdown occurs at gate edge towards drain due to the electric field crowding at that

edge for the two structures. Therefore, the breakdown characteristic of the proposed SiC MESFETs is found to be very similar to that of the conventional MESFETs.

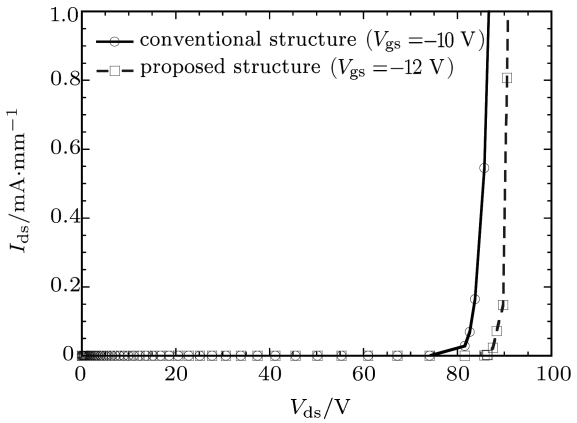


Fig. 3. Simulated three-terminal breakdown characteristics.

For a Class A amplifier, the maximum theoretical output power density (P_{max}) can be expressed as

$$P_{max} = \frac{I_{dsat}(BV_{ds} - V_{knee})}{8}, \tag{9}$$

where V_{knee} is the knee voltage. According to the above equation, P_{max} of the step buffer layer and conventional 4H-SiC MESFETs are about 3.7 W·mm^{-1} and 2.7 W·mm^{-1} respectively. Therefore, the proposed structure has superior power performance compared to a similar device with the conventional structure.

3.2. Small signal characteristics

Small-signal characteristics for 4H-SiC MESFETs with step p-buffer layer and conventional structures are estimated by S-parameter simulation from 800 MHz–80 GHz. Values of the parasitic elements for the equivalent circuit are extracted using the Dambrine method.[12] Figure 4 shows frequency dependence of the small signal current gain h_{21}, maximum stable gain (MSG), maximum available gain (MAG) and unilateral power gain (U) simulated under the bias conditions of $V_{gs} = 0$ V and $V_{ds} = 40$ V. The results show that the cut-off frequency f_T (defined as the frequency at which the current gain is equal to 1) and the maximum oscillation frequency f_{max} (defined as the frequency at which the unilateral power gain is unity) of the proposed structure are 14.5 and 62 GHz, respectively. On the other hand, for the conventional SiC MESFETs, f_T and f_{max} are 12.5 and 51 GHz, respectively. This improvement in f_T and f_{max} is attributed to the increase of the transconductance as well as the decrease of the parasitic series resistance compared to the conventional p-buffer layer MESFETs.

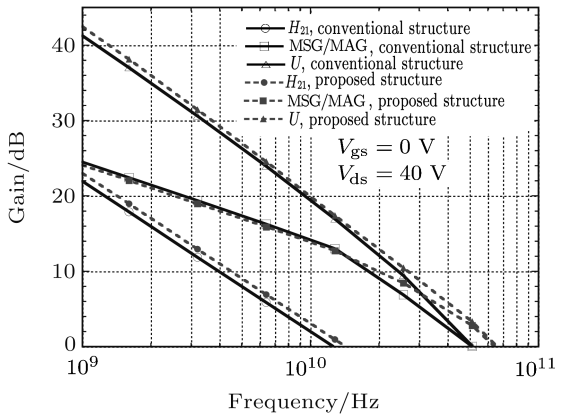


Fig. 4. Simulated small-signal high frequency characteristics of 4H-SiC MESFETs.

To understand the origin of the increase in f_T and f_{max}, the comparisons of gate-to-source capacitance (C_{gs}) and transconductance (g_m) extracted from S-parameters as a function of frequency for the two structures of simulations previously discussed are shown in Fig. 5. As compared to the conventional structure, the MESFETs with step p-buffer layer shows an approximately 17.4% g_m improvement at $V_{ds} = 40$ V and $V_{gs} = 0$ V, while the value of C_{gs} increases from 5.55×10^{-14} to 5.69×10^{-14} F. The increase of g_m is due to the fact that the variation in p-buffer layer depth results in the change in the active channel thickness, which modifies the electric field distribution inside the channel and, consequently, the electron velocity. The increase in C_{gs} is considered to be caused by the excess charges in the depletion extension region at the edge of the gate, arising from a wider channel opening outside of the gate terminal. It is known that, in the intrinsic FET, the cut-off frequency and the maximum oscillation frequency are given as follows:[13]

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{10}$$

$$f_{max} \approx \frac{f_T}{2\sqrt{r_1 + f_T\tau_3}}, \tag{11}$$

where

$$r_1 = \frac{R_g + R_i + R_s}{R_{ds}},$$
$$\tau_3 \equiv 2\pi R_g C_{gd}, \tag{12}$$

and R_g is the gate resistance, R_i and R_{ds} are the input and output resistances under the gate, C_{gd} is gate-to-drain capacitance. As is inferred from Eq. (10), the improvement of g_m has a positive impact on the cut-off frequency of SiC MESFETs, whereas the increase of C_{gs} shows the opposite behaviour. Although C_{gs} of the proposed 4H-SiC MESFETs is slightly larger than that of the conventional one, the important quantity g_m/C_{gs} still increases because of an effective enhancement in g_m.

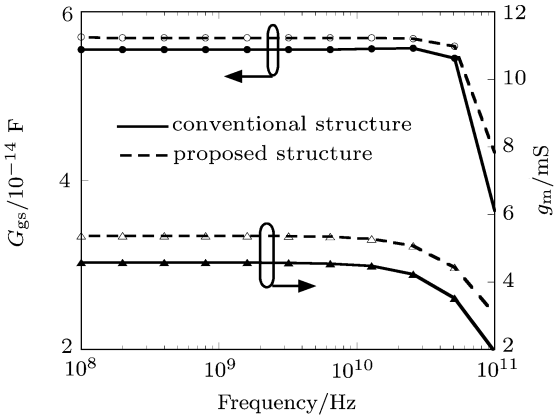


Fig. 5. Change of the extracted gate-to-source capacitance and transconductance as functions of the frequency.

Hence, it can be concluded that the higher f_T of the step p-buffer layer structure is derived from the larger g_m/C_{gs} ratio. The behaviour of f_{max}, as shown in Fig. 4, can be interpreted using Eqs. (10) and (11). In fact, the proposed structure will increase transconductance and decrease the parasitic series resistance compared to the conventional structure, which is responsible for an approximately 22% f_{max} improvement.

4. Conclusion

In this work, the electrical performances of a newly developed 4H-SiC MESFETs with step p-buffer layer are investigated in detail by 2D device simulation. The simulation results show that the saturation drain current and the output power density of the step p-buffer layer structure are about 30% and 37% larger than those of the conventional structure, due to wider channel opening between source/drain and gate terminals. The cut-off frequency and the maximum oscillation frequency of the proposed MESFETs are 14.5 and 62 GHz, respectively. On the other hand, the cut-off frequency and the maximum oscillation frequency are only 12.5 and 51 GHz for the conventional MESFETs. Compared to conventional device, the proposed device shows an approximately 17.4% improvement in transconductance at $V_{gs} = 0$ V and $V_{ds} = 40$ V. Therefore, the 4H-SiC MESFETs with step p-buffer layer have superior DC and RF performances compared to the similar device based on the conventional structure.

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