Two-dimensional analytical models for asymmetric fully depleted double-gate strained silicon MOSFETs*

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This paper develops the simple and accurate two-dimensional analytical models for new asymmetric double-gate fully depleted strained-Si MOSFET. The models mainly include the analytical equations of the surface potential, surface electric field and threshold voltage, which are derived by solving two dimensional Poisson equation in strained-Si layer. The models are verified by numerical simulation. Besides offering the physical insight into device physics in the model, the new structure also provides the basic designing guidance for further immunity of short channel effect and drain-induced barrier-lowering of CMOS-based devices in nanometre scale.

Keywords: strained-Si, double-gate MOSFET, surface potential, short-channel effect

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1. Introduction

As complementary–metal–oxide–semiconductor (CMOS) design is approaching nanometre scale, the lateral short-channel effect (SCE) and gate insulator direct tunneling will degrade the device performance greatly.[1−3] One of the approaches to overcome the gate tunneling restriction is to change the device structure in such a way that the gate length of metal–oxide–semiconductor field effect transistor (MOSFET) can still be scaled down for thinner oxide. The double-gate (DG) MOSFET is considered as one of the most attractive devices for the planar MOSFET.[4−6] With the advantages of enlarging the circuit design space, asymmetric DG MOSFET is a very promising device, its front gate and the back gate can be driven independently. Furthermore, strained-Si devices can enhance mobility, improve the device switching speed in very-large scale integrated circuit (VLSI), suppress velocity overshoot of carriers, it is a promising candidate for future high–performance MOSFET.[7] To incorporate the advantages of both asymmetric DG and strained-Si, the asymmetric fully depleted DG strained-Si MOSFET is presented in this paper. Based on the exact resultant solution of two-dimensional Poisson equation, the physical models for asymmetric fully depleted DG strained-Si MOSFET are presented. The models include calculation of the channel potential, surface electric field and threshold voltage. The model calculations are compared with the simulation results. It is shown that the model calculations are consistent with the two-dimensional numerical simulation results. By adding appropriate modification, the model can also be extended to symmetric DG MOSFET.

2. Strained-Si MOSFET

2.1. Effect of strain on bandgap

In the presence of strain, the thin film of silicon experiences the biaxial tension, and the energy band structure is changed.[8−11] The strain can increase the electron affinity of silicon, decrease the bandgap and the effective mass of carriers. The above strain-related effects on the silicon band structure can be modeled as follows:[12,13]

$$(\Delta E_{\mathrm{C}})_{\mathrm{s-Si}} = 0.57X, \tag{1}$$

$$(\Delta E_{\mathrm{g}})_{\mathrm{s-Si}} = 0.4X, \tag{2}$$

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$$V_{\rm T}\ln\left(\frac{N_{\rm V,Si}}{N_{\rm V,s-Si}}\right) = V_{\rm T}\ln\left(\frac{m^*_{\rm h,Si}}{m^*_{\rm h,s-Si}}\right)^{3/2} = 0.075X, \quad (3)$$

where X is the strain in equivalent Ge mole fraction in the relaxed SiGe butter layer, $(\Delta E_{\rm C})_{\rm s-Si}$ is the increase in electron affinity of silicon due to strain, $(\Delta E_{\rm g})_{\rm s-Si}$ is the decrease in the bandgap of silicon due to strain, $V_{\rm T}$ is the thermal voltage, $N_{\rm V,Si}$ and $N_{\rm V,s-Si}$ are the density of states (DOS) in the valence band in normal and strained-Si, respectively, $m^*_{\rm h,Si}$ and $m^*_{\rm h,s-Si}$ are effective masses of hole DOS in normal and strained-Si, respectively.

2.2. Effect of strain on flatband voltage

Since the structure is symmetrical, the effect of strain on flatband voltage of the front-channel and back-channel can be modeled as follows:[12,13]

$$(V_{\rm FB,f})_{\rm s-Si} = (V_{\rm FB,f})_{\rm Si} + \Delta V_{\rm FB,f}, \quad (4)$$

where

$$(V_{\rm FB,f})_{\rm Si} = \phi_{\rm M} - \phi_{\rm Si},$$
$$\Delta V_{\rm FB,f} = \frac{-(\Delta E_{\rm C})_{\rm s-Si}}{q} + \frac{(\Delta E_{\rm g})_{\rm s-Si}}{q} - V_{\rm T}\ln\left(\frac{N_{\rm V,Si}}{N_{\rm V,s-Si}}\right),$$

$$\phi_{\rm Si} = \chi_{\rm Si}/q + E_{\rm g,Si}/2q + \phi_{\rm f-Si},$$
$$\phi_{\rm f-Si} = V_{\rm T}\ln(N_{\rm A}/n_{\rm i,Si}).$$

In above relations, $\phi_{\rm M}$ is the work function of the gate, $\phi_{\rm Si}$ is the work function of unstrained-Si, $\phi_{\rm f-Si}$ is the Fermi potential of unstrained-Si, $E_{\rm g,Si}$ is the bandgap of unstrained-Si, q is the electronic charge, $N_{\rm A}$ is the body doping concentration, $n_{\rm i,Si}$ is the intrinsic carrier concentration in unstrained-Si.

It is important to consider the effect of strain on the built-in voltage across the source–body and drain–body junctions in strained-Si thin film, which can be written as

$$V_{\rm bi,s-Si} = V_{\rm bi,Si} + (\Delta V_{\rm bi})_{\rm s-Si}, \quad (5)$$

where

$$V_{\rm bi,Si} = \frac{E_{\rm g,Si}}{2q} + \phi_{\rm F,Si},$$
$$(\Delta V_{\rm bi})_{\rm s-Si} = \frac{-(\Delta E_{\rm g})_{\rm s-Si}}{q} - V_{\rm T}\ln\left(\frac{N_{V,\rm Si}}{N_{\rm V,s-Si}}\right).$$

3. Model formulation

3.1. Two-dimensional model for surface potential

The schematic structure of novel asymmetric DG FD strained-Si MOSFET is shown in Fig. 1.

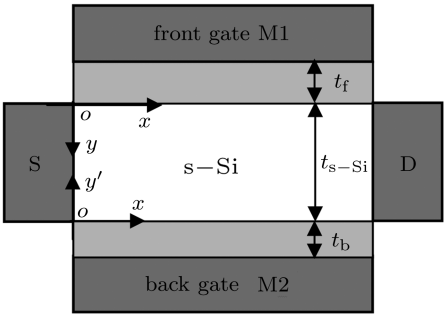


Fig. 1. Schematic structure of asymmetric DG FD strained-Si MOSFET.

Neglecting the effect of the fixed oxide charges on the electrostatics of the channel, we can write the Poisson equation of the potential distribution in the strained-Si layer before the onset of strong inversion as[14–17]

$$\frac{\partial^2\phi_1(x,y)}{\partial x^2} + \frac{\partial^2\phi_1(x,y)}{\partial y^2} = \frac{qN_{\rm A}}{\varepsilon_{\rm Si}}, \quad (0 \le x \le L, \quad 0 \le y \le t_{\rm s-Si}), \quad (6)$$

$$\frac{\partial^2\phi_2(x,y')}{\partial x^2} + \frac{\partial^2\phi_2(x,y')}{\partial y'^2} = \frac{qN_{\rm A}}{\varepsilon_{\rm Si}}, \quad (0 \le x \le L, \quad 0 \le y' \le t_{\rm s-Si}), \quad (7)$$

where $N_{\rm A}$ is the doping concentration of strained-Si layer, $\varepsilon_{\rm Si}$ is the dielectric constant of strained-Si layer, $t_{\rm s-Si}$ is the thickness of strained-Si layer. The x axis is parallel to the channel, and y axis is perpendicular to the channel. The potential profile in the vertical direction in the strained-Si film can be approximated by parabolic functions.

$$\phi_1(x,y) = \phi_{\rm s}(x) + c_{11}(x)y + c_{12}(x)y^2, \quad (0 \le x \le L, \quad 0 \le y \le t_{\rm s-Si}), \quad (8)$$

$$\phi_2(x,y) = \phi_{\rm b}(x) + c_{21}(x)y' + c_{22}(x)y'^2, \quad (0 \le x \le L, \quad 0 \le y' \le t_{\rm s-Si}), \quad (9)$$

where $\phi_{\rm s}(x)$ and $\phi_{\rm b}(x)$ represent the surface potential of the front channel and the surface potential of back channel at the gate-oxide/strained-Si interface under M1, M2, respectively. These coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$ and $c_{22}(x)$ are functions of x. The Poisson equation can be solved by using the following boundary conditions.

1) Electric flux (displacement) at the gate-oxide/strained-Si layer interface of the front gate is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=0} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}}\frac{\phi_{\rm S}(x)-V'_{\rm GS1}}{t_{\rm f}}, \tag{10}$$

$$\left.\frac{\mathrm{d}\phi_2(x,y')}{\mathrm{d}y'}\right|_{y'=t_{\rm s-Si}} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}}\frac{V'_{\rm GS1}-\phi_2(x,t_{\rm s-si})}{t_{\rm f}}, \tag{11}$$

where $\varepsilon_{\rm ox}$ is the dielectric constant of the gate oxide, $t_{\rm f}$ is the gate-oxide thickness, $V_{\rm GS}$ is the gate-to-source bias voltage, $V'_{\rm GS1} = V_{\rm GS} - (V_{\rm FB1,f})_{\rm s-Si}$.

2) Electric flux (displacement) at the gate-oxide/strained-Si layer interface of the back gate is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=t_{\rm s-Si}} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}}\frac{V'_{\rm GS2}-\phi_1(x,t_{\rm s-Si})}{t_{\rm b}}, \tag{12}$$

$$\left.\frac{\mathrm{d}\phi_2(x,y')}{\mathrm{d}y'}\right|_{y'=0} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}}\frac{\phi_0(x)-V'_{\rm GS2}}{t_{\rm b}}, \tag{13}$$

where $t_{\rm b}$ is the buried-oxide thickness, $V'_{\rm GS2} = V_{\rm GS} - (V_{\rm FB2,f})_{\rm s-Si}$.

3) The channel potential at the source side must be equal to the built-in potential of the junction of source and body,

$$\phi_1(0,0) = \phi_{\rm S}(0) = V_{\rm bi,s-Si} = \phi_{\rm b}(0) = \phi_2(0,0). \tag{14}$$

4) The channel potential at the drain side must be equal to the built-in potential of the junction of source and body plus the drain-to-source bias voltage,

$$\phi_1(L,t_{\rm s-Si}) = V_{\rm bi,s-Si} + V_{\rm DS} = \phi_2(L,t_{\rm s-Si}), \tag{15}$$

where $V_{\rm DS}$ is the drain-to-source bias voltage.

Using the boundary conditions (10), (11), (12) and (13), one can obtain the coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$, $c_{22}(x)$ in Eqs. (9) and (10), and obtain the expressions for $\phi_1(x,y)$ and $\phi_2(x,y)$. Substituting $\phi_1(x,y)$ and $\phi_2(x,y)$ into Eqs. (6) and (7) respectively and substituting $y=0$, we can obtain

$$\frac{\mathrm{d}^2\phi_{\rm S}(x)}{\mathrm{d}x^2} - \alpha_1^2\phi_{\rm S}(x) = \beta_1, \tag{16}$$

$$\frac{\mathrm{d}^2\phi_{\rm b}(x)}{\mathrm{d}x^2} - \alpha_2^2\phi_{\rm b}(x) = \beta_2, \tag{17}$$

where

$$\alpha_1^2 = \frac{\varepsilon_{\rm ox}(a_1t_{\rm b}+t_{\rm f}+t_{\rm b})}{\varepsilon_{\rm Si}t_{\rm f}t_{\rm si}t_{\rm b}\left(1+\frac{1}{2}a_1\right)},$$

$$\beta_1 = \frac{qN_{\rm A}}{\varepsilon_{\rm Si}} - \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}}\frac{t_{\rm f}V'_{\rm GS,b}+(t_{\rm b}+a_1t_{\rm b})V'_{\rm GS,f}}{t_{\rm f}t_{\rm si}t_{\rm b}\left(1+\frac{1}{2}a_1\right)},$$

$$\alpha_2^2 = \frac{\varepsilon_{\rm ox}(a_2t_{\rm f}+t_{\rm f}+t_{\rm b})}{\varepsilon_{\rm Si}t_{\rm f}t_{\rm si}t_{\rm b}\left(1+\frac{1}{2}a_2\right)},$$

$$\beta_2 = \frac{qN_{\rm A}}{\varepsilon_{\rm si}} - \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}}\frac{t_{\rm b}V'_{\rm GS,f}+(t_{\rm f}+a_2t_{\rm f})V'_{\rm GS,b}}{t_{\rm f}t_{\rm si}t_{\rm b}\left(1+\frac{1}{2}a_2\right)}.$$

Here $a_1 = \varepsilon_{\rm ox}t_{\rm si}/\varepsilon_{\rm Si}t_{\rm b}$, $a_2 = \varepsilon_{\rm ox}t_{\rm si}/\varepsilon_{\rm Si}t_{\rm f}$.

The solutions of Eqs. (16) and (17), which are simple second-order non-homogenous differential equations with constant coefficients, can be written as

$$\phi_{\rm S}(x) = A\exp(\alpha_1x) + B\exp(-\alpha_1x) - \frac{\beta_1}{\alpha_1^2}, \tag{18}$$

$$\phi_{\rm b}(x) = C\exp(\alpha_2x) + D\exp(-\alpha_2x) - \frac{\beta_2}{\alpha_2^2}. \tag{19}$$

Using the boundary conditions (14), (15) to solve A, B, C and D, we can obtain

$$A = \frac{V_{\rm bi,s-S}+V_{\rm DS}-V_{\rm bi,s-S}\exp(-\alpha_1L)-(\beta_1/\alpha_1^2)(\exp(-\alpha_1L)-1)}{\exp(\alpha_1L)-\exp(-\alpha_1L)}, \tag{20}$$

$$B = \frac{V_{\rm bi,s-S}+V_{\rm DS}-V_{\rm bi,s-S}\exp(\alpha_1L)-(\beta_1/\alpha_1^2)(\exp(\alpha_1L)-1)}{\exp(-\alpha_1L)-\exp(\alpha_1L)}, \tag{21}$$

$$C = \frac{V_{\rm bi,s-S}+V_{\rm DS}-V_{\rm bi,s-S}\exp(-\alpha_2L)-(\beta_2/\alpha_2^2)(\exp(-\alpha_2L)-1)}{\exp(\alpha_2L)-\exp(-\alpha_2L)}, \tag{22}$$

$$D = \frac{V_{\rm bi,s-S}+V_{\rm DS}-V_{\rm bi,s-S}\exp(\alpha_2L)-(\beta_2/\alpha_2^2)(\exp(\alpha_2L)-1)}{\exp(-\alpha_2L)-\exp(\alpha_2L)}. \tag{23}$$

The minimum potential of the front-channel and back-channel can be calculated from Eqs. (18) and (19).

$$\phi_{\rm s,min} = 2\sqrt{AB} - \frac{\beta_1}{\alpha_1^2}, \tag{24}$$

$$\phi_{\rm b,min} = 2\sqrt{CD} - \frac{\beta_2}{\alpha_2^2}. \tag{25}$$

The minimum occurs at

$$x_{\min,\mathrm{f}} = \frac{1}{2\alpha_1}\ln\left(\frac{B}{A}\right), \tag{26}$$

$$x_{\min,\mathrm{b}} = \frac{1}{2\alpha_2}\ln\left(\frac{D}{C}\right). \tag{27}$$

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field horizontal components under the front gate and back gate are given by

$$E_{1,\mathrm{f}}(x) = A\alpha_1\exp(\alpha_1 x) - B\alpha_1\exp(-\alpha_1 x), \tag{28}$$

$$E_{2,\mathrm{b}}(x) = C\alpha_2\exp(\alpha_2 x) - D\alpha_2\exp(-\alpha_2 x). \tag{29}$$

3.2. Two-dimensional model for threshold voltage

The threshold voltage V_{TH} is the value of the gate voltage V_{GS} at which a conducting channel of SOI MOSFET is induced. In a fully depleted thin film SOI MOSFET, it is desirable that the front channel turns on before the back channel. Therefore, the threshold voltage is taken to be the value of gate source voltage. The $\phi_{\mathrm{s,min}} = 2\phi_{\mathrm{F,si}}$, where $\phi_{\mathrm{F,si}}$ is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. For the strained-Si SOI MOSFET, the threshold condition under the front gate is modified as

$$\phi_{\mathrm{s,min}} = 2\phi_{\mathrm{F,Si}} + \Delta\phi_{\mathrm{s-Si}} = \phi_{\mathrm{th}}, \tag{30}$$

where

$$\Delta\phi_{\mathrm{s-Si}} = -\frac{(\Delta E_{\mathrm{g}})_{\mathrm{s-Si}}}{q} + V_{\mathrm{T}}\ln\left(\frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s-Si}}}\right),$$

ϕ_{th} is the value of surface potential at which the volumetric inversion electron charge density in the strained-Si device is the same as that in the unstrained-Si, i.e., equal to the body doping.

In the case of asymmetric DG structure, due to the coexistence of different metal M1, M2, t_{f}, t_{b}, the threshold voltage is defined as the value of V_{GS} at which the minimum surface potential of the front channel $\phi_{\mathrm{s,min}}$ equals ϕ_{th}, or the minimum surface potential of the back channel $\phi_{\mathrm{s,min}}$ equals ϕ_{th}. Hence, we can determine the value of threshold voltage as the value of V_{GS} by solving Eqs. (24) and (25). The threshold voltage of the front gate can be expressed as follows:

$$V_{\mathrm{TH,f}} = \left[-\left(\frac{-b_{\mathrm{f}} + \sqrt{b_{\mathrm{f}}^2 - 4a_{\mathrm{f}}c_{\mathrm{f}}}}{2a_{\mathrm{f}}}\right) + \frac{qN_{\mathrm{A}}}{\alpha_1^2\varepsilon_{\mathrm{si}}}\right] + \frac{t_{\mathrm{f}}(V_{\mathrm{FB2,f}})_{\mathrm{s-Si}} + (t_{\mathrm{b}} + a_1 t_{\mathrm{b}})(V_{\mathrm{FB1,f}})_{\mathrm{s-Si}}}{(t_{\mathrm{b}} + a_1 t_{\mathrm{b}} + t_{\mathrm{f}})}, \tag{31}$$

where

$$\begin{aligned}
a_{\mathrm{f}} &= \frac{1}{4} - \frac{(\exp(-\alpha_1 L) - 1)(\exp(\alpha_1 L) - 1)}{(\exp(-\alpha_1 L) - \exp(\alpha_1 L))(\exp(\alpha_1 L) - \exp(-\alpha_1 L))},\\
b_{\mathrm{f}} &= \frac{1}{2}\phi_{\mathrm{th}} - \frac{(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi,s-S}}\exp(\alpha_1 L))(\exp(-\alpha_1 L) - 1)}{(\exp(-\alpha_1 L) - \exp(\alpha_1 L))(\exp(\alpha_1 L) - \exp(-\alpha_1 L))}\\
&\quad + \frac{(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi,s-S}}\exp(-\alpha_1 L))(\exp(\alpha_1 L) - 1)}{(\exp(-\alpha_1 L) - \exp(\alpha_1 L))(\exp(\alpha_1 L) - \exp(-\alpha_1 L))},\\
c_{\mathrm{f}} &= \frac{1}{4}\phi_{\mathrm{th}}^2 - \frac{(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi,s-S}}\exp(\alpha_1 L))(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi,s-S}}\exp(-\alpha_1 L))}{(\exp(-\alpha_1 L) - \exp(\alpha_1 L))(\exp(\alpha_1 L) - \exp(-\alpha_1 L))}.
\end{aligned}$$

The threshold voltage of the back gate can be expressed as follows:

$$V_{\mathrm{TH,b}} = \left[-\left(\frac{-b_{\mathrm{b}} + \sqrt{b_{\mathrm{b}}^2 - 4a_{\mathrm{b}}c_{\mathrm{b}}}}{2a_{\mathrm{b}}}\right) + \frac{qN_{\mathrm{A}}}{\alpha_2^2\varepsilon_{\mathrm{si}}}\right] + \frac{t_{\mathrm{b}}(V_{\mathrm{FB1,f}})_{\mathrm{s-Si}} + (t_{\mathrm{f}} + a_2 t_{\mathrm{f}})(V_{\mathrm{FB2,f}})_{\mathrm{s-Si}}}{(t_{\mathrm{b}} + a_2 t_{\mathrm{f}} + t_{\mathrm{f}})}, \tag{32}$$

where

$$\begin{aligned}
a_{\mathrm{b}} &= \frac{1}{4} - \frac{(\exp(-\alpha_2 L) - 1)(\exp(\alpha_2 L) - 1)}{(\exp(-\alpha_2 L) - \exp(\alpha_2 L))(\exp(\alpha_2 L) - \exp(-\alpha_2 L))},\\
b_{\mathrm{b}} &= \frac{1}{2}\phi_{\mathrm{th}} - \frac{(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi.,s-S}}\exp(\alpha_2 L))(\exp(-\alpha_2 L) - 1)}{(\exp(-\alpha_2 L) - \exp(\alpha_2 L))(\exp(\alpha_2 L) - \exp(-\alpha_2 L))}\\
&\quad + \frac{(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi,s-S}}\exp(-\alpha_2 L))(\exp(\alpha_2 L) - 1)}{(\exp(-\alpha_2 L) - \exp(\alpha_2 L))(\exp(\alpha_2 L) - \exp(-\alpha_2 L))},\\
c_{\mathrm{b}} &= \frac{1}{4}\phi_{\mathrm{th}}^2 - \frac{(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi,s-S}}\exp(\alpha_2 L))(V_{\mathrm{bi,s-S}} + V_{\mathrm{DS}} - V_{\mathrm{bi,s-S}}\exp(-\alpha_2 L))}{(\exp(-\alpha_2 L) - \exp(\alpha_2 L))(\exp(\alpha_2 L) - \exp(-\alpha_2 L))}.
\end{aligned}$$

The threshold voltage is the minimum value of threshold voltages of the front channel and the back channel,

$$V_{\rm TH} = \min[V_{\rm TH,f}, V_{\rm TH,b}]. \tag{33}$$

4. Results and discussions

To verify the proposed analytical models, an FD n-channel DG asymmetric structure is shown in Fig. 1. Typical values of work function for gate metals M1 and M2 are 4.35 eV and 4.70 eV, respectively. $t_{\rm f} = 1.5$ nm, $t_{\rm b} = 3$ nm, $t_{\rm s-Si} = 10$ nm, $N_{\rm A} = 1 \times 10^{17}$ cm^{-3}.

Figure 2 shows the surface potentials of the front gate and the back gate and the difference between them against the horizontal distance in the channel for $L = 20$ nm. It can be seen that the incorporation of asymmetric DG strained-Si design decreases the surface potential barriers of the front gate and the back gate surface for increasing effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer at the source and drain ends. However, in the middle of the channel there is an increase of the potential barrier for increasing effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer, as shown in Figs. 2(a) and 2(b). Figure 2(c) shows the difference between the surface potential of the front gate and the back gate, i.e. $\phi_{\rm b}(x) - \phi_{\rm S}(x)$. The $|\phi_{\rm b}(x) - \phi_{\rm S}(x)|$ increases with increasing effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer.

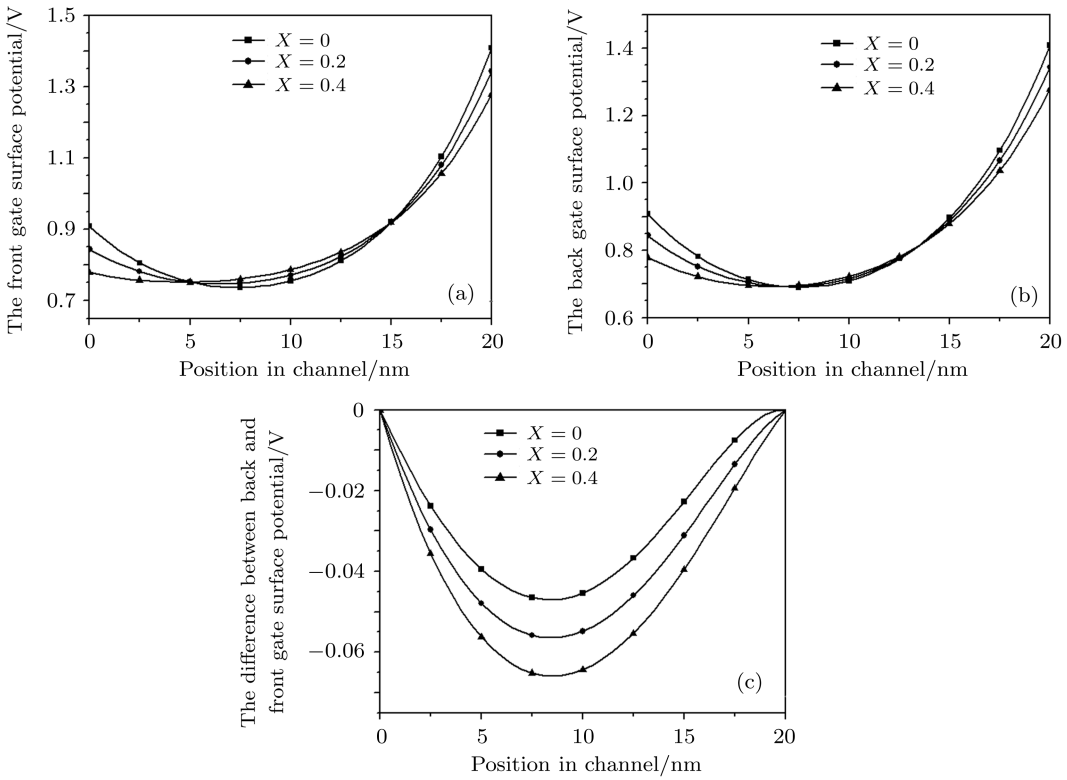


Fig. 2. Variation of surface potential of the front gate and the back gate along the channel for a 20 nm asymmetric DG strained-Si MOSFET with the position in the channel: (a) surface potential distribution of the front gate; (b) surface potential distribution of the back gate; (c) difference between the surface potentials of the front gate and the back gate.

For different effective Ge mole fraction in relaxed $Si_{1-x}Ge_x$ buffer ($x = 0$, $x = 0.2$ and $x = 0.4$), Fig. 3 shows the surface electric fields of the front gate and the back gate variation along the horizontal distance in the channel for $L = 20$ nm, respectively. The surface electric field increases with the increase of the horizontal distance to the source ends. It is also observed that the surface electric field increases with increasing effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer at the source ends. However, the surface electric field decreases with increasing effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer at the drain ends, as shown in Figs. 3(a) and 3(b).

Figure 4 shows the variation of the front gate and the back gate threshold voltage with strain X (Ge content in the relaxed SiGe layer) for a gate length of 20 nm. We can observe that the threshold voltages of the front

gate and the back gate almost decrease linearly with increasing strain, it even becomes negative for Ge content of 0.3–0.4. The threshold voltage decreases with increasing Ge content X very significantly. It can be attributed to the decrease of the flatband voltage, decrease of the source–body/drain–body built-in potential barrier, and an earlier inversion due to a decrease in $\phi_{\rm th}$.

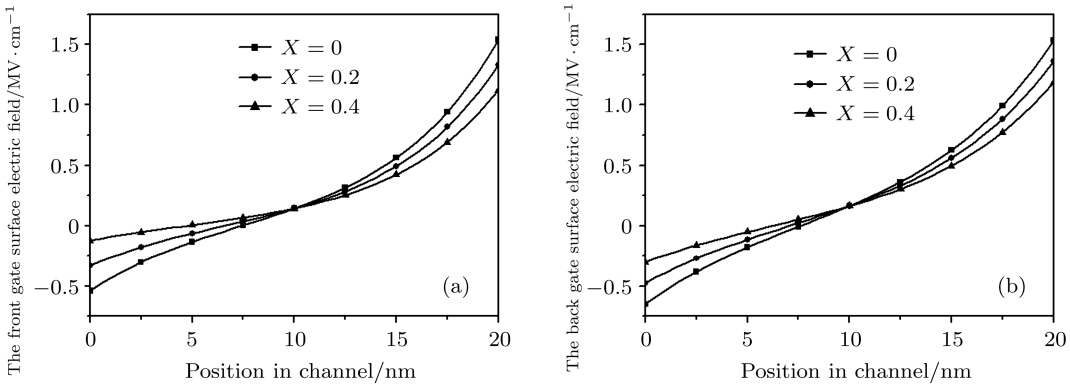


Fig. 3. Variation of the surface electric field along the channel for a 20 nm asymmetric DG MOSFET as a function of Ge mole fraction in relaxed SiGe buffer: (a) electric field distribution of the front gate surface; (b) electric field distribution of the back gate surface.

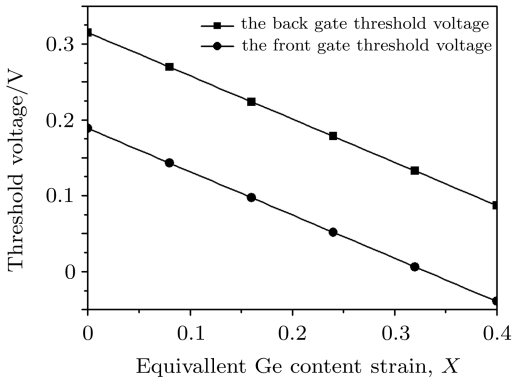


Fig. 4. Variation of threshold voltages of the front gate and the back gate with strain X (Ge component in relaxed SiGe buffer).

Figure 5 shows variation of threshold voltage with the gate length for different Ge mole fraction. It is observed that SCE become serious with decreasing channel length. It is also observed that the threshold voltage is lower for higher strain in the silicon film for given channel length. The change for increasing Ge content X is due to the decrease of the flatband voltage, decrease in the built-in potential barrier, and an earlier inversion due to a decrease in $\phi_{\rm th}$. The threshold voltage of the front gate is smaller than that of the back gate. So the threshold voltage is equal to the threshold voltage of the front gate.

Figure 6 shows the variation of drain induced barrier lowering (DIBL) with channel length for Ge mole fraction $X = 0.2$ for asymmetric DG FD strained-Si MOSFET. The DIBL is obtained from the difference between the threshold voltage at high drain-drain source voltage ($V_{\rm ds} = 0.5$ V) and the threshold voltage at low drain-drain source voltage ($V_{\rm ds} = 0.05$ V). It is observed that DIBL is remarkable for the short channel length, while it can be negligible for the long channel length.

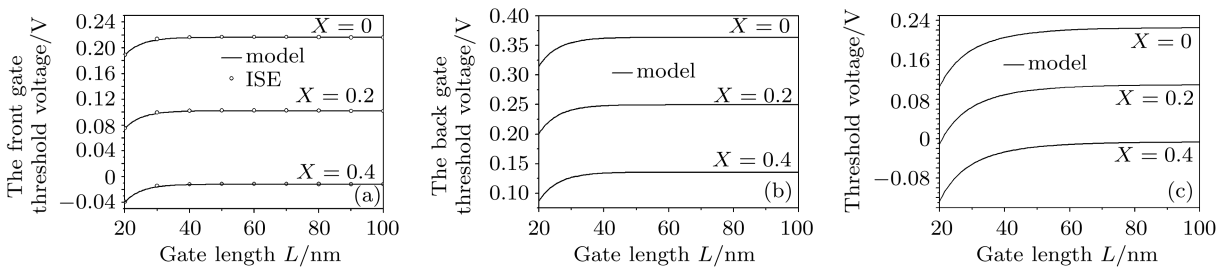


Fig. 5. Variation of threshold voltage along the channel for asymmetric DG MOSFET as a function of Ge mole fraction in relaxed SiGe buffer: (a) threshold voltage of front gate; (b) threshold voltage of back gate; (c) threshold voltage of planar device.

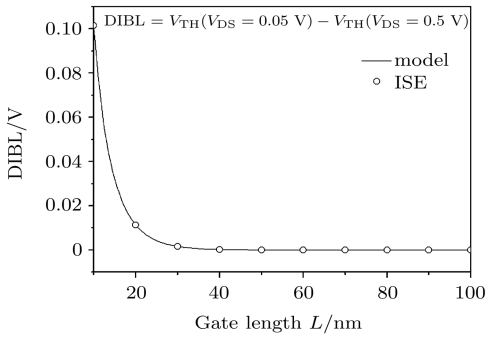


Fig. 6. The DIBL versus the channel length L.

5. Conclusion

Based on the two-dimensional solution of Poisson equation, we present the analytical models for asymmetric DG FD strained-Si MOSFET including the surface potential, surface electric field and threshold voltage. It is shown that the asymmetric DG FD strained-Si MOSFET can reduce SCE and DIBL. The obtained model results are in good agreement with the simulation results.

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