Rapid Communication

Development and characteristic analysis of a field-plated Al_2O_3/AlInN/GaN MOS–HEMT*

Mao Wei(毛 维)[a)†], Yang Cui(杨 翠)[b)], Hao Yao(郝 跃)[a)],
Zhang Jin-Cheng(张进成)[a)], Liu Hong-Xia(刘红侠)[a)], Bi Zhi-Wei(毕志伟)[a)],
Xu Sheng-Rui(许晟瑞)[a)], Xue Jun-Shuai(薛军帅)[a)], Ma Xiao-Hua(马晓华)[a)], Wang Chong(王 冲)[a)],
Yang Lin-An(杨林安)[a)], Zhang Jin-Feng(张金风)[a)], and Kuang Xian-Wei(匡贤伟)[a)]

[a)] *Key Lab of the Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an* 710071, *China*
[b)] *School of Technical Physics, Xidian University, Xi'an* 710071, *China*

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We present an AlInN/AlN/GaN MOS–HEMT with a 3 nm ultra-thin atomic layer deposition (ALD) Al_2O_3 dielectric layer and a 0.3 μm field-plate (FP)-MOS–HEMT. Compared with a conventional AlInN/AlN/GaN HEMT (HEMT) with the same dimensions, a FP-MOS–HEMT with a 0.6 μm gate length exhibits an improved maximum drain current of 1141 mA/mm, an improved peak extrinsic transconductance of 325 mS/mm and effective suppression of gate leakage in both the reverse direction (by about one order of magnitude) and the forward direction (by more than two orders of magnitude). Moreover, the peak extrinsic transconductance of the FP-MOS–HEMT is slightly larger than that of the HEMT, indicating an exciting improvement of transconductance performance. The sharp transition from depletion to accumulation in the capacitance–voltage (C–V) curve of the FP-MOS–HEMT demonstrates a high-quality interface of Al_2O_3/AlInN. In addition, a large off-state breakdown voltage of 133 V, a high field-plate efficiency of 170 V/μm and a negligible double-pulse current collapse is achieved in the FP-MOS–HEMT. This is attributed to the adoption of an ultra-thin Al_2O_3 gate dielectric and also of a field-plate on the dielectric of an appropriate thickness. The results show a great potential application of the ultra-thin ALD-Al_2O_3 FP-MOS–HEMT to deliver high currents and power densities in high power microwave technologies.

Keywords: field-plate, ultra-thin Al_2O_3 gate dielectric, FP-MOS–HEMT, atomic layer deposited
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1. Introduction

The AlInN/GaN-based high electron mobility transistor (HEMT) is an excellent alternative to the AlGaN/GaN HEMT in high-power, high-frequency applications, and has recently attracted great attention not only due to the formation of a high density two-dimensional electron gas (2DEG) at the AlInN/GaN interface, but also because of the possibile fabrication of more reliable strain-free devices.[1,2] According to theoretical calculations, an AlInN/GaN material system should exhibit a quantum well polarization-induced charge 2–3 times higher than that found in conventional AlGaN/GaN material systems,[1] which can lead to a significant improvement in power performance. Recently, an AlInN/GaN HEMT heterostructure grown on a sapphire substrate with a 2DEG density of 3.4×10^{13} cm^{-2} has been reported.[3] An AlInN/GaN HEMT on SiC with 10 W/mm and a 50% power-added efficiency (PAE) at 10 GHz has also been created.[4] However, many actual and important problems, which restrict the high-voltage/high-power operation of AlInN/GaN high power electronics are still not satisfactorily resolved, such as the low Schottky barrier height,[5] the high reverse leakage current of the Schottky contact and the presence of trap,[6] imperfectness in the fabrication of devices and difficulties with the epitaxial technique.[7] This can lead to a reduction of the forward gate bias, a decrease of the breakdown voltage and a deterioration of the current collapse in an AlInN/GaN-based HEMT. The insulation gate

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†Corresponding author. E-mail: mwxidian@126.com
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technique, where Al_2O_3 is used as the gate dielectric to form Al_2O_3/AlInN/GaN MOS–HEMTs,[8] is a promising approach to overcoming these issues. However, the insertion of such a layer, making the gate-to-channel separation larger, might significantly degrade the aspect ratio. This could cause a deteriorations in device performance such as transconductance. Thus it is necessary to make the gate dielectric layer as thin as possible, or adopt another dielectric of much higher permittivity such as ZrO_2 or HfO_2 in the AlInN/GaN-based MOS–HEMT.[9] Although the insulation gate technique is capable of reducing gate leakage to some extent, it does not alleviate electrical field crowding at the drain-side of the gate edge.[10] Breakdowns of a AlInN/GaN-based MOS–HEMT still tend to occur near the gate due to the high electrical field. Thus, a field-plate (FP) technique,[11−13] which is effective in modulating the electric field distribution along a channel, may be required to increase the breakdown voltage in high power applications. The efficacy of the FP technique has been demonstrated in the latest papers about conventional Schottky gate AlInN/GaN-based HEMTs.[4,14,15] Nevertheless, few investigations of AlInN/GaN-based HEMTs with both a gate dielectric layer and a FP have been carried out thus far. This field deserves further investigation.

In this paper, the fabrication and electrical performance of an ultra-thin-Al_2O_3/$Al_{0.85}In_{0.15}N$/AlN/GaN MOS–HEMT with a 0.3 μm FP (FP-MOS–HEMT) is demonstrated. Ultra-thin Al_2O_3 of 3 nm, used as the gate dielectric, was deposited using atomic layer deposition (ALD). With the insertion of an Al_2O_3 layer under the gate, both the forward gate leakage and the reverse gate leakage were reduced remarkably, and the transfer characteristics, as well as the transconductance characteristics, improved significantly compared with those of the conventional $Al_{0.85}In_{0.15}N$/AlN/GaN HEMT. Off-state three-terminal breakdown measurements show a pronounced improvement in the breakdown voltage of the FP-MOS–HEMT due to the adoption of a FP on the dielectric of appropriate thickness. Double-pulse measurements demonstrated the effective suppression of current collapse in the FP-MOS–HEMT. In addition, the phenomenon that the peak extrinsic transconductance of the FP-MOS–HEMT is increased slightly compared with that of the HEMT, was observed. This is different from the results in another report on Al_2O_3/AlInN/AlN/GaN MOS–HEMT.[8]

2. Device fabrication

The epilayer structure of the device used in this study was grown by metal–organic chemical vapour deposition (MOCVD) on a *c*-plane sapphire substrate. It is composed of a 2 μm insulating GaN buffer layer followed by a 1-nm-thick AlN interlayer and a 12 nm undoped $Al_{0.85}In_{0.15}N$ layer with an In content of around 15%. With this In content, AlInN grown on GaN is near-lattice-matched and almost without strain. The room-temperature Hall mobility and the sheet 2DEG density were 1503 $cm^2/(V{\cdot}s)$ and $1.49{\times}10^{13}$ cm^{-2}, respectively.

Figure 1 shows the cross section of the 3nm-Al_2O_3/AlInN/AlN/GaN FP-MOS–HEMT. For this study, the first step of the device fabrication was to make a mesa isolation using Cl_2 plasma in a reactive ion etch (RIE) system. The second step was to anneal the e-beam evaporated Ti/Al/Ni/Au at 850 °C for 30 s in a N_2 ambient to realize the ohmic contact. A contact resistance of 0.4 $\Omega{\cdot}$mm was achieved. The drain–source distance was 3.5 μm. The third step was to deposit a 3 nm Al_2O_3 layer by ALD at 300 °C. Ni/Au/Ni deposited by e-beam evaporation was used as the gate metal. The distance of the gate from the source contact was 0.7 μm. The final step was to deposit a 55-nm-thick silicon nitride (SiN) layer using a PECVD system. A field-plate was formed with e-beam evaporated Ti/Au on the top of the silicon nitride layer, this completed the process of fabricating the 3 nm-Al_2O_3/AlInN/AlN/GaN FP-MOS–HEMT.

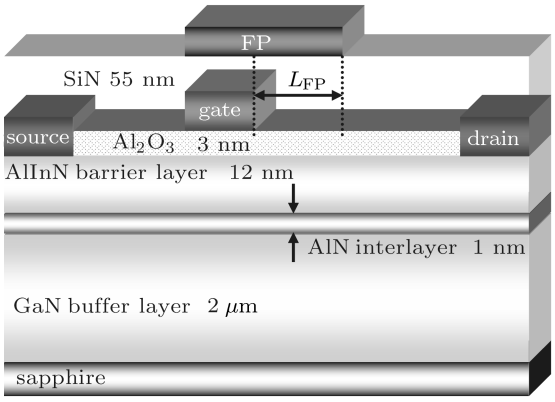


Fig. 1. Cross section of the 3nm-Al_2O_3/AlInN/AlN/GaN FP-MOS–HEMT.

The FP was connected electrically to the gate through the metal pads and the effective length L_{FP} of the FP was 0.3 μm. The gate length and width were 0.6 μm and 100 μm respectively. For comparison, a conventional AlInN/AlN/GaN HEMT with the

same dimensions as the FP-MOS–HEMT, but without a passivation layer and FP, was fabricated at the same time.

3. Results and discussion

Figure 2 shows the C–V measurements at 1 MHz of the gate capacitors of the HEMT and the FP-MOS–HEMT with a diameter of 130 μm. A sharp transition from the depletion region to the accumulation region in the profile of the FP-MOS–HEMT, which is similar to that of the HEMT, can be observed, which demonstrates a high-quality interface between the Al_2O_3 and the AlInN. In the accumulation region, the total capacitance can be expressed as $1/C_{\text{FP-MOS-HEMT}} = 1/C_{\text{ox}}+1/C_{\text{HEMT}}$, where $C_{\text{FP-MOS-HEMT}} = 76.8$ pF and $C_{\text{HEMT}} = 95.1$ pF are the zero-bias capacitances of the FP-MOS–HEMT and HEMT respectively. Thus, the zero-bias capacitance of the Al_2O_3 layer, C_{ox}, can be calculated to be 399 pF. The dielectric constant ε_{OX} of Al_2O_3 is found to be 10 (using the thinkness $d_{\text{OX}} = 3$ nm for the Al_2O_3 layer), which is typical for Al_2O_3 prepared by ALD.[16] I–V characteristics of the gate–source Schottky diode in the HEMT and the gate–source MOS structure in the FP-MOS–HEMT with the same dimensions are shown in the inset of Fig. 2. Effective suppression of gate leakage current can be observed in the FP-MOS–HEMT when compared with the HEMT. The gate leakage current is suppressed by about one order of magnitude in the reverse direction ($V_{\text{GS}} = -15$ V), while it is suppressed by more than two orders of magnitude in the forward direction ($V_{\text{GS}} = 2$ V). This indicates a great improvement in the two-terminal breakdown voltage of the FP-MOS–HEMT.

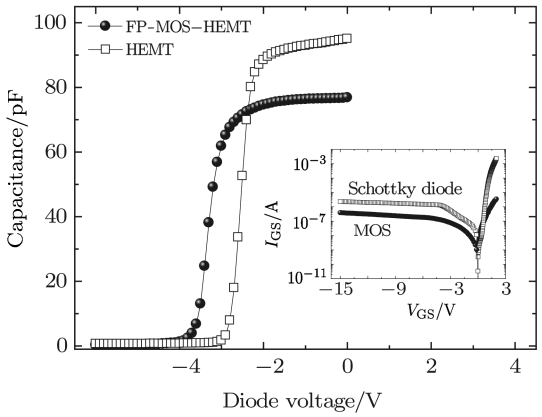


Fig. 2. C–V curves at 1 MHz on the gate capacitors of the HEMT and the FP-MOS–HEMT with a diameter of 130μm. The inset shows the I–V characteristics of the gate Schottky diode and the gate Al_2O_3/HEMT MOS structures.

Figure 3 shows a comparison of the transfer characteristic between the HEMT and the FP-MOS–HEMT. It can be seen that the maximum I_{DS} of the HEMT is limited to 836 mA/mm at $V_{\text{GS}} = 1$ V due to the large forward gate leakage current, but that of the FP-MOS–HEMT can reach 1141 mA/mm at a gate bias of 3 V. Moreover, the FP-MOS–HEMT always exhibits a higher I_{DS} than the HEMT at the same V_{GS}. This is probably due to the surface passivation effect of the Al_2O_3 layer, leading to an increase in channel carrier concentration by passivating the surface traps.[17] It also clearly demonstrates the superiority of the HEMT with surface passivation using an Al_2O_3 dielectric. In this paper, the pinch-off voltage is defined as the gate bias intercept of the extrapolation of the drain current at the point of peak transconductance. Thus, the pinch-off voltages of the HEMT and the FP-MOS–HEMT are –3 V and –3.8 V respectively, indicating a small shift $\Delta V_T = -0.8$ V of the pinch-off voltage in the FP-MOS–HEMT. This negative shift is attributed to a decrease in gate barrier capacitance, and it is in good agreement with the value obtained from the formula $\Delta V_T = V_{\text{PO}} d_{\text{OX}} \varepsilon_{\text{AlInN}}/(d_{\text{AlInN}} \varepsilon_{\text{OX}})$,[9] neglecting the AlN spacer, where V_{PO} denotes the conventional HEMT pinch-off voltage, d_{AlInN} and $\varepsilon_{\text{AlInN}}$ denote the thickness and the permittivity of the AlInN layer respectively. This also indicates that it is a high-quality Al_2O_3/AlInN interface with few interface states.[9]

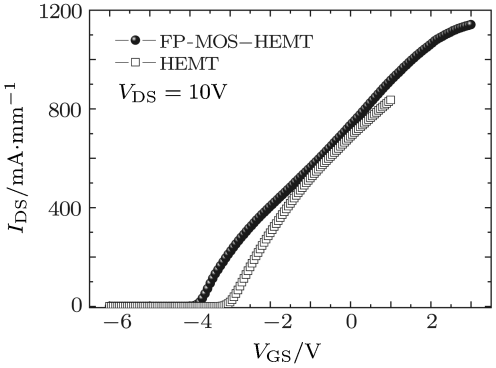


Fig. 3. Comparison of the transfer characteristics of the HEMT and the FP-MOS–HEMT.

Figure 4 shows the transconductance characteristics as a function of gate bias for both the HEMT and the FP-MOS–HEMT at $V_{\text{DS}} = 10$ V. Unlike the results reported in Ref. [8] for the AlInN/AlN/GaN MOS–HEMT with a Al_2O_3 gate dielectric layer of 5 nm, the peak extrinsic transconductance G_{m} of 325 mS/mm found in the FP-MOS–HEMT is slightly larger than that of 318 mS/mm found in the HEMT,

indicating a considerable and exciting improvement of transconductance performance in the FP-MOS–HEMT. A similar phenomenon was also observed in Ref. [9] on the AlInN/AlN/GaN MOS–HEMT with a ZrO_2 or HfO_2 gate dielectric. This could be explained as an improvement in intrinsic mobility due to a reduced surface depletion effect below the gate; leading to an improvement in the transconductance of the MOS–HEMT.[9]

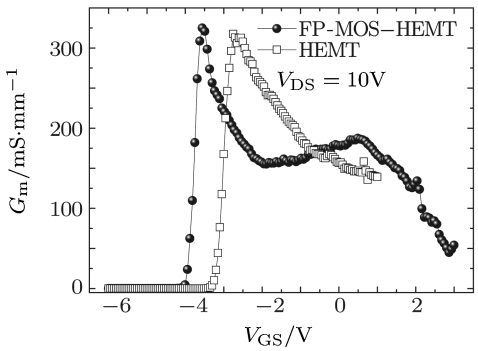


Fig. 4. Transconductance characteristics each as a function of the gate bias for HEMT and FP-MOS–HEMT at $V_{DS} = 10$ V.

Figure 5 shows the off-state three-terminal drain–source breakdown characteristics of the HEMT and the FP-MOS–HEMT, measured at gate voltage V_{GS} of –8 V. The breakdown voltage BV_{DS} is defined as the drain voltage at a gate current of 1 mA/mm, which is consistent with the rapidly increased currents caused by avalanche breakdown. The FP-MOS–HEMT with a 0.3 μm FP shows a breakdown voltage of 133 V, while the conventional HEMT indicates that the breakdown voltage is only 82V. In this paper, a new concept of FP efficiency, defined as a ratio of the increment of the breakdown voltage to the FP length, is introduced to describe the ability of the FP to improve the breakdown voltage. The breakdown voltage of the FP-MOS–HEMT has an increment of 51 V compared with that of the HEMT, and the FP efficiency is calculated to be approximately 170 V/μm, which is a very high value compared to anything ever achieved for the HEMTs currently available. To a certain extent, the high efficiency of the FP-MOS–HEMT is related to the utilization of the Al_2O_3 gate dielectric layer to reduce the leakage current. Furthermore, its high efficiency is attributed mainly to the adoption of both an Al_2O_3 layer (3 nm) and a SiN layer (55 nm) of an appropriate total thickness beneath the FP. This leads to a significant improvement in the ability of the FP to reduce the peak value of the electric field occuring at the drain-edge of the Schottky gate and to redistribute the electric field along the 2DEG channel in the gate–drain spacing.

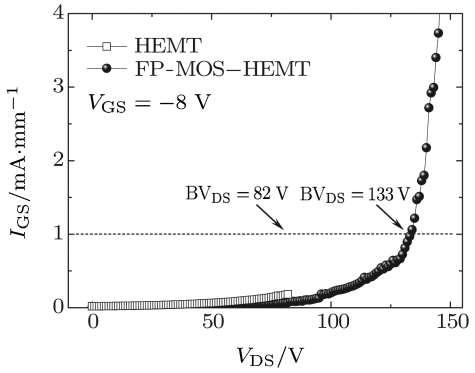


Fig. 5. Off-state three-terminal drain–source breakdown characteristics of the HEMT and the FP-MOS–HEMT.

Figure 6 shows DC and double-pulse current voltage measurements for the conventional HEMT (Fig. 6(a)) and the FP-MOS–HEMT (Fig. 6(b)). The gate voltage varies from –6 V to 1 V in steps of 1 V. The double-pulse measurements are carried out by pulsing both the drain–source voltage and the gate–source voltage synchronously away from the baseline bias points ($V_{GQ} = -8$ V, $V_{DQ} = 15$ V) to the points (V_{GS}, V_{DS}) where the current is measured. For these measurements, pulse width and pulse period are 500 ns and 0.1 ms, respectively. As can be seen, when compared with the DC measurement, the conventional HEMT shows a significant drain current collapse, while a negligible collapse is observed for the FP-MOS–HEMT. The remarkable reduction in current collapse for the FP-MOS–HEMT is attributed not only to the passivation effect of the Al_2O_3 layer on the surface state traps, but also to the modulation effect of the FP. The FP can modulate the direction of the longitudinal electric field, as well as the intensity distribution of transverse and longitudinal electric fields within the AlInN barrier layer, which can lead to an improvement in the ionization probability of the traps.[18] The results further confirm the superiority of Al_2O_3/AlInN/AlN/GaN MOS–HEMT with an FP in high power microwave applications.

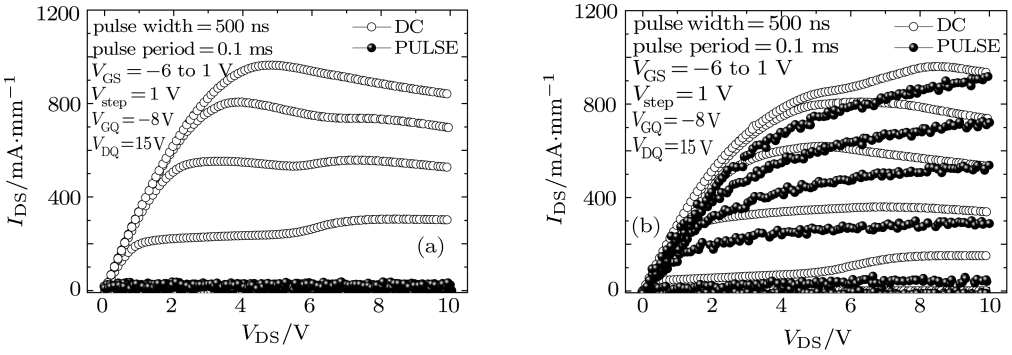


Fig. 6. DC and double-pulse current voltage measurements for conventional HEMT (a) and FP-MOS–HEMT (b).

4. Conclusions

A 3nm-Al_2O_3/$Al_{0.85}In_{0.15}N$/AlN/GaN MOS–HEMT with a 0.3 μm FP is fabricated and its characteristics are investigated. This FP-MOS–HEMT with a gate length of 0.6 μm exhibits a maximum drain current of 1141 mA/mm, a peak extrinsic transconductance of 325 mS/mm and reductions in the magnitude of the gate leakage by about one order in the reverse direction and by more than two orders in the forward direction. In addition, due to the adoption of the ultra-thin Al_2O_3 gate dielectric layer and the 0.3 μm FP on the dielectric layer with an appropriate thickness, the FP-MOS–HEMT shows a large off-state breakdown voltage of 133 V, a high FP efficiency of 170 V/μm and a negligible current collapse compared with the conventional HEMT. Moreover, a considerable and exciting improvement of transconductance performance, where by the peak extrinsic transconductance in the FP-MOS–HEMT is slightly larger than that in the HEMT, is achieved. All these excellent characteristics above demonstrate the great potential and superiority of the ultra-thin ALD-Al_2O_3 AlInN/AlN/GaN FP-MOS–HEMT for high-power and high-frequency applications.

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