An analytical model for coplanar waveguide on silicon-on-insulator substrate with conformal mapping technique*

He Da-Wei(何大伟)[a)b)], Cheng Xin-Hong(程新红)[a)†], Wang Zhong-Jian(王中健)[a)], Xu Da-Wei(徐大伟)[a)], Song Zhao-Rui(宋朝瑞)[a)], and Yu Yue-Hui(俞跃辉)[a)]

[a)] *State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai* 200050, *China*

[b)] *Graduate University of the Chinese Academy of Sciences, Beijing* 100049, *China*

(Received 12 June 2010; revised manuscript received 11 August 2010)

In this paper, the authors present an analytical model for coplanar waveguide on silicon-on-insulator substrate. The four-element topological network and the conformal mapping technique are used to analyse the capacitance and the conductance of the sandwich substrate. The validity of the model is verified by the full-wave method and the experimental data. It is found that the inductance, the resistance, the capacitance and the conductance from the analytical model show they are in good agreement with the corresponding values extracted from experimental *S*-parameter until 10 GHz.

Keywords: coplanar waveguide, silicon-on-insulator, conformal mapping

PACS: 02.60.–x, 72.60.+g, 84.40.–x **DOI:** 10.1088/1674-1056/20/1/010210

1. Introduction

As an essential passive device, coplanar waveguide plays an important role in the family of transmission lines. However, as the frequency increases, the substrate loss becomes high. Due to low resistivity, traditional bulk silicon substrate cannot suppress the attenuation. Thanks to the inserted oxide layer, silicon-on-insulator (SOI) structure can have several advantages over bulk silicon, these including lower parasitic capacitance, higher resistivity, suppressed short channel effect, and simplified process.[1] The SOI substrate was widely applied to complementary metal–oxide–semiconductor (CMOS), radio-frequency (RF) and microwave circuits, and even to passive devices.[2,3] Unfortunately, in the models about coplanar waveguide (CPW) on SOI substrate, the top silicon was usually oxidised in the process, and then the model of bulk silicon was used directly. According to simulation results as shown in Fig. 1, the existence of the top silicon could reduce the insertion loss, and the effect was significant with the frequency increasing, implying that the top silicon acted as an electric-field-shielding layer. However, the SOI substrate is staggered with insulated layers and semi-conductor layers, and it cannot be treated as an insulator layer or a semiconductor layer when the model for CPW on SOI substrate is considered. In order to solve this problem, the conformal mapping technique was used to design an equivalent resistance-capacitance (RC) lumped network. Comparing with full-wave method,[4] the conformal mapping technique can lead to an analytical solution in the closed form,[5] provide a satisfactory accuracy in a wide frequency band up to 20 GHz, and it is also suitable for modeling the electromagnetic mechanism of the coplanar waveguide on multi-layered substrate including the SOI substrate.

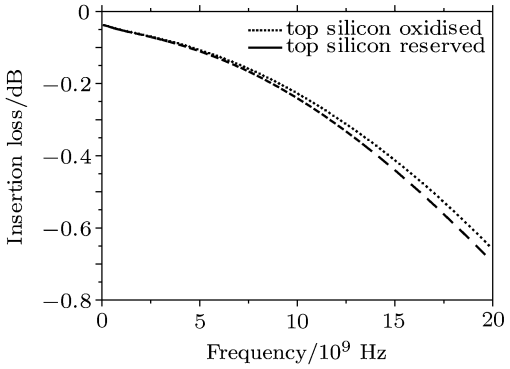


Fig. 1. Comparison of insertion loss between top silicon oxidised and top silicon reserved.

*Project supported by the National Natural Science Foundation of China (Grant No. 10775166), and the Zhejiang Provincial Science Technology Foundation, China (Grant No. 2008C31002).

†Corresponding author. E-mail: xh_cheng@mail.sim.ac.cn

© 2011 Chinese Physical Society and IOP Publishing Ltd

In this paper, an analytical model with a four-element equivalent circuit for the coplanar waveguide on SOI substrate is presented. This model can accurately analyse the relationship between the geometric structure and the performance of coplanar waveguide, and is suitable for device simulation and layout design. The rest of the present paper is organised as follows. In Section 2, the device structure and corresponding parameters are briefly presented, a four-element topological network is constructed to describe electrical properties, and equivalent elements are deduced with conformal mapping technique. In Section 3, the model validity is proved by comparing our results with results from the full-wave method and experiment results separately, and their deviations are discussed. Finally, in Section 4, main conclusions are drawn from the present study.

2. Physical model of CPW on SOI substrate

The structure to be discussed in this paper is shown in Fig. 2. The oxide isolation of SiO_2 layer separates the coplanar waveguide from the SOI substrate. The dielectric permittivity and the conductivity are ε_1 and σ_1 for SiO_2 layer, and they are ε_2 and σ_2 for Si layer, respectively.

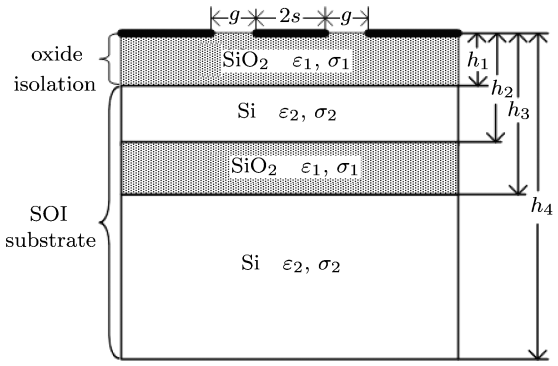


Fig. 2. Cross section of CPW on SOI substrate.

An equivalent circuit to illustrate the electromagnetic interrelationship between the CPW and the SOI substrate is shown in Fig. 3, where metal conductive loss is represented by a resistance (R) and an inductance (L), the energy storage and the energy loss associated with the transverse electric field and the transverse current are represented by equivalent dielectric capacitance (C) and equivalent substrate conductance (G).[6]

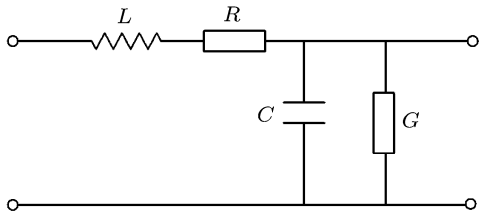
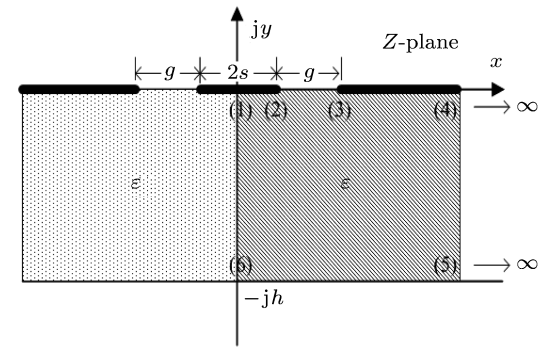


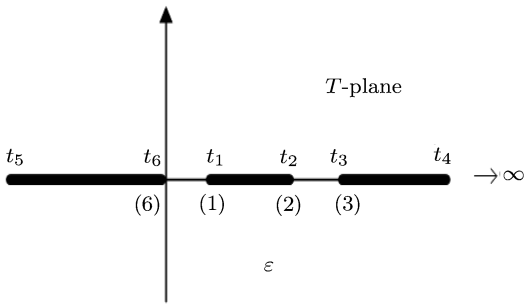
Fig. 3. Equivalent circuit of CPW on SOI substrate.

2.1. Conformal transformation

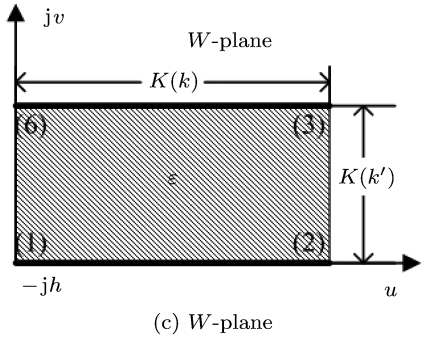
As shown in Fig. 4(a), the CPW can be treated as a symmetric structure. Suppose that two ground planes on both sides of the central conductor are extended to infinity and the thickness of SOI substrate is infinite.



(a) Z-plane



(b) T-plane



(c) W-plane

Fig. 4. Conformal transformation of CPW.

The magnetic field distribution around the central conductor is mostly perpendicular to the centerline of the structure, and a vertical magnetic wall lies in $Z = 0$ plane. Therefore, the whole substrate can be divided into two parts and each of them can be resolved in the same way as below.

The conformal transformation includes two steps.[7] Firstly, Schwartz–Christoffel transformation is used to map the right part of SOI substrate:

$$t = \cosh^2\left(\frac{\pi \cdot Z}{2h}\right), \quad \text{where} \quad Z = x + jy. \tag{1}$$

As shown in Figs. 4(a) and 4(b), t_1, t_2, t_3, t_4, t_5 and t_6 can be expressed as

$$t_1 = \cosh^2(0) = 1, \quad t_2 = \cosh^2\left(\frac{\pi s}{2h}\right),$$
$$t_3 = \cosh^2\left(\frac{\pi(s+g)}{2h}\right), \tag{2}$$
$$t_4 = t_5 = \infty,$$
$$t_6 = \cosh^2\left(\frac{\pi \cdot (-jh)}{2h}\right) = 0. \tag{3}$$

Secondly, the lower part of the T-plane is transformed into a finite image internal Z domain by using the following Christoffel–Schwartz transformation as shown in Fig. 4(c):

$$W = u + \mathrm{j}v = K(k) + K(k') = \int_1^t \frac{A \cdot \mathrm{d}t}{\sqrt{t(t-t_3)(t-t_2)(t-t_1)}}, \tag{4}$$

where $K(k)$ is the complete elliptical integral of the first kind with modulus

$$k = \frac{\sinh\left(\frac{\pi \cdot s}{2h}\right)}{\sinh\left(\frac{\pi(s+g)}{2h}\right)}. \tag{5}$$

When $h \to \infty$, then $k \approx \dfrac{s}{s+g}$,
where

$$\frac{K(k)}{K(k')} \approx \begin{cases} \dfrac{1}{\pi}\ln\left[2\dfrac{1+\sqrt{k}}{1-\sqrt{k}}\right], & 0.707 \le k \le 1, \\ \dfrac{\pi}{\ln\left[2\dfrac{1+\sqrt{k'}}{1-\sqrt{k'}}\right]}, & 0 \le k \le 0.707, \end{cases} \tag{6}$$

with

$$k' = \sqrt{1-k^2}. \tag{7}$$

Therefore, the right half of the substrate is finally mapped into the closed region in W-plane, and three discrete parts of CPW are transformed into an integrated one. Thus the capacitance and the conductance of the SOI substrate can be calculated by the conformal mapping technique similarly.

2.2. Substrate capacitance

The results deduced in the previous section could be extended to a multilayer substrate structure. The multi-layer substrate is split into a several-single-layer substrate according to the physical layout and line geometry as shown in Fig. 5. Consequently, the total capacitance of CPW is the sum of the capacitances in parallel, and is deduced by conformal transformations:

in Fig. 5(a),

$$C_4 = 2\varepsilon_0\varepsilon_2 \frac{K(k_4)}{K(k_4')}, \tag{8}$$

in Fig. 5(b),

$$C_3 = 2\varepsilon_0(\varepsilon_1 - \varepsilon_2)\frac{K(k_3)}{K(k_3')}, \tag{9}$$

in Fig. 5(c),

$$C_2 = 2\varepsilon_0(\varepsilon_2 - \varepsilon_1)\frac{K(k_2)}{K(k_2')}, \tag{10}$$

in Fig. 5(d),

$$C_1 = 2\varepsilon_0(\varepsilon_1 - \varepsilon_2)\frac{K(k_1)}{K(k_1')}. \tag{11}$$

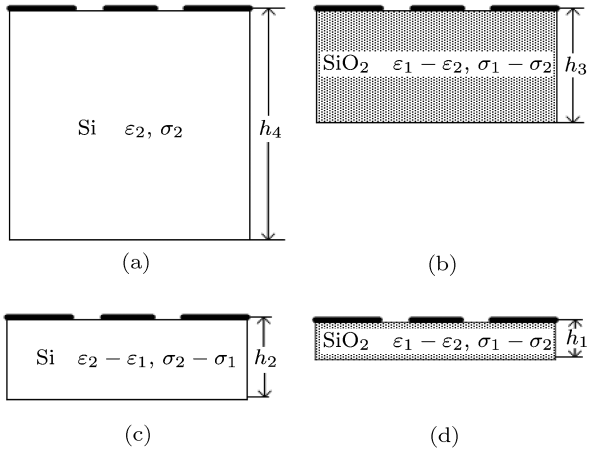


Fig. 5. Decomposition diagram of the substrate shown in Fig. 2.

In addition, the capacitance induced by air dielectric of upper part should be considered, and it can also be obtained by mapping it into a finite rectangular area in Z plane in the same way. And we use h_0 to describe the effect of the half plane above the

CPW structure in free space, where $h_0 \to \infty$, so the capacitance C_0 is expressed as

$$C_0 = 2\varepsilon_0 \frac{K(k_0)}{K(k_0')}, \tag{12}$$

with

$$k_0 = \frac{\sinh\left(\dfrac{\pi \cdot s}{2h_0}\right)}{\sinh\left[\dfrac{\pi \cdot (s+g)}{2h_0}\right]} |_{h_0 \to \infty} \approx \frac{s}{s+g}.$$

The total capacitance of CPW is the sum of the partial capacitances and the capacitance of the air-filled upper half space, i.e.,

$$C = C_0 + C_1 + C_2 + C_3 + C_4. \tag{13}$$

2.3. Substrate conductance

In semiconductor layers, dielectric loss and conductance loss were characterised by loss tangeng $\tan\delta_\varepsilon = \varepsilon_\varepsilon''/\varepsilon_\varepsilon'$ and $\tan\delta_0 = (\varepsilon_\sigma''/\varepsilon_\sigma') = \sigma/(\varepsilon_0\varepsilon'\omega)$ respectively, and the latter was transformed into $\sigma = \varepsilon_0\varepsilon'\omega\tan\delta_0$.[8] Note that σ is proportional to ε'. Assume that the total line losses are small and the quasi-transverse electronagnetic wave (TEM) approximation is suitable, then the conformal mapping technique will be used to evaluate the shunt conductance of the CPW on SOI substrate.

For SOI substrate, the SiO_2 dielectric layer can be treated as a semi-conductor layer with conductance $\sigma_1 \to 0$. Then, the substrate conductance in Fig. 5 can be expressed as follows:

for Fig. 5(a),

$$G_4 = 2\sigma_2 \frac{K(k_4)}{K(k_4')}, \tag{14}$$

for Fig. 5(b),

$$G_3 = 2(\sigma_1 - \sigma_2)\frac{K(k_3)}{K(k_3')}, \tag{15}$$

for Fig. 5(c),

$$G_2 = 2(\sigma_2 - \sigma_1)\frac{K(k_2)}{K(k_2')}, \tag{16}$$

for Fig. 5(d),

$$G_1 = 2(\sigma_1 - \sigma_2)\frac{K(k_1)}{K(k_1')}. \tag{17}$$

In view of the insulator of the air layer, the upper half plane effect on the whole substrate conductance is neglected, and the total substrate conductance is calculated as

$$G = G_1 + G_2 + G_3 + G_4. \tag{18}$$

The conductivity of SiO_2 layer σ_1=0 leads to

$$G = 2\sigma_2\left[\frac{K(k_4)}{K(k_4')} - \frac{K(k_3)}{K(k_3')} + \frac{K(k_2)}{K(k_2')} - \frac{K(k_1)}{K(k_1')}\right]. \tag{19}$$

2.4. Line inductance

The magnetic field profile of the present structure is nearly the same as that in the normal coplanar waveguide, so the line inductance L_s of CPW on SOI substrate can be described by the same expression as that on the bulk silicon substrate through using the conformal mapping technique,[9] i.e.,

$$L_s = \frac{1}{4c^2\varepsilon_0} \cdot \frac{K(k')}{K(k)}, \tag{20}$$

where $k = \frac{s}{s+g}$ and $k' = \sqrt{1-k^2}$.

2.5. Line resistance

At high frequency, the current density distribution within semi-infinite conductor is not uniform, and it is exponentially reduced from the surface to the centre, which is called skin effect. The skin depth can be expressed as

$$\delta_s = \frac{1}{\sqrt{\pi\mu_0\sigma f}}. \tag{21}$$

Line resistance and metal loss were deduced by conformal mapping technique in the same way.[10,11] For the line thickness $t < 3\delta_s$, a simple approximation can be used to estimate the effective sheet resistance:[12]

$$R_s = \frac{1}{\sigma\delta_s\{1 - \exp(-t/\delta_s)\}}. \tag{22}$$

3. Comparison between measurement and modeling

In order to validate suggested analytical model, the S parameters of the equivalent circuit of CPW on SOI substrate are compared with the S parameters calculated by Advanced Drainage System (ADS) Momentum where the full-wave method is employed. As shown in Fig. 6, the model can achieve the same accuracy as the full-wave method. Note that there exists some mismatch in the low frequency, which is due to the simplified substrate topology configuration.

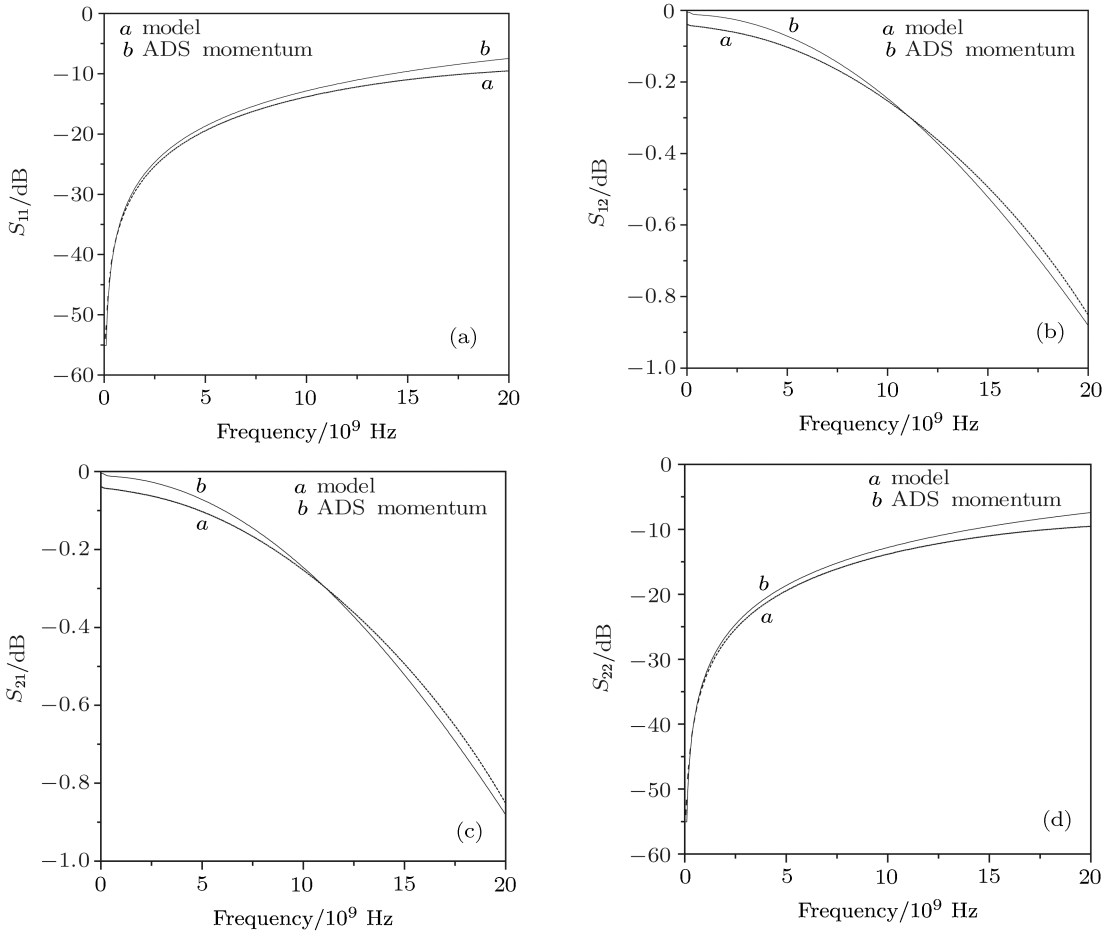


Fig. 6. Comparisons between S parameters : (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}, obtained from full-wave method and conformal mapping technique.

The values of equivalent elements, calculated by the model, are compared with the results extracted from the experimental data. The 1 μm oxide isolation layer was deposited on the SOI substrate with a conductivity of 0.02 S/m, then the 1 μm aluminum layer was sputtered and patterned to form CPW structures.

Then HP 8722D network analyser was used to measure S parameters of the CPW. Open-Short de-embedding technology was employed to de-embed the parasitic parameters.[13] The extracting values from de-embed S parameters are compared with those calculated from the model expressions (1)–(22).

The extraction process was discussed in detail in Ref. [14].

$$\mathrm{e}^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1}, \tag{23}$$

where

$$K = \left\{ \frac{\left(S_{11}^2 - S_{21}^2 + 1\right)^2 - \left(2S_{11}\right)^2}{\left(2S_{21}\right)^2} \right\}^{1/2}, \tag{24}$$

$$Z^2 = Z_0^2 \frac{\left(1 + S_{11}\right)^2 - S_{21}^2}{\left(1 - S_{11}\right)^2 - S_{21}^2} = \frac{(R + \mathrm{j}\omega L)}{(G + \mathrm{j}\omega C)}. \tag{25}$$

Then,

$$R = \mathrm{Re}\left\{\gamma Z\right\}, \tag{26}$$

$$L = \mathrm{Im}\left\{\gamma Z\right\}/\omega, \tag{27}$$

$$G = \mathrm{Re}\left\{\gamma Z\right\}, \tag{28}$$

$$C = \mathrm{Im}\left\{\gamma/Z\right\}/\omega. \tag{29}$$

Using the expressions deduced in Section 2, the values of equivalent elements are obtained and compared with the extracted experimental values as shown in Fig. 7.

It is found that the inductance, the capacitance and the conductance of the CPW are almost independent of frequency, and the resistance is dependent on frequency. Higher resistance at higher frequency is reflected by this model. Furthermore, the difference between the model and the experiment is acceptable, and the element values calculated by this model clearly predict the tendency of the extracted values. However, some spikes and ripples in the low frequency band cannot be ignored, and the main reasons are discussed as below.

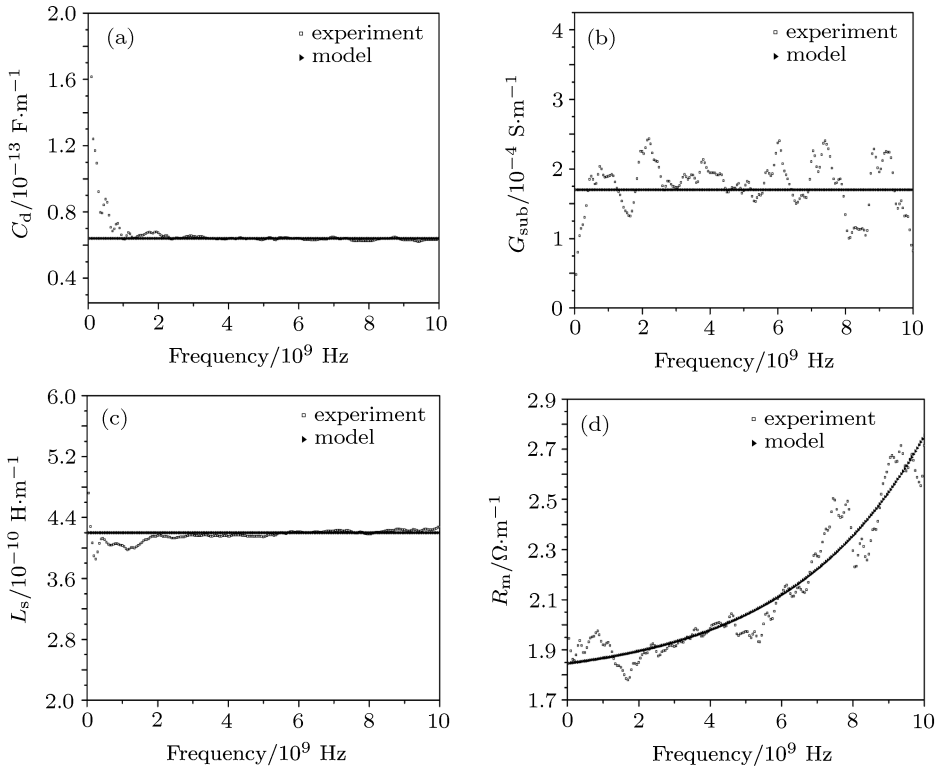


Fig. 7. Comparisons between the model and the experimental measurement for the four equivalent circuit elements defined: (a) substrate capacitance C_d, (b) substrate conductance G_{sub}, (c) line inductance L_s, and (d) line resistance R_m.

First, when the S parameters of the CPW are measured, the error has been produced due to the contact between the pad and the probe, and fluctuation is unavoidable during measurement.

Secondly, the open-short de-embedding method is used to extract the parasitic S parameters. In this method a few more dummy structures are used in a specific lumped-element circuit approximation, which reduces de-embedding accuracy at high frequencies.[15] In the ADS momentum simulation, it is found that most of the mismatches originate from the de-embedding method.

Thirdly, some suppositions in the conformal mapping technique are ideal. In order to satisfy the conformal mapping conditions, it is assumed that two ground planes on both sides of the central conductor are infinite and the CPW is built on a substrate with an infinite thickness. In fact, the ground plane width and substrate thickness are finite, and the suppositions bring the errors into line capacitance and shunt conductance.

Finally, the four-element network can approximately present the electromagnetic mechanism between the CPW and the substrate, and back-stepping to the values of the elements with the measured data leads to an inaccuracy or abrupt change in two ends of the frequency band as shown in Fig. 7.

4. Conclusion

A four-element network is used to present the characterisation of the CPW on an SOI substrate, which is staggered with insulated layers and semiconductor layers. The conformal mapping technique is used to deduce the expressions of the capacitance and conductance of SOI substrate, and then the S parameters of the four-element network are compared with those obtained through the ADS momentum simulation. The values of the four elements in the equivalent network are extracted from the experimental S parameters, and compared with those calculated by the analytical model. It is found that the results from the analytical model are in good agreement with those from the full-wave method and experiment data, and that the tendency of the extracted values can be clearly predicted. Finally, the reasons of the mismatch are analysed, and ADS momentum simulation indicates that the de-embedding method give rise to the most of mismatches. Consequently, this analytical model allows a simple evaluation of the CPW on SOI substrate, and also can be extended to other similar cases.

References

[1] Chen C L and Spector S J 2002 *IEEE Electron. Dev. Lett.* **23** 52

[2] Eggert D and Huebler P 1997 *IEEE Trans. Electron Dev.* **44** 1981

[3] Gianesellol F, Gloria D, Montusclat S, Raynaud C, Boret S, Dambrine G, Lepilliet S, Martineau1 B and Pilard R 2007 *IEEE/MTT-S Int. Microwave Symp.* Honolulu, Hawaii, June 3–8, 2007 p453

[4] Bedair S S and Wolff I 1992 *IEEE Trans. Microw. Theory* **40** 41

[5] Schinzinger R and Laura P A A 1991 *Conformal Mapping Methods and Applications* (New York: Elsevier Science Publishing Company Inc.) p266

[6] Ko J S, Kim B K and Lee K 1997 *IEEE Trans. Electron Dev.* **44** 856

[7] Gillick M, Robertson I D and Joshi J S 1993 *IEEE Trans. Microw. Theory* **41** 1606

[8] Gevorgian S, Berg H, Jacobsson H and Lewin T 2003 *IEEE Microw. Mag.* **4** 60

[9] Kwon Y R and Hietala V M 1987 *IEEE Trans. Microw. Theory* **35** 545

[10] Ghione G 1993 *IEEE Trans. Microw. Theory* **41** 1499

[11] Tuncer E, Lee B T, Islam M S and Neikirk D P 1994 *IEEE Trans. Microw. Theory* **42** 1807

[12] Rautio J C 2000 *IEEE Microw. Mag.* **1** 60

[13] Koolen M C A M, Geelen J A M and Versleijen M P J G 1991 *IEEE 1991 Bipolar Circuits and Technology Meeting* Minneapolis, Minnesota, September 9–10, 1991 p188

[14] Eo Y and Eisenstadt W R 1993 *IEEE Trans. Compon. Hybrids Manuf. Technol.* **16** 555

[15] Tiemeijer L F, Havens R J, Jansman A B M and Bouttement Y 2005 *IEEE Trans. Microw. Theory* **53** 723