An interconnect width and spacing optimization model considering scattering effect*

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As the feature size of the CMOS integrated circuit continues to shrink, the more and more serious scattering effect has a serious impact on interconnection performance, such as delay and bandwidth. Based on the impact of the scattering effect on latency and bandwidth, this paper first presents the quality-factor model which optimises latency and bandwidth effectively with the consideration of the scattering effect. Then we obtain the analytical model of line width and spacing with application of curve-fitting method. The proposed model has been verified and compared based on the nano-scale CMOS technology. This optimisation model algorithm is simple and can be applied to the interconnection system optimal design of nano-scale integrated circuits.

Keywords: scattering effect, curve fitting, interconnection line dimensions, nanometer integrated circuits

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1. Introduction

As the feature size of the Complement Metal–Oxide–Semiconductor (CMOS) integrated circuit continues to shrink, interconnection lines are decreasing in size and the radius of interconnect close to or even shorter than the mean free path of electronics (about 40 nm for copper at room temperature), resulting in scattering effect which can cause large errors if we ignore it. Number of researchers have found that the presence of scattering effect will greatly increase the resistivity of the interconnection,[1,2] thereby affect the interconnection performance such as delay and bandwidth. Therefore, in order to reduce scattering effect, researchers have studied exploratory structures such as carbon nano-tubes as possible replacement of copper interconnection,[3] but at least by 22 nm technology, it is not likely that copper will be replaced by carbon nano-tubes or other materials.[3] There are also efforts in manufacturing improvement to partially reduce the scattering effect of copper wires,[4] but even so the scattering effect can no longer be ignored as the technology continues to scale down. Thus, in the performance analysis of interconnection line, we must consider scattering effect, or it will cause serious errors.

In order to improve interconnection performance, researchers have proposed a number of optimisation methods,[5−23] including the line width and spacing optimisation model. In Ref. [5], the line width optimisation method compromising power and delay has been proposed based on the impact of the line width on them, while Refs. [6] and [7] give the optimisation model of the line width and spacing taking into account delay, power consumption, area and bandwidth at the same time. As the feature size of the CMOS integrated circuit continues to shrink, scattering effect will become increasingly significant, and due to ignoring scattering effect, the above literatures will produce errors which can not be ignored. With consideration of scattering effect, the optimisation model of the line width for delay has been proposed in Ref. [8]. However, with the increasing signal frequency and the reducing rise time, bandwidth has become one of the key factors to be considered when we design a global interconnect. Therefore this paper discusses the optimisation model of the line width and spacing for delay and bandwidth with consideration of scattering effect. This model is simple and can be extended to the situation considering power and area.

In this paper, we have got the analytical model of the optimal line width and spacing by the figure of merit (FOM) method. We firstly give the expressions of interconnection delay and bandwidth with consid-

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eration of scattering effect in the nano-scale CMOS processes. Then we put forward the FOM optimisation model which optimises latency and bandwidth, and obtain the analytical model of the line width and spacing by the use of curve fitting method. Finally, we validate the need to consider scattering effect, and give the optimisation results of the proposed model.

2. The delay–bandwidth considering scattering effect

2.1. Delay

Based on curve fitting techniques, Ref. [8] has proposed the analytical model to predict the resistivity of copper with consideration of scattering effect:

$$\rho(W) = \rho_{\mathrm{B}} + \frac{K_\rho}{W}, \tag{1}$$

where fitting parameters $\rho_{\mathrm{B}} = 2.202\ \mu\Omega\cdot\mathrm{cm}$, $K_\rho = 1.030\times10^{-15}\ \Omega\cdot\mathrm{m}^2$. It is noteworthy that ρ_{B} is roughly the same as the resistivity of copper wire without consideration of scattering effect.

The cross-section of the global interconnection is shown in Fig. 1, where W, S and T are the interconnection line width, spacing and thickness respectively, T_{OX} is the interconnection dielectric layer thickness. In the Refs. [9] and [10], we can see that if the interconnection line inductance per unit length $l < l_{\mathrm{crit}}$, the interconnection delay response will be similar to the reaction with the Elmore delay, where l_{crit} is overdamped key length inductance.[10] As the feature size of the CMOS integrated circuit continues to shrink, the Elmore delay model can be set up in most conditions, so in this paper we use the Elmore delay model to estimate the global interconnection delay. Reference [10] shows that if buffer size k and the length h between two buffers satisfy the following formula:

$$k = k_{\mathrm{opt}} = \sqrt{\frac{r_{\mathrm{s}}c}{rc_0}}, \quad h = h_{\mathrm{opt}} = \sqrt{\frac{2r_{\mathrm{s}}(c_0+c_{\mathrm{p}})}{rc}}, \tag{2}$$

then the time index of this interconnection segment is optimal, that is:

$$\tau = r_{\mathrm{s}}(c_0+c_{\mathrm{p}}) + \frac{r_{\mathrm{s}}}{k_{\mathrm{opt}}} + rh_{\mathrm{opt}}k_{\mathrm{opt}}c_0 + \frac{1}{2}rch_{\mathrm{opt}}^2, \tag{3}$$

where r_{s}, c_0 and c_{p} are the output resistance, input capacitance and output capacitance of a minimum-sized repeater respectively, r and c are the interconnection resistance and capacitance per unit length respectively.

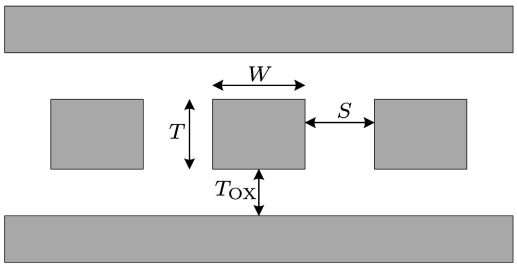


Fig. 1. Cross section of global interconnections.

As the interconnection delay is proportional to delay per unit length, so for interconnection lines with a given length, the conclusions obtained by the analysis of the delay per unit length are also applied to total interconnection delay. In this case, this paper takes the delay per unit length as the analysis object.

By Eqs. (2) and (3), we can get the optimal delay index per unit length

$$\left(\frac{\tau}{h}\right)_{\mathrm{opt}} = 2\sqrt{r_{\mathrm{s}}c_0}\left(1+\sqrt{\frac{1}{2}\left(1+\frac{c_{\mathrm{p}}}{c_0}\right)}\right)\sqrt{rc}. \tag{4}$$

By Eq. (4), we can see that the interconnection delay per unit length is a function of interconnection parameters r and c, which is shown in Eqs. (5) and (6) respectively:

$$r = \frac{\rho(W)}{WT}, \tag{5}$$

$$c = c_{\mathrm{a}} + c_{\mathrm{b}}W + \frac{c_{\mathrm{c}}}{S}, \tag{6}$$

where c_{a} represents the fringing capacitance, c_{b} represents the parallel plate capacitance to the top and bottom layers of metal and is proportional to interconnect width, c_{c} represents the coupling capacitance between the neighbouring interconnections and is inversely proportional to interconnection spacing.

Substituting Eqs. (1), (5) and (6), into Eq. (4), we can get the unit length optimal delay index with consideration of scattering effect

$$\left(\frac{\tau}{h}\right)_{\mathrm{opt}} \propto \frac{\sqrt{W+K}}{W}\sqrt{c_{\mathrm{a}}+c_{\mathrm{b}}W+\frac{c_{\mathrm{c}}}{S}}, \tag{7}$$

where

$$K = \frac{K_\rho}{\rho_{\mathrm{B}}}. \tag{8}$$

2.2. Bandwidth

As the signal frequency increases and the rise time decreases, increasing interconnection bandwidth has become an important part of the requirements in high-speed digital circuit performance. As shown in Fig. 2, in the condition of considering scattering effect, the

bandwidth B of global interconnections with the optimal buffer insertion is given by

$$\begin{aligned} B &= N\frac{1}{D} \\ &\propto \frac{E_{\text{chip}}}{W+S}\frac{1}{(\tau/h)_{\text{opt}}} \\ &\propto \frac{1}{W+S}\frac{W}{\sqrt{W+K}}\frac{1}{\sqrt{(c_{\text{a}}+c_{\text{b}}W+c_{\text{c}}/S)}}, \end{aligned} \tag{9}$$

where E_{chip} is the width of the chip.

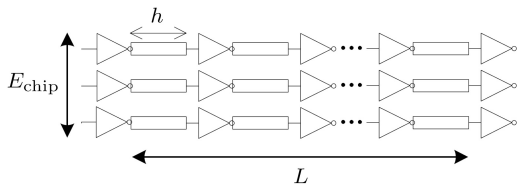


Fig. 2. Global interconnections with optimal buffer insertion.

3. The analytical optimization model of interconnection line width and spacing

The aim of global interconnection design is to obtain small delay per unit length and large bandwidth. Unfortunately, from Eqs. (7) and (9) we can see that small delay requires large global interconnection width and spacing, but large bandwidth requires small global interconnection width and spacing. They do not have the same demand on line width and spacing, so latency and bandwidth can not be optimal at the same time and we only can compromise them. In order to optimise delay and bandwidth effectively, this paper uses the effective trade-off FOM model of latency and bandwidth:

$$\text{FOM} = \left(\frac{\tau}{h}\right)_{\text{opt}}\left(\frac{1}{B}\right)^{\eta}, \tag{10}$$

where η is the weight factor which describes the weight of the bandwidth in the FOM. Assume that the minimum line width is equal to the minimum line spacing, $W_{\min} = S_{\min}$,[7] the optimal line width and spacing for the minimum FOM can be determined by setting simultaneously the derivative of FOM with respect to W and S to zero,

$$\begin{cases} \frac{\partial \text{FOM}}{\partial W} = 0, \\ \frac{\partial \text{FOM}}{\partial S} = 0, \end{cases} \quad \text{and} \quad \begin{cases} W \geq W_{\min}, \\ S \geq S_{\min}. \end{cases} \tag{11}$$

Through the calculation and analysis, we can find

$$\begin{cases} \frac{\partial \text{FOM}}{\partial W} = f_1(W,S)\, g_1(W,S) + c_{\text{b}} g_2(W,S), \\ \frac{\partial \text{FOM}}{\partial S} = -f_2(W,S)\, g_1(W,S) - \frac{c_{\text{c}}}{S^2} g_2(W,S), \end{cases} \tag{12}$$

where the specific form of $f_1(W,S)$, $f_2(W,S)$, $g_1(W,S)$ and $g_2(W,S)$ can be got by solving the partial differention of Eq. (10). Because of its complex form, we do not give the specific form. Setting Eq. (12) to 0, we can obtain

$$\frac{f_1(W,S)}{f_2(W,S)} = \frac{c_{\text{b}}S^2}{c_{\text{c}}} = \lambda, \tag{13}$$

where λ is a proportional factor. Due to different weight η, the optimal line width and line spacing value is different. Accordingly, if we change the weight η, $\frac{f_1(W,S)}{f_2(W,S)}$ will also change, namely λ will also change. So λ is not a constant but a weight-related function, that is $\lambda = \lambda(\eta)$. Using of curve fitting method, we have found that when $0.5 \leq \eta \leq 3$,

$$\lambda = a + \frac{b}{\eta}, \tag{14}$$

where a, b are constants in a specific process, as shown in Table 1. It is noteworthy that, in most conditions, $0.5 \leq \eta \leq 3$ can meet the application requirements. Figure 3 shows the curve fitting status based on the 45 nm CMOS process. From Fig. 3, we can see that Eq. (14) can accurately fit $\lambda(\eta)$.

Table 1. Curve fitting parameters.

Tech. Node	90 nm	65 nm	45 nm
a	−0.0451	−0.0679	−0.0385
b	0.5854	0.5193	0.5250

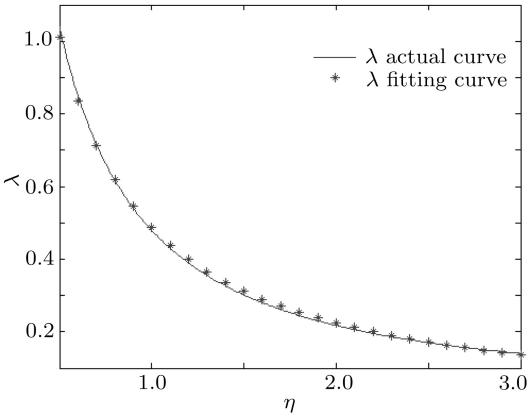


Fig. 3. Curve fitting status based on the 45 nm CMOS process.

By the analysis of Eq. (13), we can obtain

$$\begin{cases} S_{\rm opt} = \sqrt{\frac{\lambda c_{\rm c}}{c_{\rm b}}}, \\ (2\lambda\eta + \eta - 1)\, W_{\rm opt}^2 + (2\lambda\eta K - 2K - S_{\rm opt}\eta - S_{\rm opt})\, W_{\rm opt} - 2\,(1+\eta)\, K S_{\rm opt} = 0. \end{cases} \tag{15}$$

In practice, in order to determine $\lambda(\eta)$, we can firstly choose a, b from Table 1 according to the technical type. Then based on the actual application requirements of the delay and bandwidth, we can select the appropriate weight η. Finally, we can obtain the optimal line width and spacing by calculating Eq. (15).

4. Model validation and analysis

To illustrate the need for considering scattering effect, we compare the optimal results considering scattering effect with that without considering scattering effect. Table 2 lists the optimisation results based on 45 nm CMOS process under two kinds of situations, where $W_{\rm opt}/W_{\rm min}$ is the optimal line width as a ratio of the minimum line width, $S_{\rm opt}/S_{\rm min}$ is the optimal line spacing as a ratio of the minimum line spacing. By the analysis of Table 2, we find that in both cases, the optimal line spacing is same, while the error of the optimal line width is great and the maximum error closes to 25%. This is mainly because scattering effect influences the metal resistivity through the line width, and has nothing to do with the line spacing, so in both cases the optimal line spacing is the same, while the error of the optimal line width is great. The great error of the optimal line width is bound to lead to the error of the performance which can not be ignored, thus affects the entire integrated circuit design, and therefore we have to consider scattering effect when we analyse the performance of interconnection lines.

The methodology outlined above is used to optimise the width and spacing of global interconnections for International Technology Roadmap for Semiconductors (ITRS) technology nodes from 90 nm up to 45 nm and the relevant technology parameters can be seen in Ref. [6]. We consider three optimisation criteria, that is, $\eta = 0.5$, $\eta = 1.0$ and $\eta = 1.5$. Because this model has a simple analytical form, so in practical applications, if the results of three above-mentioned weights do not satisfy with the practical requirements, users can choose appropriate weight factor according to the actual request and then obtain the optimal line width and spacing by calculating Eq. (14).

Table 3 lists the results of this optimisation model where $F_{\rm opt}/F_{\rm min}$ is the ratio of optimised FOM when $W = W_{\rm opt}$ and $S = S_{\rm opt}$ to the FOM when $W = W_{\rm min}$ and $S = S_{\rm min}$. From Table 3, it is obvious that the optimal line width $W_{\rm opt}$ and spacing $S_{\rm opt}$ are reasonable and suitable for nanometer designs, which indicates that the proposed methodology is an effective method for global interconnection optimisation.

Table 2. Comparison between two kinds of optimisation results based on 45 nm process.

η	with scattering effect		without scattering effect		error/%	
	$\frac{W_{\rm opt}}{W_{\rm min}}$	$\frac{S_{\rm opt}}{S_{\rm min}}$	$\frac{W_{\rm opt}}{W_{\rm min}}$	$\frac{S_{\rm opt}}{S_{\rm min}}$	W	S
0.5	12.3349	3.6390	10.6715	3.6390	13.49	0
1.0	6.4027	2.5237	5.1875	2.5237	18.98	0
1.5	4.5580	2.0194	3.5194	2.0194	24.98	0

Table 3. Optimisation results for different criteria and various technology nodes.

Tech. Node	η=0.5			η=1.0			η=1.5		
	$\frac{W_{\rm opt}}{W_{\rm min}}$	$\frac{S_{\rm opt}}{S_{\rm min}}$	$\frac{F_{\rm opt}}{F_{\rm min}}$	$\frac{W_{\rm opt}}{W_{\rm min}}$	$\frac{S_{\rm opt}}{S_{\rm min}}$	$\frac{F_{\rm opt}}{F_{\rm min}}$	$\frac{W_{\rm opt}}{W_{\rm min}}$	$\frac{S_{\rm opt}}{S_{\rm min}}$	$\frac{F_{\rm opt}}{F_{\rm min}}$
90 nm	9.0126	2.9558	0.4720	4.7045	2.0385	0.5937	3.3214	1.6212	0.6778
65 nm	12.3916	3.4856	0.3827	6.2053	2.3770	0.4974	4.3012	1.8664	0.5772
45 nm	12.3349	3.6390	0.3547	6.4027	2.5237	0.4526	4.5580	2.0194	0.5196

Table 4 lists the delay per unit length $(\tau/h)_{\rm opt}$ at $W = W_{\rm opt}$ and $S = S_{\rm opt}$ as a fraction of $(\tau/h)_{\rm opt}$ at $W = S = W_{\rm min}$. Obviously, increasing the width and spacing of the wires reduces the delay per unit length significantly. Also note that the relative improvements in delay tends to increase with technology scaling, such as the delay is improved by 50% in 90 nm technology to 62% in 45 nm technology for the crite-

rion of $\eta = 1.5$.

Table 5 lists the bandwidth B at $W = W_{\rm opt}$ and $S = S_{\rm opt}$ as a fraction of B at $W = S = W_{\rm min}$. As the improvement in delay is at the expense of bandwidth, so when the relative improvement in delay is improved, its bandwidth performance will been degenerated. From Table 5, we can see that the decline in bandwidth is from 19% to 53%. In practice, users should make a reasonable compromise in optimisation between delay and bandwidth according to the actual request to reach a performance optimisation and meet the actual application requirements at the same time.

Table 4. Ratio of $(\tau/h)_{\rm opt}$ at $W = W_{\rm opt}$, $S = S_{\rm opt}$ with $(\tau/h)_{\rm opt}$ at $W = S = W_{\rm min}$.

Tech. Node	$\eta = 0.5$	$\eta = 1.0$	$\eta = 1.5$
90 nm	0.3339	0.4196	0.4974
65 nm	0.2642	0.3405	0.4084
45 nm	0.2507	0.3184	0.3767

Table 5. Ratio of B at $W = W_{\rm opt}$, $S = S_{\rm opt}$ with B at $W = S = W_{\rm min}$.

Tech. Node	$\eta = 0.5$	$\eta = 1.0$	$\eta = 1.5$
90 nm	0.5005	0.7068	0.8136
65 nm	0.4767	0.6845	0.7940
45 nm	0.4994	0.7036	0.8071

5. Conclusion

Based on the significant impact of scattering effect, we propose the optimisation model by optimising the width and line spacing to optimise delay and bandwidth with consideration of scattering effect. In this paper, we first give the expressions of interconnect delay and bandwidth in the nano-scale CMOS processes with consideration of scattering effect. Then we put forward the FOM optimisation model which optimises latency and bandwidth, and obtain the analytical model of the line width and spacing by the use of curve fitting method. Finally, we validate the need to consider scattering effect, and give the optimization results of the proposed model. Our optimisation model is simple and can be applied to nano-CMOS integrated circuit interconnect system optimal design.

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