Rapid Communication

Fabrication of suspended graphene devices and their electronic properties*

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Suspended graphene devices are successfully fabricated by using a novel PMMA/MMA/PMMA tri-layer resist technique. The gap between graphene and dielectric substrate can be easily controlled by the thickness of the bottom PMMA layer, and no wet-etching with hazardous hydrofluoric acid is involved in our fabrication process. Electrical characterizations on suspended graphene devices are performed in vacuum when *in-situ* current annealing directly leads to a significant improvement on transport properties of graphene, i.e., the increase of carrier mobility with the reduction of width of Dirac peak. Our results make a new opportunity to study intrinsic properties of graphene.

Keywords: graphene, transport, suspension, high mobility
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1. Introduction

Graphene, an isolated atomic plane of graphite, has become one of the most exciting research topics since it was first deposited on silicon oxide (SiO_2) substrates by mechanical exfoliation in 2004.[1] Graphene has been proposed as a unique quantum system to study many-body phenomena in condensed matter physics and a promising candidate for future nanoelectronics.[2−8] The underlying assumption is that graphene is minimally affected by its environment and behaves as a truly two-dimensional material. However, recent experiments have shown that graphene, with all lattice atoms directly exposed to extrinsic fluctuations, is particularly sensitive to scattering impurities from SiO_2 substrates.[9−12] Thus improving qualities of substrates or suspending graphene is important to eliminate extrinsic scatterings of graphene and reveal its intrinsic prosperities.

While suspended graphene devices with ultrahigh electron mobilities have been achieved in the past, they were all obtained from conventional devices supported on SiO_2/Si substrates by removing the SiO_2 layer with hydrofluoric acid (HF) etching.[13,14] HF vapours produced during etching can pose a serious health threat,[15] and chemical etching is not compatible with current complimentary metal–oxide–semiconductor (CMOS) techniques.

In this paper, we report a simple and efficient way to fabricate suspended graphene devices with a flexible PMMA/MMA/PMMA tri-layer resist technique. Transport properties of our suspended devices are further characterized in vacuum at room temperature, and improved mobilities and reduced width of Dirac peaks are realized by current annealing of suspended graphene.

2. Experiments

2.1. Preparation and Raman characterization of graphene

A thin polymethyl methacrylate (PMMA) layer was first coated on top of a SiO_2/Si substrate and baked at 180 °C for 15 min. We note that the thickness of the PMMA layer sets the gap between graphene and the dielectric substrate, which can be adjusted as desired. Then the thickness of the SiO_2

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dielectric layer was calculated based on the thickness of the PMMA layer to give the optimal optical contrast of single-layer graphene on the PMMA/SiO_2/Si substrate.[16−18] In the following discussion, the fabrication of devices is demonstrated with 120nm thick PMMA layer on the top of 180nm SiO_2.

Graphene flakes were then deposited on PMMA from natural graphite by mechanical exfoliation.[1,17,18] Single-layers were located by their optical contrast and further confirmed via Raman characterization as shown in Fig. 1. We note that the sharp, single 2D Raman peak at 2675 cm^{-1} distinguishes a single-layer from few-layer graphene, and the absence of D peak around 1350 cm^{-1} shows that there are no/little lattice defects in our graphene nanomembrane.[17−20]

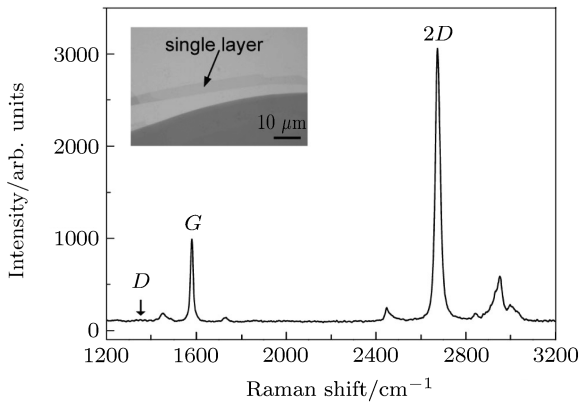


Fig. 1. Raman spectrum of single-layer graphene on the PMMA. Raman measurements were performed by using a micro-Raman spectroscope (Renishaw in Via) at a wavelength of 514 nm. The laser power was set at 1.0 mW and a 100× objective lens with N.A. = 0.90 was used to focus the laser beam on the sample, which resulted in a laser spot of ∼1.0 μm. Inset shows optical image of single layer graphene on PMMA.

2.2. Fabrication of suspended graphene devices

The key steps to fabricating suspended graphene devices are illustrated in Fig. 2. The first step is that the graphene flakes on the PMMA substrate were coated with 500 nm of methacrylic acid (MAA) as the second resist layer followed by the third resist layer of 120 nm PMMA. We placed an MMA layer between the two PMMA layers because PMMA's solvent, chlorobenzene, dissolves the first PMMA layer very fast during spinning and dislocates graphene flakes when directly spin-coated on the top of the graphene flakes. On the other hand, the solvent of MMA, ethyl lactate, is a weak solvent for PMMA and does not move the flakes during the second spinning (Fig. 2(b)).[17] The second step is that electrical contacts to graphene were patterned by electron beam lithography (EBL) (Fig. 2(c)). Then 5 nm Cr and 115 nm Au films were deposited sequentially by employing thermal evaporation (Fig. 2(d)) followed by lift-off in acetone. The third step is that the chip with graphene devices was transferred from acetone to ethanol solution and further dried in a CO_2 critical point drier to prevent the surface-tension-induced collapse of suspended graphene nanomembranes (Fig. 2(e)).

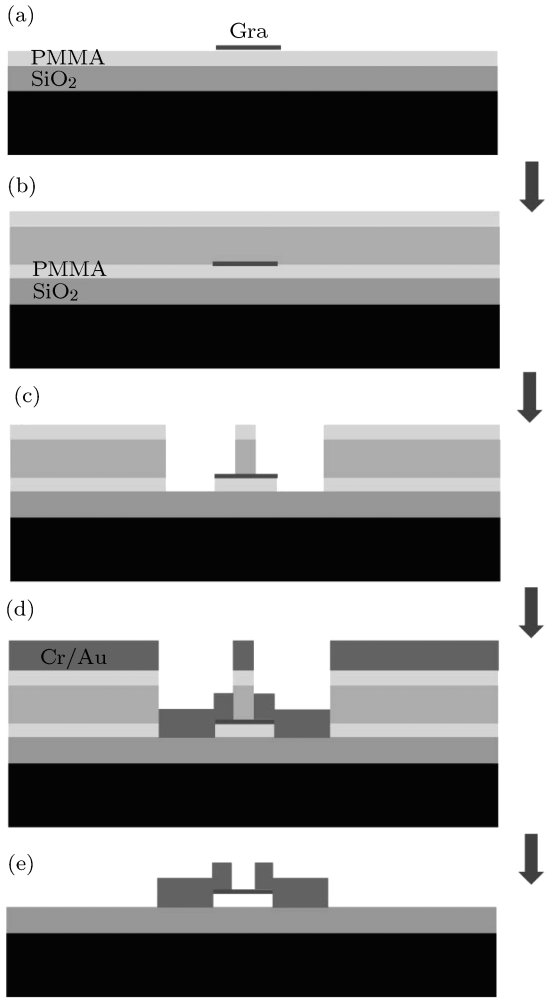


Fig. 2. Fabrication scheme of suspended graphene devices. (a) Deposition of graphene flakes on the top of a SiO_2/Si substrate coated with 120nm thick PMMA resist layer; (b) MMA and PMMA layers were spin-coated sequentially on the top of the graphene flakes; (c) Electron-beam lithography to define contacts; (d) Deposition of metal films; (e) Graphene was suspended by a pair of metallic electrodes after lift-off.

3. Results and discussion

Using the PMMA/MMA/PMMA tri-layer resist process, we have successfully fabricated suspended graphene devices (Fig. 3(a)). Atomic force microscopy (AFM) of the same device (Fig. 3(b)) was conducted to confirm the integrity of the graphene sheet and its suspension above the SiO_2 surface. The gap between graphene and the dielectric SiO_2 substrate was measured to be 120 nm, which is consistent with the thickness of the bottom PMMA layer.

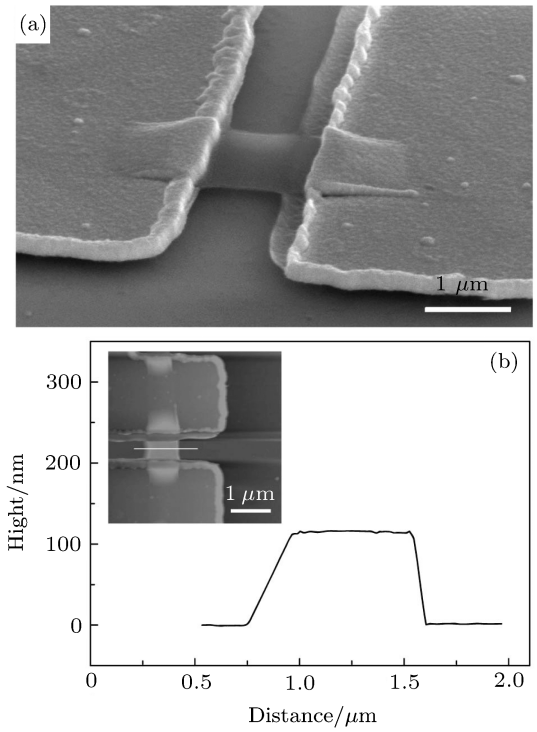


Fig. 3. Suspended graphene. (a) SEM image of a suspended graphene device is taken at 60° angle with respect to the sample plane; (b) An AFM line scan profile confirms the 120nm distance between graphene and the dielectric substrate of the same device in (a). Inset shows the AFM image of the device.

The electrical properties of the suspended graphene device are summarized in Fig. 4. The black line shows the source–drain conductance measured as a function of back gate voltage right after the device fabrication. When a negative gate voltage is applied, the Fermi level sits in the valence band and holes are the majority carriers in graphene. The conductance starts to decrease with gate voltage increasing due to the depletion of holes until it reaches its minimum at the Dirac point of ~ 15 V, where the Fermi energy is at the crossover between valence and conduction bands. Then, the conductance increases with the gate voltage as the Fermi level goes to the conduction band and the accumulation of electrons begins in graphene.[1,21,22]

The mobilities of hole- and electron-carriers in our suspended graphene devices can be calculated as[21,22]

$$\mu = \frac{\mathrm{d}G/\mathrm{d}V_{\mathrm{gate}}}{C_{\mathrm{g}}} \times \frac{L}{W}, \tag{1}$$

where C_{g} is the unit-area capacitance of the back-gate, L and W are the channel length and width of the suspended graphene between source and drain, G is the conductance of the device, and $\mathrm{d}G/\mathrm{d}V_{\mathrm{gate}}$ is the transconductance for hole or electron branches and can be measured as the slopes in the linear regions in Fig. 4.

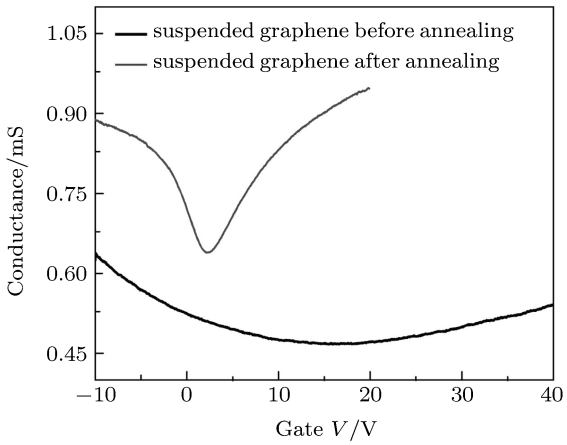


Fig. 4. Transport characterization of the same suspended graphene device as that in Fig. 3. Conductance is plotted as a function of the back-gate voltage before and after current annealing.

For the device considered in Fig. 4, the unit-area capacitance can be estimated to be[22]

$$\begin{aligned} C_{\mathrm{g}} &= 1/\left(\frac{1}{\frac{\varepsilon_0}{d_{\mathrm{vac}}}} + \frac{1}{\frac{\varepsilon_0\varepsilon_{\mathrm{ox}}}{d_{\mathrm{ox}}}}\right) \\ &= 1/\left(\frac{1}{\frac{8.85\times10^{-12}}{1.2\times10^{-7}}} + \frac{1}{\frac{8.85\times10^{-12}\times4}{1.8\times10^{-7}}}\right) \\ &= 5.4\times10^{-5}\ \mathrm{F/m^2}, \end{aligned} \tag{2}$$

thus the mobilities of holes and electrons for the as-fabricated device are estimated to be 3600 and 1000 $\mathrm{cm^2/(V{\cdot}s)}$, respectively.

Resist contamination from fabrication processes has been observed in former studies, and Joule heating by current annealing was used to stripe resist residues on graphene.[13] We carried out the device annealing in vacuum by slowly increasing the source–drain voltage and monitoring simultaneously the current flowing through the sample. When the current started to

fluctuate, the source–drain voltage would keep constant until the current saturates. This process was repeated more than twice. We note that a few volts of the source–drain voltage induced a large current of a few milliampares, which results in a very large current density J of a few 10^8 A/cm^2.

The electrical properties of our graphene devices were measured again after surface cleaning of graphene by annealing. The curve of conductance versus the gate voltage after annealing is shown as the grey line in Fig. 4, which is more symmetrical and smooth than that before annealing. Further, the width of the Dirac peak is almost one magnitude narrower after annealing than before annealing. These changes confirm the improvement on the sample quality after current annealing, which results in the increase of mobilities in graphene (16,000 and 9500 cm^2/(V·s) for holes and electrons, respectively). We note that the performance of our devices is comparable to those of HF-etched suspended devices at room temperature in Refs. [13] and [23]. High mobility at room temperature makes suspended graphene a very promising candidate for fast nanoelectronics and ultrasensitive sensors.[2]

4. Conclusions

We demonstrate a PMMA/MMA/PMMA trilayer resist technique by which electrically contacted graphene can be suspended through controlling the distance from the dielectric substrate. Electrical transport characteristics of suspended graphene devices are investigated in vacuum at room temperature. Upon *in-situ* current annealing, mobilities for holes and electrons are both significantly enhanced and the width of the Dirac peaks is almost one order of magnitude narrower than that before annealing. Our approach enables the easy approaching intrinsic properties in graphene.

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