Study of 4H-SiC junction barrier Schottky diode using field guard ring termination*

Chen Feng-Ping(陈丰平)†, Zhang Yu-Ming(张玉明), Lü Hong-Liang(吕红亮), Zhang Yi-Men(张义门), and Huang Jian-Hua(黄建华)

School of Microelectronics, Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xidian University, Xi'an 710071, China

(Received 11 January 2010; revised manuscript received 15 March 2010)

This paper reports that the 4H-SiC Schottky barrier diode, PiN diode and junction barrier Schottky diode terminated by field guard rings are designed, fabricated and characterised. The measurements for forward and reverse characteristics have been done, and by comparison with each other, it shows that junction barrier Schottky diode has a lower reverse current density than that of the Schottky barrier diode and a higher forward drop than that of the PiN diode. High-temperature annealing is presented in this paper as well to figure out an optimised processing. The barrier height of 0.79 eV is formed with Ti in this work, the forward drop for the Schottky diode is 2.1 V, with an ideality factor of 3.2, and junction barrier Schottky diode with blocking voltage higher than 400 V was achieved by using field guard ring termination.

Keywords: 4H-SiC, junction barrier Schottky diode, annealing, electrical characteristics
PACC: 7155D, 7330, 7340N

1. Introduction

With increasing interest in SiC Schottky barrier diode (SBD) in power conversion applications, much attention has been focused on improving SiC SBD performance. Thus, the junction barrier Schottky (JBS) diode was proposed which offers Schottky-like ON-state and fast switching characteristics, while the OFF-state characteristics have a low leakage current similar to that of the PiN diode. Several SiC JBS diodes have been reported by different groups.[1−3] The conduction loss can be much lower than that of a PiN diode with a breakdown voltage of less than 3 kV due to the high turn-on voltage (2.7 V) of the SiC p–n junction.[4] The leakage current of the JBS diode is lower than that of a SBD by shielding the high electric field away from the Schottky contact by depletion layer of p–n junctions. To create a JBS diode with a high break down voltage, several kinds of terminations have been used in the structure, such as junction termination extension and mesa termination. However, these terminations require etching and extra ion-implantation. To reduce the processing steps, field guard ring (FGR) was used in this work and it was fabricated with P^+ for p–n junction simultaneously. Because the P^+ regions of the SiC JBS diodes are formed by ion implantation, a high-temperature (> 1600 °C) activation annealing step is required. This step will cause harming the surface since silicon can preferentially evaporate at the high annealing temperature. Several tests have been done in this work to show the influence from the annealing to the surface and the electric characteristics of the devices. To study the influence of different parameters of structure on the electric characteristics and to compare each different devices, 4H-SiC SBD, PiN diode and two kinds of JBS diodes with different parameters were fabricated in this work.

2. Design and fabrication

A 10 μm N^- epilayer with doping of 1.56×10^{15} cm^{-3} was grown on the N^+ substrate produced by CREE and doped by the concentration more than 1×10^{18} cm^{-3}. To create the circular P^+ regions, multiple implantations were used. At 400 °C, in argon ambience, Al ion was implanted with energy of 30 eV, 280 eV, and 500 eV when the doses of 8.6×10^{13} cm^{-2}, 5.2×10^{14} cm^{-2}, and 7.8×10^{14} cm^{-2} were taken respectively. As shown in Fig. 1, the P^+ junction grid is characterised by the width of the P^+

*Project supported by the 13115 Innovation Engineering of Shanxi (Grant No. 2008ZDKG-30).
†Corresponding author. E-mail: fpchen@yeah.net
© 2010 Chinese Physical Society and IOP Publishing Ltd

implantation window (W) and the spacing in between (S). The FGRs are characterised by the width of a single ring (L) and the spacing between two nearest rings (D). According to Ref. [5], L was chosen to be the fixed value 5 μm, and $D = 2.5$ μm in the experiment described below. The FGRs with 5 μm-wide for each ring were implanted around the periphery of the forward conducting active area to reduce electric field crowding toward the edge of the diode under reverse bias. All the FGRs were formed simultaneously with the P^+ junction regions stated above, thus the depth and concentration are same to the P^+ junction regions. Samples were annealed at 1650 °C for 45 min in argon ambience. Then, the profile in 0.6 μm depth was measured.

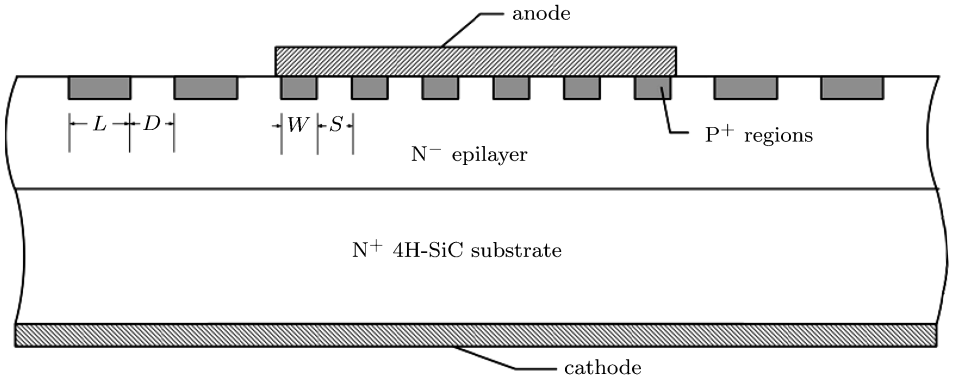


Fig. 1. Schematic cross section of the JBS diodes with FGRs as edge termination.

Figure 2 shows the distribution of the Al atoms before and after annealing, tested by secondary ion mass spectroscopy. As can be seen from this figure, the distribution of the Al atoms are barely changed after annealing, only in the depth more than 0.4 μm, and the concentration curve becomes more smooth. It shows that the Al atoms move a little deeper in epilayer after annealing. To protect the surface of 4H-SiC and avoid silicon atoms escaping from surface at high annealing temperature, a graphite crucible being full of SiC powder is used to reduce the surface damage during annealing process.[6]

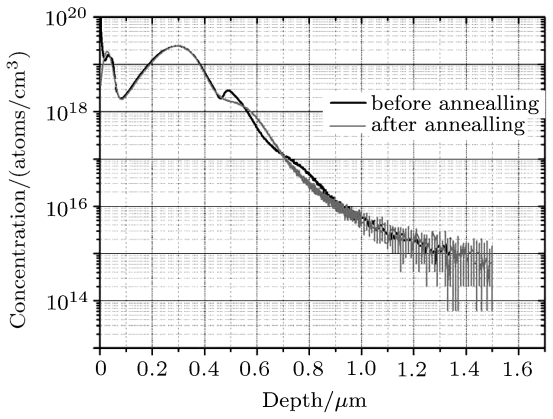


Fig. 2. Distribution of Al atoms before and after the annealing.

The Tri-layer metallization of Ti/Ni/Ag was used to form a backside contact, and subsequently annealed at 1000 °C in gas mixture of 97% N_2 and 3% H_2 for 5 min. The Bi-layer metallization of Ti/Ag was used to form the front Schottky metal contact.

3. Results and discussion

3.1. Activation annealing

High-temperature activation annealing for the p-type dopant creates damage to the SiC surface, thus degrading the Schottky performance. Figure 3(a) shows the scanning electron microscope (SEM) photograph of the surfaces before annealing. Figure 3(b) shows the SEM photograph of the surfaces after annealing at 1650 °C in argon for 45 min in a graphite crucible full of SiC powder.

Figure 3(a) shows a relatively smooth surface. After annealing in the graphite crucible, the surface is damaged at a certain extent. It contains gullies in the form of strips in the whole surface of the samples, as is shown in Fig. 3(b). Further electrical characterisation results presented in the following part, will show that those surface damages degrade the device performance.

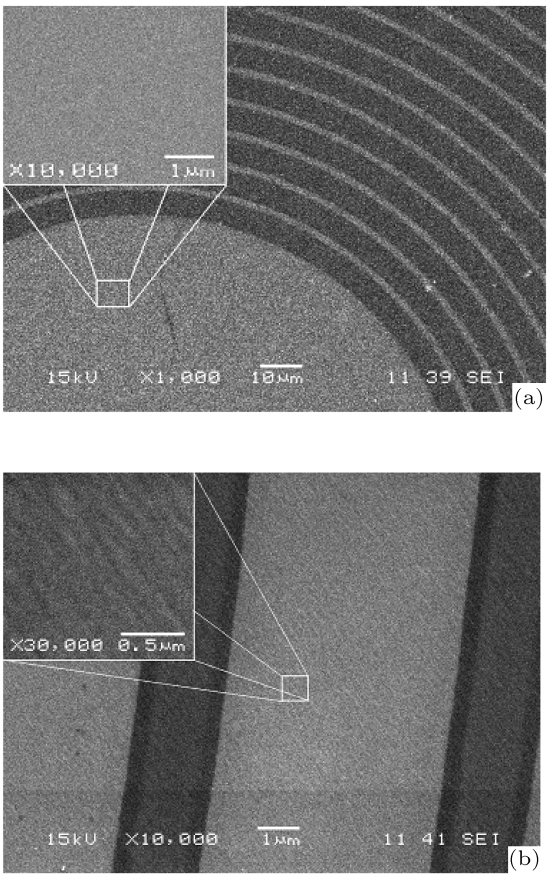


Fig. 3. The SEM photographs of the 4H-SiC surface: (a) before annealing and (b) after annealing.

3.2. Electrical characteristics

The fabricated devices were electrically characterised at room temperature using the Tektronix 370B programmable curve tracer and Agilent B1500A semiconductor device analyser. According to parameters stated previously, the JBS mentioned below are designated as JBS (S, W).

Since SiC JBS diodes conduct current only through the Schottky region, it is expected that the forward drop is low due to the low barrier height in comparison with the high turn on voltage of SiC p–n junction. Forward current density–voltage (J–V) characteristics of the 4H-SiC JBS diodes fabricated are shown in Fig. 4.

Using the thermionic emission theory, the current through the SiC Schottky diode can be expressed in the form

$$I = AA^*T^2 \exp\left(-\frac{\phi_{\rm B}}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right], \quad (1)$$

where A is the diode area, A^* is the Richardson's constant, $\phi_{\rm B}$ is the Schottky barrier height, n is the ideality factor, and other constants have their usual meaning. At a low forward voltage, the ideality factor is given by

$$n = \frac{q}{kT}\frac{\partial V}{\partial \ln I}. \quad (2)$$

Calculating with the equations given above, we obtain that the forward drop for the Schottky diode is 2.1 V, with an ideality factor of 3.2. The forward drop of JBS diode with W of 4 μm and S of 3 μm is 3.9 V at 64.8 A/cm^2. The ideality factor is larger due to the interface states of the SBDs, residual defects and surface roughening caused by ion implantation and annealing. As Ref. [7] shows, the experimental measurements have a good agreement with simulated results, which indicates a good agreement between experiments and the thermionic emission mode.

Figure 4 indicate that with the same W, the forward drop decreases to be closer to that of the SBDs as the S increases. Measurements also show that the PiN diode has a large forward drop ($>$ 6 V) and a low current density, which is not presented in Fig. 4. From the y-intercept of the linear region of the J–V curves, the barrier height of Ti/4H-SiC ϕ_B=0.79 eV can be obtained, this value is consistent with that in Ref. [8].

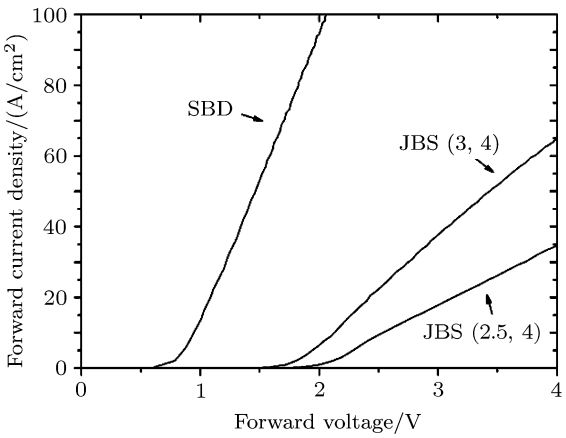


Fig. 4. Forward J–V characteristics of JBS diodes and SBD.

The possible reverse leakage current mechanisms of the JBS are (1) thermionic emission, (2) thermionic field emission, (3) field emission, and (4) generation in the depletion region. In addition to these basic mechanisms, surface leakage and defect-related leakage may occur. The dominant mechanism depends on the Schottky barrier height, temperature, applied voltage, surface status, and defects in the material.

Figure 5 shows the reverse J–V characteristics of SBD, PiN and JBS diodes. As can be seen in Fig. 5, reverse current density of JBS diodes is higher than PiN

diode, and lower than SBD. As tested by Tektronix 370B programmable curve tracer, JBS(3,4) shows a break voltage higher than 400 V. The main reasons resulted in a relatively high leakage current and low breakdown voltage are: (1) Ti is used as the metal to form the Schottky barrier, the barrier height formed in this work is 0.79 eV, which is smaller than the one fabricated with Ni ($\phi_{\rm B} = 1.26$ eV);[10] (2) multi-step ion implantation brought in damages in the space lattice; (3) high temperature annealing caused the deterioration of the epilayer, which was stated previously.

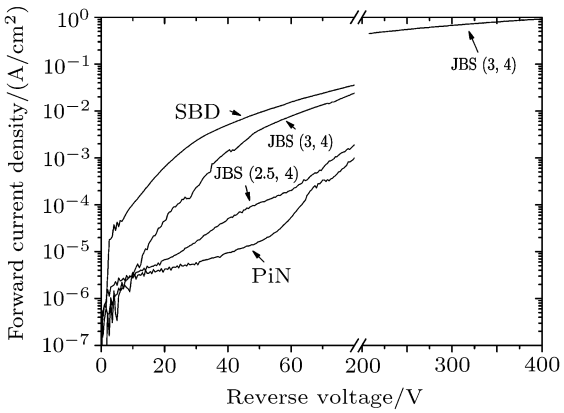


Fig. 5. Reverse J–V characteristics of SBD, PiN and JBS diodes.

To reduce the damage during high-temperature activation annealing, AlN can be used to prevent 4H-SiC surface from silicon evaporation,[10] and carbon film is a feasible way as well.[5]

4. Summary

The design and fabrication procedure of planar 4H-SiC JBS rectifiers with FGRs as the termination were studied. Measurements show the performance tradeoffs between forward characteristics and reverse leakage current density of these JBS diodes. With P^+ region doping concentration ($\sim 1\times10^{18}$ cm^{-3}) and window spacing (3 μm), 4H-SiC JBS rectifiers with Schottky-like forward characteristics and pin-like reverse characteristics have been experimentally demonstrated.

References

[1] Jun W, Yu D, Bhattacharya S and Huang A Q 2009 *Energy Conversion Congress and Exposition. IEEE* San Jose, USA 20–24 Sep. 2009 p1488–1493

[2] Gao Y, Huang A Q and Agarwal A K 2008 *ISPSD 20th International Symposium* Florida, USA 18–22 May 2008 p233–236

[3] Hull B A, Sumakeris J J and O'Loughlin M J 2008 *IEEE Transactions on Electron Devices* **55** 1864

[4] Zhu L, Chow T P, Jones K A and Agarwal A 2006 *IEEE Transactions on Electron Devices* **53** 363

[5] Cao L H 2000 *4H-SiC Gate Turn-Off Thyristor and Merged P-i-N and Schottky Barrier Diode* (Ph.D. Thesis) (New Jersey: Rutgers University New Brunswick)

[6] Guo H 2007 *Theoretical and Experimental Study on Ohmic Contacts to Silicon Carbide* (Ph.D. Thesis) (Shaanxi: Xidian University) (in Chinese)

[7] Wang S G, Yang L A, Zhang Y M, Zhang Y M, Zhang Z Y and Yan J F 2003 *Chin. Phys.* **12** 322

[8] Wang S G, Zhang Y M and Zhang Y M 2003 *Chin. Phys.* **12** 94

[9] Zhang L, Zhang Y M, Zhang Y M, Han C and Ma Y J 2009 *Acta Phys. Sin.* **58** 2737 (in Chinese)

[10] Jones K A, Shah P B, Kirchner K W, Lareau R T, Wood M, Ervin M H, Vispute R D, Sharma R P, Venkatesan T and Holland O W 1999 *Mater. Sci. Eng.* **61–62** 281