A multilevel nano-scale interconnection RLC delay model*

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Based on the multilevel interconnections temperature distribution model and the RLC interconnection delay model of the integrate circuit, this paper proposes a multilevel nano-scale interconnection RLC delay model with the method of numerical analysis, the proposed analytical model has summed up the influence of the configuration of multilevel interconnections, the via heat transfer and self-heating effect on the interconnection delay, which is closer to the actual situation. Delay simulation results show that the proposed model has high precision within 5% errors for global interconnections based on the 65 nm CMOS interconnection and material parameter, which can be applied in nanometer CMOS system chip computer-aided design.

Keywords: multilevel interconnection, thermal distribution, RLC interconnection delay, current density

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1. Introduction

As the CMOS integrated circuits develop into nanometer level, the integrated devices and the metal interconnections scale down unceasingly, the current density and the number of layer of metal interconnection line further increase, the thermal issues of metal interconnections lines have become a major design consideration for high-performance integrated circuits including microprocessor.[1−7] The excessively high temperature and the non-uniform thermal distribution of interconnections may affect the clock signal of the circuits and degrade performance and reliability of chips. In particular, the use of low dielectric constant materials in recent years can reduce the interconnection parasitic capacitance, and thus reduce the interconnection delay, the dynamic power loss and the crosstalk, but the low thermal conductivity of low dielectric constant materials causes the interconnection temperature to raise sharply.[4,5] And then due to the fact that the resistance of metal interconnection will increase with temperature, the interconnection delay would increase acutely, leading to the exacerbated circuit performance. Regarding the complex interconnection network of nanometer level system chip, we find that the effect of parasitic capacitance and parasitic inductance is prominent day by day, so it is necessary to consider the influence of multilevel interconnection layout and the interconnection self-heating effect on the delay.

In view of the influence of temperature distribution effect on the interconnection delay, Ajami *et al.*[1] and Liu *et al.*[3] have studied the impact of interconnection temperature on the RC delay but not considered the inductance effect. Wang and Zhou[2] have considered the influence of via effect and fringe effect on interconnection temperature profile, and have obtained a multilevel interconnection thermal distribution quite close to the actual condition. However, it only takes via as a heat transfer channel rather than a heat source. The self-heating of via has already become a very important heat source in integrated circuits, and will affect the thermal distribution of interconnection, moreover, it may cause the temperature of both the sides of interconnection to be higher than the middle of interconnection,[6] so the via self-heating effect cannot be neglected for the nanometer level multilevel interconnections.[5] Reference [8] proposed an RLC interconnection delay analytical model based on the 1-D thermal distribution, which has considered the influence of the inductance effect and the temperature distribution effect on the delay, however, it has not considered the synthetical influence of the layout of multilevel interconnections, the via self-heating and the via effect as well as the fringe effect on the interconnection delay.

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This paper proposes a kind of multilevel interconnection temperature distribution model first, and has analysed the multilevel interconnection temperature distribution based on 65nm CMOS technological parameters. The third part of paper uses the modified one-pole RLC interconnection delay model with the method of numerical analysis, obtains the analytical RLC delay model which considers the thermal distribution of multilevel interconnections, and has validated and discussed the analytical RLC delay model of global interconnection based on 65nm CMOS interconnection and material parameters.

2. Thermal distribution model of multilevel interconnections

In the nanometer level CMOS process, the number of the layers of metal interconnection increases and the structure of interconnection is also getting more and more complex. According to ITRS2007,[9] the number of the layers of future metal interconnection will achieve 13 or more. In this case, it is very difficult to obtain an exact analytic expression of thermal distribution as those proposed in Ref. [1] for a more complex interconnection structure and huge interconnection network, furthermore, the via self-heating has already become a very important heat source of integrated circuit since the diameter of via further reduces in ultra large scale integrated circuit (ULSI),[5,6] therefore this paper takes via not only as a heat conduction channel, but also an important heat source which affects the interconnection temperature distribution.

A multilevel interconnection network is shown in Fig. 1. For the ith metal interconnection, assume the interconnection width is $w_{\mathrm{m},i}$, the line thick is $t_{\mathrm{m},i}$, the length is L_i, the spacing between the same level interconnection is d_i, the insulator thickness is h_i, the via diameter is D_i, generally speaking the via diameter may be smaller than or be equal to the width of interconnection, this paper takes the via diameter to be equal to the interconnection width, $T_i(x)$ is temperature profile along the length of the ith interconnection line, $T_{i-1}(x)$ is temperature profile along the length of the (i-1)th interconnection line, K_{ins} is the heat conductivity of insulator, K_{m} is the metal heat conductivity, and assume that the heat conductivity is constant,[1,2,6,8] $L_{\mathrm{D},i}$ is the heat diffusion length of interconnect, $J_{\mathrm{m},i}$ is the interconnection current density, ρ_{m} is the resistivity of metal at 0 °C, β is the temperature coefficient of metal resistivity, ρ_{v} is the via resistivity, $J_{\mathrm{v},i}$ is the via current density. Assume that the Joule heat produced by interconnections is divided into two parts, the Joule heat Q_{via} produced by the interconnection on the top of via and the self-heating of via $Q_{\mathrm{via,self\text{-}heat}}$ transmit directly through the via to its connected next metal, and the Joule heat produced by the other parts (Q_{ins}) transmits completely through the insulator to the next metal, then the expressions are as follows:[2]

$$\begin{aligned} & Q_{\mathrm{via,self\text{-}heat}} \\ &= \left(J_{\mathrm{v},i+1}\cdot\frac{\pi D_{i+1}^2}{4}\right)^2\cdot\left(\frac{\rho_{\mathrm{v}}\cdot h_{i+1}}{\frac{\pi D_{i+1}^2}{4}}\right), \end{aligned} \tag{1}$$

$$\begin{aligned} Q_{\mathrm{via}} &= \left(J_{\mathrm{m},i+1}\cdot w_{\mathrm{m},i+1}\cdot t_{\mathrm{m},i+1}\right)^2 \\ &\quad\times\left(\frac{\rho_{\mathrm{m}}\cdot L_{\mathrm{D},i+1}}{w_{\mathrm{m},i+1}\cdot t_{\mathrm{m},i+1}}\right) \\ &= J_{\mathrm{m},i+1}^2\cdot\rho_{\mathrm{m}}\cdot L_{\mathrm{D},i+1}\cdot w_{\mathrm{m},i+1}\cdot t_{\mathrm{m},i+1}, \end{aligned} \tag{2}$$

$$Q_{\mathrm{via}}^* = Q_{\mathrm{via,self\text{-}heat}} + Q_{\mathrm{via}}, \tag{3}$$

$$\begin{aligned} Q_{\mathrm{ins}} &= L_i\cdot w_{\mathrm{m},i}\Big\{J_{\mathrm{m},i+1}^2\cdot\rho_{\mathrm{m}} \\ &\quad\times t_{\mathrm{m},i+1}\cdot\frac{w_{\mathrm{m},i+1}}{w_{\mathrm{m},i+1}+d_{i+1}} \\ &\quad\times\frac{L_{i+1}-2\cdot L_{\mathrm{D},i+1}}{L_{i+1}} \\ &\quad+\sum_{j=i+2}^{n}\left(J_{\mathrm{m},j}^2\cdot\rho_{\mathrm{m}}\cdot t_{\mathrm{m},j}\cdot\frac{w_j}{w_j+d_j}\right)\Big\}, \end{aligned} \tag{4}$$

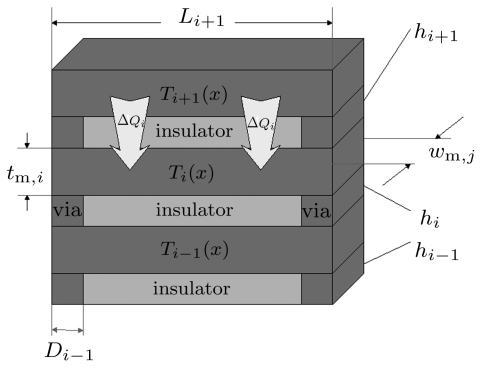


Fig. 1. Schematic diagram of multilevel interconnection structure.

Then the heat transmitted by the upper layer interconnections is

$$\Delta Q_i = 2\cdot Q_{\mathrm{via}}^* + Q_{\mathrm{ins}}. \tag{5}$$

We can obtain the heat generated by the ith metal interconnection line as [1]

$$\begin{aligned} p_{\mathrm{g}}(x) &= \left(J_{\mathrm{m},i}\cdot w_{\mathrm{m},i}\cdot t_{\mathrm{m},i}\right)^2\cdot r(x) \\ &= \left(J_{\mathrm{m},i}\cdot w_{\mathrm{m},i}\cdot t_{\mathrm{m},i}\right)^2 \end{aligned}$$

$$\times \frac{\rho_{\rm m} \cdot L_i}{w_{{\rm m},i} \cdot t_{{\rm m},i}} \left(1 + \beta \cdot T_i\left(x\right)\right). \quad (6)$$

On the other hand, energy losses due to the heat transfer between the ith interconnection and the $(i-1)$th metal through the insulator is:

$$p_l\left(x\right) = \frac{T_i\left(x\right) - T_{i-1}\left(x\right)}{R_{{\rm T},i}} = \left(T_i\left(x\right) - T_{i-1}\left(x\right)\right) \cdot \frac{k^*_{{\rm ins,eff},i} w_{{\rm m},i} \cdot L_i}{h_i}. \quad (7)$$

Where $R_{{\rm T},i}$ is the insulator thermal resistance, and

$$k^*_{{\rm ins,eff},i} = k_{\rm ins} \cdot \frac{h_i}{w_{{\rm m},i}} \cdot 1.685 \times \left[\log\left(1 + \frac{h_i}{w_{{\rm m},i}}\right)\right]^{-0.59} \cdot \left(\frac{h_i}{t_{{\rm m},i}}\right)^{-0.078}$$

is a kind of more precise effective insulator thermal conductivity proposed by Andrews,[10] in the deep submicron CMOS process, it is more accurate in comparison with the effective thermal conductivity of quasi-two-dimensional model.[1]

Therefore the net heat energy generated per unit volume of the ith metal interconnection line is

$$Q^*_i = \frac{p_{\rm g}\left(x\right) + \Delta Q_i - p_l\left(x\right)}{w_{{\rm m},i} \cdot t_{{\rm m},i} \cdot L_i}. \quad (8)$$

Thus the summarized stable interconnection heat flow equation can be written as

$$\frac{{\rm d}^2 T_i\left(x\right)}{{\rm d}x^2} = -\frac{Q^*_i}{k_{\rm m}} = \frac{1}{L^2_{{\rm D},i}}\left(T_i\left(x\right) - T_{i-1}\left(x\right)\right) - \left(\theta_i + \frac{\Delta Q_i}{k_{\rm m} w_{{\rm m},i} t_{{\rm m},i} L_i}\right), \quad (9)$$

where

$$\frac{1}{L^2_{{\rm D},i}} = \frac{1}{k_{\rm m}}\left(\frac{k^*_{{\rm ins,eff},i}}{t_{{\rm m},i} h_i} - J^2_{{\rm m},i}\rho_{\rm m}\beta\right), \quad \theta_i = \frac{J^2_{{\rm m},i}\rho_{\rm m}}{k_{\rm m}}.$$

In order to simplify the computation, assume that the temperature of the $(i-1)$th interconnection line is constant ($T_{i-1}(x) = T_{{\rm avg},i-1}$), then solve Eq. (9), we can obtain the temperature profile and the average temperature of the ith metal interconnection respectively:

$$T_i\left(x\right) = T_{{\rm avg},i-1} + L^2_{{\rm D},i} \cdot \left(\theta_i + \frac{\Delta Q_i}{k_{\rm m} w_{{\rm m},i} t_{{\rm m},i} L_i}\right) \times \left(1 - \frac{\sinh\frac{x}{L_{{\rm D},i}} + \sinh\frac{L_i - x}{L_{{\rm D},i}}}{\sinh\frac{L_i}{L_{{\rm D},i}}}\right), \quad (10)$$

$$T_{{\rm avg},i} = T_{{\rm avg},i-1} + L^2_{{\rm D},i} \cdot \left(\theta_i + \frac{\Delta Q_i}{k_{\rm m} w_{{\rm m},i} t_{{\rm m},i} L_i}\right) \times \left(1 - \frac{\tanh\frac{L_i}{2L_{{\rm D},i}}}{\frac{L_i}{2L_{{\rm D},i}}}\right). \quad (11)$$

3. RLC delay model considering multilevel interconnections thermal distribution

A distributed RLC transmission line model with the length of L is shown in Fig. 2, r, l and c are its resistance, inductance and capacitance per unit length interconnection respectively, the source is modeled as a resistance $R_{\rm s}$ and capacitance $C_{\rm p}$, the load at the end of the interconnection is modeled by using capacitance $C_{\rm L}$.

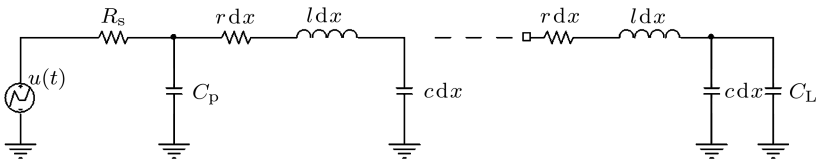


Fig. 2. A distributed RLC transmission line model.

Thus, the transfer function for the interconnection line of Fig. 2 is[11]

$$H\left(s\right) = \frac{V_{\rm out}\left(s\right)}{V_{\rm in}\left(s\right)} = \frac{1}{\left[\cosh\left(\theta L\right) + \frac{Z_{\rm s}}{Z_0}\sinh\left(\theta L\right)\right] + \frac{1}{Z_{\rm L}}\left[Z_0\sinh\left(\theta L\right) + Z_{\rm s}\cosh\left(\theta L\right)\right]}, \quad (12)$$

where $\theta = \sqrt{(r+sl)\,sc}$ is the propagation constant, $Z_0 = \sqrt{(r+sl)/sc}$ is the characteristic impedance, $Z_{\rm L} = 1/sC_{\rm L}$ is the capacitive impedance of load, and $Z_{\rm s} = R_{\rm s} + 1/sC_{\rm p}$ is the source impedance.

We truncate the transfer function by expanding the hyperbolic functions around $s = 0$, collecting terms up to the coefficient of s^2 in the denominator, we obtain the truncated transfer function as

$$H(s) \approx 1/\left(1 + sb_1 + s^2 b_2\right), \tag{13}$$

where

$$b_1 = R_{\rm s}(C_{\rm p} + C_{\rm L} + cL) + \frac{rcL^2}{2} + rLC_{\rm L}, \tag{14}$$

$$b_2 = \frac{rcL^2}{6}(R_{\rm s}cL + rLC_{\rm L}) + \frac{lcL^2}{2} + \frac{\left(rcL^2\right)^2}{24} + \frac{rcL^2}{2}R_{\rm s}(C_{\rm p} + C_{\rm L}) + lLC_{\rm L} + rLR_{\rm s}C_{\rm p}C_{\rm L}. \tag{15}$$

In order to reduce the computation complexity, this paper uses the modified one-pole (first order) transfer function model which is proposed in Ref. [12]:

$$H(s) \approx 1/1 + b_1' s, \tag{16}$$

where $b_1' = b_1 + b_2/b_1$.

Although this is a first order function, its precision is close to the precision of the second order function actually, and its stability is better, a compromise of both precision and stability.

Thus we can get the step response $V_{\rm out}(s) = V_{\rm in}(s) \cdot H(s) = (V_0/s)(1/(1 + b_1' s))$, then obtain $V_{\rm out}(t)$ by using the inverse Laplace transform, and the 90% delay threshold as follows:

$$\tau_{0.9} = 2.30 \cdot b_1'. \tag{17}$$

Table 1. The interconnection parameters of 65 nm CMOS process.[13]

	wire width $w_{\rm m}$	wire thick tm	spacing d	insulator thick h	ε
local interconnect	0.10 μm	0.20 μm	0.10 μm	0.20 μm	2.2
intermediate interconnect	0.14 μm	0.35 μm	0.14 μm	0.20 μm	2.2
global interconnect	0.45 μm	1.20 μm	0.45 μm	0.20 μm	2.2

The delay of intermediate interconnection and local interconnection is smaller in comparison with the global interconnection,[1,9] and it has a smaller impact on the performance of integrated circuits, therefore this paper mainly analyses the delay of the global interconnection line. Assume that M1 is the local interconnection line, M2–M4 are intermediate interconnection lines, M5–M9 are global interconnection lines, the lengths of each layer interconnection: 10, 20, 40, 80, 200, 400, 800, 1000 and 2000 μm respectively. According to the data provided by ITRS2007,[9] thermal conductivity of Cu ($K_{\rm m}$) is 386 W/(m·K), thermal conductivity of insulator ($K_{\rm ins}$) is 0.12 W/(m·K), temperature coefficient of Cu (β) is 4.3×10^{-3}/°C, the resistivity is $2.2\times10^{-8}\Omega$·m. Assume that all metal lines are electrified and achieve the limiting current density 9.95×10^9 A/m^2, and uniform substrate temperature is set at 105 °C, then we can obtain the temperature profile of each layer through simulating the nine-layer interconnection lines based on the BPTM[13] 65 nm CMOS process of Table 1 with Eqs. (10) and (11). The temperature profile of global interconnection line (M8) is shown in Fig. 3.

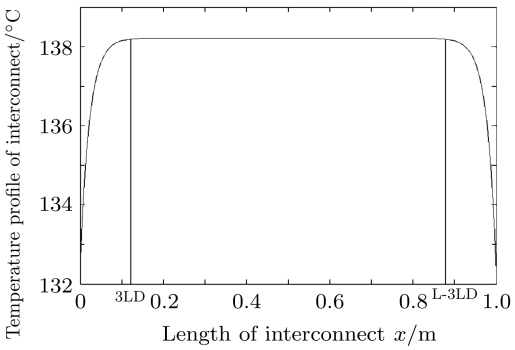


Fig. 3. Temperature profile of global interconnection line (M8).

The results of computation indicate that for the global interconnection line (for example M8), when $x = 3L_{\rm D}$, $T \approx 0.9979 \cdot T_{\max}$, therefore we may consider that the interconnection line has achieved maximum temperature when $x = 3L_{\rm D}$.[8]

Since Eqs. (14) and (15) have not included the influence of the temperature distribution effect, the

paper modifies them as follows:

$$b_1^* = R_{\rm s}\left(C_{\rm p}+C_{\rm L}+cL\right)+\eta+\lambda, \tag{18}$$

$$b_2^* = \frac{\eta}{3}\left(R_{\rm s}cL+\lambda\right)+\frac{lcL^2}{2}+\frac{(\eta)^2}{6}+\eta R_{\rm s}\left(C_{\rm p}+C_{\rm L}\right) + lLC_{\rm L}+\lambda R_{\rm s}C_{\rm p}, \tag{19}$$

where $\eta = \int_0^L r\left(x\right)c\left(L-x\right){\rm d}x$, $\lambda = \int_0^L r\left(x\right)C_{\rm L}{\rm d}x$, $r(x)=r_0(1+\beta\cdot T(x))$, r_0 is the resistance of the unit length interconnection line at 0°, and $T(x)$ is the interconnection line temperature profile.

Due to the complex interconnection network of the nanometer level system chip, the modified RLC delay model has an integral module, which is difficult to solve and will seriously influence the velocity and efficiency of simulation, this paper uses the method of numerical integration to simplify it.

Based on the interconnection temperature profile shown in Fig. 3, we divide the interconnection line into three sections. One of them the temperature is always constant, and the temperature of the other two sections is variable, then it is possible to obtain the simplified delay expression with the Newton–Cotes numerical integration formula (takes $n=4$) as

$$\eta = \eta_1+\eta_2+\eta_3, \tag{20}$$

where

$$\begin{aligned}
\eta_1 &= \int_0^{3L_D} f\left(x\right){\rm d}x \approx \frac{3L_D}{90}\left[7f\left(0\right)+32f\left(\frac{3}{4}L_D\right)+12f\left(\frac{6}{4}L_D\right)+32f\left(\frac{9}{4}L_D\right)+7f\left(3L_D\right)\right],\\
\eta_2 &= \int_{3L_D}^{L-3L_D} f\left(x\right){\rm d}x = r_0c\left(1+\beta T_{\max}\right)\frac{\left[\left(L-3L_D\right)^2-\left(3L_D\right)^2\right]}{2},\\
\eta_3 &= \int_{L-3L_D}^{L} f\left(x\right){\rm d}x \approx \frac{3L_D}{90}\left[7f\left(L-3L_D\right)+32f\left(L-\frac{9}{4}L_D\right)+12f\left(L-\frac{6}{4}L_D\right)\right.\\
&\quad \left.+32f\left(L-\frac{3}{4}L_D\right)+7f\left(L\right)\right],\\
f\left(x\right) &= r\left(x\right)c\left(L-x\right) = r_0c\left(1+\beta\cdot T\left(x\right)\right)\left(L-x\right).
\end{aligned}$$

Using the same method we may obtain

$$\lambda = \lambda_1+\lambda_2+\lambda_3, \tag{21}$$

where

$$\begin{aligned}
\lambda_1 &= \int_0^{3L_D} g\left(x\right){\rm d}x \approx \frac{3L_D}{90}\left[7g\left(0\right)+32g\left(\frac{3}{4}L_D\right)+12g\left(\frac{6}{4}L_D\right)+32g\left(\frac{9}{4}L_D\right)+7g\left(3L_D\right)\right],\\
\lambda_2 &= \int_{3L_D}^{L-3L_D} g\left(x\right){\rm d}x = \left(L-6L_D\right)r_0\left(1+\beta\cdot T_{\max}\right)\cdot C_{\rm L},\\
\lambda_3 &= \int_{L-3L_D}^{L} g\left(x\right){\rm d}x \approx \frac{3L_D}{90}\left[7g\left(L-3L_D\right)\right.\\
&\quad \left.+32g\left(L-\frac{9}{4}L_D\right)+12g\left(L-\frac{6}{4}L_D\right)+32g\left(L-\frac{3}{4}L_D\right)+7g\left(L\right)\right],\\
g\left(x\right) &= r\left(x\right)C_{\rm L} = r_0\left(1+\beta\cdot T\left(x\right)\right)\cdot C_{\rm L}.
\end{aligned}$$

The Newton–Cotes formula used for sections with variable temperature has quintic algebra precision and has high stability. According to Eqs. (10), (11) and (17)–(21), we can obtain a precise RLC delay considering temperature profile of multilevel interconnections.

Table 2. Parasitic capacitance and parasitic inductance of different insulator thickness.

insulator thickness h/μm	0.20	0.25	0.30	0.35	0.40	0.45	0.50
capacitance per unit length/(fF/μm)	0.20594	0.19465	0.187996	0.18378	0.18098	0.17906	0.17773
inductance per unit length/(pH/μm)	1.52	1.52	1.52	1.52	1.52	1.52	1.52

Analysing the eighth interconnection line (M8), we can obtain the inductance and the capacitance per unit length of different insulator thickness of the 65nm process with the parasitic inductance and parasitic capacity extraction method of the BPTM model,[13−16] which is shown in Table 2. Then we can obtain comparison results shown in Table 3 using Matlab software to simulate the proposed model.

Table 3. Comparison of interconnection delay.

R_S	C_p/pf	C_L/pf	proposed model/ps	the delay of temperature unawareness/ps	error
10	0.5	0.176	109.9	108.1	1.64%
20	0.5	0.176	125.1	122.1	2.4%
10	5	0.176	209.1	204	2.44%
20	5	0.176	330.8	325	1.75%
10	0.5	1.76	393.4	375.4	4.58%
20	0.5	1.76	451	429.9	4.68%
10	5	1.76	548	524.5	4.29%
20	5	1.76	732.5	705.5	3.69%

In Table 3, the delay of temperature unawareness is the RLC delay which is obtained with the Eqs. (14), (15) and (17) at the reference temperature (substrate temperature), the error is relative to the model proposed in the paper. The simulation results indicate that the RLC delay which does not consider the temperature distribution effect has underestimated the interconnection delay.

Figure 4 shows the relationship between the interconnection delay and the insulator thickness of the multilevel interconnection under different current densities, where $J_1 = 9.95 \times 10^9$ A/m^2, $J_2 = 1.20 \times 10^{10}$ A/m^2, $J_3 = 1.37 \times 10^{10}$ A/m^2, $J_4 = 1.72 \times 10^{10}$ A/m^2, $J_5 = 2.0 \times 10^{10}$ A/m^2 and $J_6 = 2.2 \times 10^{10}$ A/m^2, the drive resistance is 20 Ω, the drive capacitance is 5pf, and the load capacitance is 0.176 pf. Figure 4 shows that the interconnection delay increases with the current density when the insulator thickness is constant; when the current density is low, the interconnection delay decreases if the thickness of each insulator layer increases simultaneously. The reason is that although the increase of the thickness of each insulator layer deteriorates the heat dispersion of interconnection line, causing the temperature to rise sharply, the increase of insulator thickness will lead the parasitic capacitance of interconnection line to reduce (as shown in Table 2). And also, the effect of parasitic capacitance will be the major factor to affect the interconnection delay when the current density is low, so the interconnection delay will reduce; as the current density increases, the interconnection line and the via self-heating effect are getting more and more severe, which become the dominant factor influencing RLC delay, and cause the interconnection delay to increase. The variety of the structure of interconnection will not only impact the heat dispersion of interconnection line, but also change the parasitic capacitance and the parasitic inductance of the interconnection line, thus influence interconnection delay. The influence of the effect of interconnection self-heating on delay will get more and more fierce along with the increase of current density of the nanometer level ICs, so it is necessary to precisely analyse the influence of multilevel interconnection temperature distribution effect on the RLC delay.

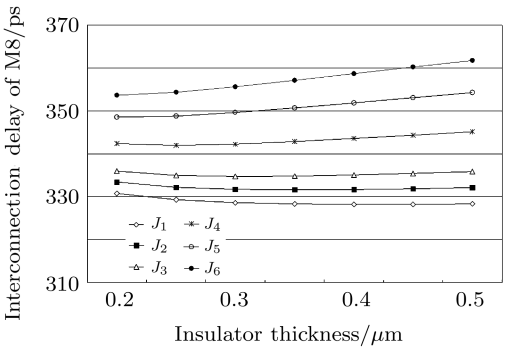


Fig. 4. The relationship of interconnection delay and insulator thickness with different current density.

4. Conclusion

As the size of the ULSI scales down continuously, the influence of the effect of interconnection self-heating on delay receives more and more attention. This paper proposes a novel RLC delay model considering the thermal distribution of nanometer level multilevel interconnection with numerical analysis according to the actual temperature distribution condition of the multilevel interconnections. The analytical delay model obtained not only considers the temperature effect but also is a simple and stable model. It can be used in analysing the influence of the structure of multilevel interconnections on the interconnection delay and applied in the design, optimization and synthesis of nanometer level integrated circuits. The proposed model is very valuable in practical applications.

References

[1] Ajami A H, Banerjee K and Pedram M 2005 *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* **24** 849

[2] Wang N L and Zhou R D 2004 *J. Semiconductors* **25** 1510

[3] Liu E X, Li E P and Wei X C 2008 *2008 Electrical Design of Advanced Packaging and Systems Symposium* December 10–12, 2008 Seoul, South Korea, p171

[4] Banerjee K, Amerasekera A and Dixit G 1996 *IEEE International Electron Devices Meeting* December 8-11, 1996 San Francisco, USA, p65

[5] Chiang T Y and Saraswat K C 2003 *2003 Symposium on VLSI Technology and Circuits* April 23-25, 2003 Kyoto, Japan, p275

[6] Pei S W, Huang H and He X S 2006 *Microelectronics* **36** 385

[7] Zhu Z M, Qian L B and Yang Y T 2009 *Chin. Phys.* B **18** 1188

[8] Yang Y T, Leng P and Dong G 2008 *J. Semiconductors* **29** 1843

[9] Semiconductor Industry Association 2007 *International Technology Roadmap for Semiconductors*

[10] Andrews R V 1955 *Chem. Eng. Prog.* **51** 67

[11] Kahng A B and Muddu S 1997 *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* **16** 1507

[12] Yu Q J and Kuh E S 2001 *Proc. IEEE* **89** 772

[13] http://www.eas.asu.edu/∼ptm/

[14] Li X, Wang J M and Tang W Q 2009 *Acta Phys. Sin.* **58** 3603 (in Chinese)

[15] Wu Z M, Lei Q S, Geng X H, Zhao Y, Sun J and Xi J P 2006 *Chin. Phys.* **15** 1320

[16] Zhang Z G, Guo S X, Gao F L, Yu S Y and Li X Y 2009 *Acta Phys. Sin.* **58** 2772 (in Chinese)