A novel partial silicon on insulator high voltage LDMOS with low-k dielectric buried layer*

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A novel partial silicon-on-insulator (PSOI) high voltage device with a low-k (relative permittivity) dielectric buried layer (LK PSOI) and its breakdown mechanism are presented and investigated by MEDICI. At a low k value the electric field strength in the dielectric buried layer ($E_{\rm I}$) is enhanced and a Si window makes the substrate share the vertical drop, resulting in a high vertical breakdown voltage; in the lateral direction, a high electric field peak is introduced at the Si window, which modulates the electric field distribution in the SOI layer; consequently, a high breakdown voltage (BV) is obtained. The values of $E_{\rm I}$ and BV of LK PSOI with $k_{\rm I} = 2$ on a 2 μm thick SOI layer over 1 μm thick buried layer are enhanced by 74% and 19%, respectively, compared with those of the conventional PSOI. Furthermore, the Si window also alleviates the self-heating effect.

Keywords: silicon-on-insulator, low k dielectric, electric field, breakdown voltage

PACC: 7340T, 7390, 736H

1. Introduction

The advantages of silicon-on-insulator (SOI) technology such as superior isolation, high speed and low loss have attracted much attention. However, SOI technology suffers a low vertical breakdown voltage ($\rm BV_{ver}$) and self-heating effect (SHE). Many SOI device structures have been proposed to improve $\rm BV_{ver}$ by enhancing the electric field strength in the dielectric buried layer ($E_{\rm I}$), in which the buried layer is exclusively made of silicon dioxide.[1−10] Although SOI high voltage devices with the variable low-k dielectric buried layer (VLKD SOI) can improve BV, its SHE is aggravated due to the lower thermal conductivity (κ) of low-k (LK) dielectrics than that of dioxide in the conventional SOI.[11,12] Partial SOI (PSOI) technology can increase the BV and reduce the SHE because of its Si window.[10,13,14]

In the present paper, a novel low-k dielectric buried layer high voltage LDMOS on partial SOI is proposed and its breakdown characteristics are discussed. The value of BV is improved because of the enhancement of $E_{\rm I}$ as well as the modulation effects of both the low k dielectric and the Si window on the electric field in the SOI layer. The SHE in LK PSOI is investigated as well.

2. Structure and mechanism

The cross sections of LK PSOI and conventional PSOI (CPSOI) LDMOSFETs (lateral double- diffused metal-oxide-semiconductor field-effect-transistors) are shown in Fig. 1. A dielectric with a low k value (< 3.9) and high critical field strength is used as the buried layer in LK PSOI compared with silicon dioxide in the CPSOI. Denote $t_{\rm S}$ and $t_{\rm I}$ as the thicknesses of SOI and buried layers, respectively, $N_{\rm d}$ and $N_{\rm sub}$ as the doping concentrations of the SOI layer and substrate, $L_{\rm d}$, $L_{\rm W}$ and L as the lengths of drift region, Si window and the device, respectively. The x-direction and the y-directions are given in Fig. 1. A conventional SOI (CSOI) is the CPSOI with $L_{\rm W} = 0$.

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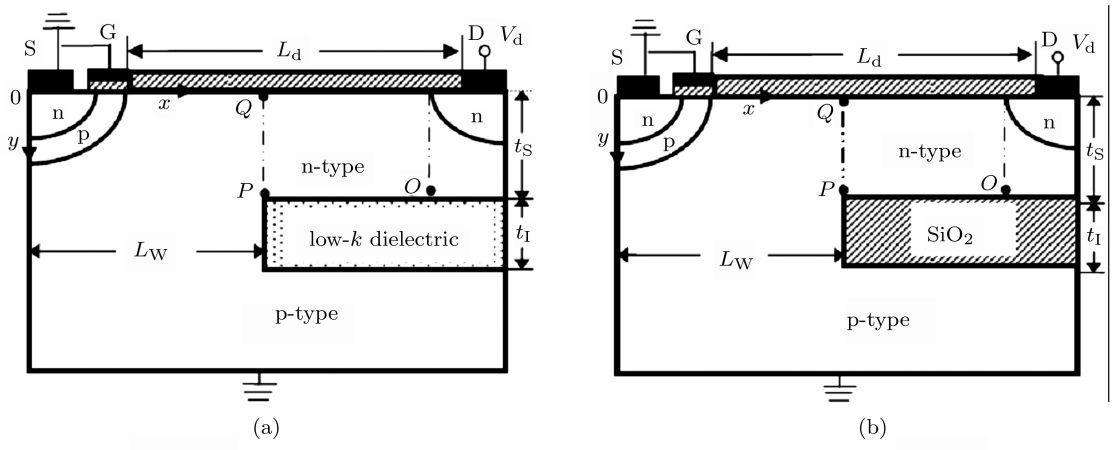


Fig. 1. Cross sections of LDMOSFETs (V_d is the applied voltage): (a) LK PSOI, and (b) CPSOI.

The value of BV is determined by a smaller value between the lateral and the vertical breakdown voltages: BV_{lat} and BV_{ver}. The field plates and the reduced surface field (RESURF) technology are used to improve the BV_{lat} as employed in bulk silicon devices. The value of BV for an LK PSOI device is therefore determined by BV_{ver}. According to the vertical breakdown theory and the assumptions for SOI devices in Ref. [2], we obtain an approximate formula for BV of PSOI devices, i.e.

$$BV = 0.5 t_S E_S + E_I t_I + V_{sub}, \tag{1}$$

where

$$E_I = E_S k_S / k_I, \tag{2}$$

E_S and E_I represent the field strengths of the SOI layer and the dielectric buried layer at their interface under the drain, respectively. The first and second items on the right-hand side in Eq. (1) are the voltage drops across the SOI layer and the buried layer, denoted as V_S and V_I. Voltage V_{sub} is the voltage sustained by the substrate and $V_{sub} = 0$ for SOI devices. Equation (2) represents the continuity of the electric displacement on the Si / buried layer interface; and k_S and k_I are the relative permittivities of Si and buried layer respectively.

A Si window makes the substrate share the vertical voltage drop and modulates the electric field distribution in the Si layer. Moreover it offers a heat conduction path. Both of them result in a high BV and a reduced SHE for the LK PSOI LDMOS.

3. Results and discussion

All simulation results are obtained by MEDICI in this paper. Figure 2 shows the electric field and potential distributions in the y-direction under the drain for LK PSOI with $k_I = 2, 3$ and the CPSOI ($k_I = 3.9$) and CSOI ($k_I = 3.9$) LDMOSFETs. For LK PSOI with $k_I = 2$ and $L_W = 25$ μm, E_I increases from 94 V/μm of the CPSOI to 164 V/μm at breakdown, and BV from 315 V to 375 V. The values of E_I and BV are increased by 74% and 19%, respectively. By comparison with their electric field distributions at $V_d = 315$ V, the modulation effect of low-k dielectric makes E_I increase from 94 V/μm of the CPSOI to 121 V/μm of LK PSOI and E_S decrease from 28 V/μm to 20 V/μm, which enhances V_I and avoids a premature breakdown in Si layer, leading to a high BV. E_I, V_I and BV increase with k_I decreasing for all PSOI LDMOSFETs as illustrated in Figs. 2(a) and 2(b). 43.7% and 48.5% of BV are shared by the buried layer and the substrate for LK PSOI with $k_I = 2$, respectively, while 30% and 59.4% for the CPSOI. For the CPSOI, most of the BV is supported by the substrate with a low N_{sub} and the BV will greatly decrease if N_{sub} increases. In Fig. 2(a), although E_I for the CSOI is higher than that of the CPSOI because its continuous buried oxide prevents potential lines from extending into the substrate, V_{sub} equals zero and therefore BV for the CSOI is lowest.

Figure 3 gives the electric field distributions in the x-direction. Their optimum values of L_W are 25 μm, 27 μm and 29 μm for PSOI LDMOSFETs with $k_I = 2$, 3 and 3.9, respectively (as illustrated in Fig. 5(a)). In Fig. 3(a), new interface electric field peaks P_1, P_2 and P_3 are generated at the end of the dielectric buried layer (P point in Fig. 1) because of the difference in

permittivity between the Si and the buried layer. The smaller the value of $k_{\rm I}$ is, the higher the peak will be. Surface field peaks Q_1, Q_2 and Q_3 are introduced due to the coupling effect of peaks P_1, P_2 and P_3, which optimizes the electric field distribution in the SOI layer and thus improves the $\rm BV_{lat}$. The highest peaks P_1 and Q_1 result in the highest BV for LK PSOI with $k_{\rm I} = 2$.

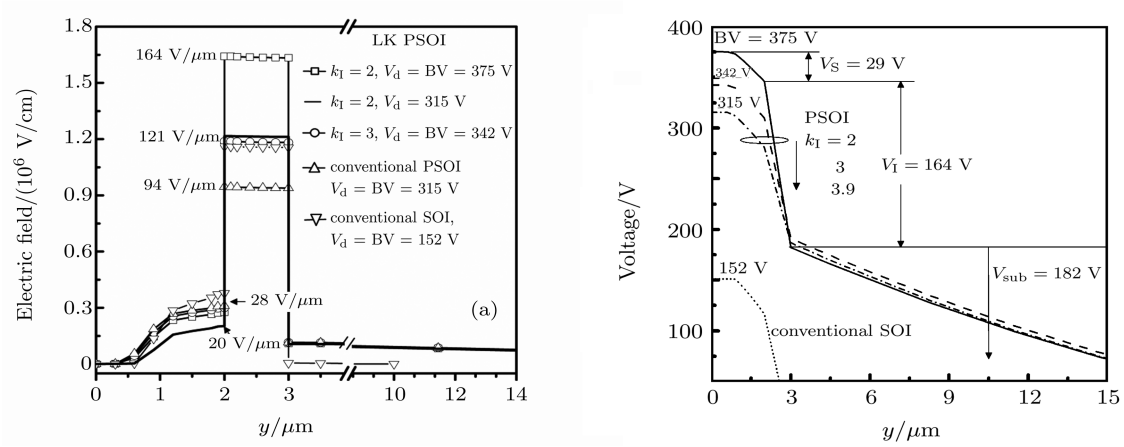


Fig. 2. Electric field (a) and potential (b) distributions in y-direction under the drain ($t_{\rm I} = 1$ μm, $t_{\rm S} = 2$ μm, $L_{\rm d} = 30$ μm, $L = 40$ μm, $N_{\rm sub} = 2\times10^{14}$ cm^{-3}).

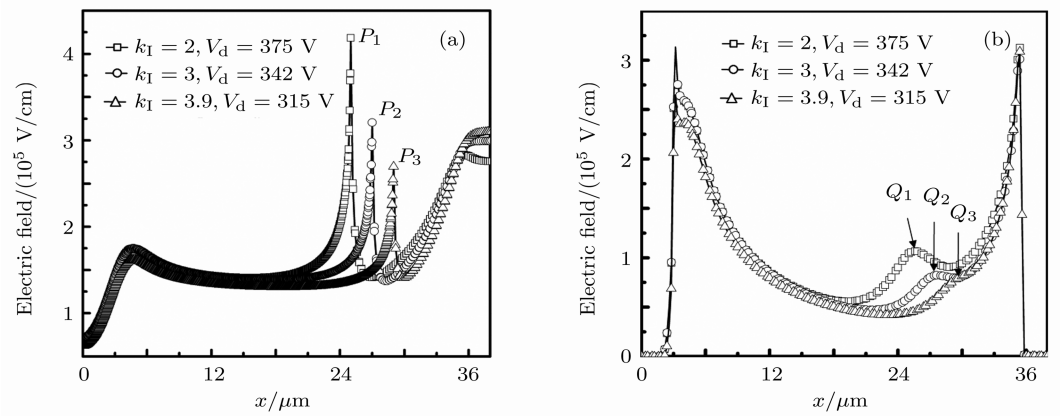


Fig. 3. Electric field distributions ($t_{\rm I} = 1$ μm, $t_{\rm S} = 2$ μm, $L_{\rm d} = 30$ μm, $L = 40$ μm, $N_{\rm sub} = 2\times10^{14}$ cm^{-3}) on the interface of the Si/ buried layer (a) and surface (b).

Figure 4 shows the effects of $k_{\rm I}$ on the fields at O, P and Q points in Fig. 1 as well as the maximum BV ($\rm BV_{max}$) for PSOI devices with their own optimal $L_{\rm W}$ and $N_{\rm d}$. The fields at O, P and Q points and $\rm BV_{max}$ increase with $k_{\rm I}$ decreasing at $k_{\rm I} \geq 2$. However, a premature breakdown at P point, caused by a large difference in permittivity between the Si and the low-k dielectric, leads to a low BV at $k_{\rm I} = 1.5$. So $2 \leq k_{\rm I} \leq 3$ is an optimal range.

Figure 5 (a) shows the dependence of BV on $L_{\rm W}$ as a function of $k_{\rm I}$. The values of BV first increase and then decrease with $L_{\rm W}$ increasing for all PSOI LDMOSFETs. It can be explained by Fig. 5(b). The value of $V_{\rm I}$ decreases while $V_{\rm sub}$ increases due to the

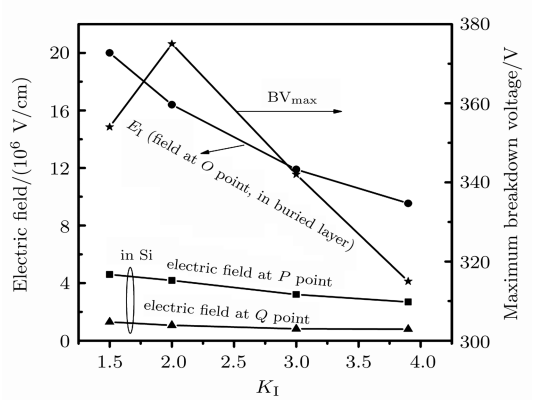


Fig. 4. Dependences of the fields at O, P and Q points as well as $\rm BV_{max}$ on $k_{\rm I}$ ($t_{\rm I} = 1$ μm, $t_{\rm S} = 2$ μm, $L_{\rm d} = 30$ μm, and $N_{\rm sub} = 2\times10^{14}$ cm^{-3}).

deep extension of the depletion region in the substrate with $L_{\rm W}$ increasing, and $V_{\rm S}$ almost keeps constant if the SOI layer is fully depleted, which is illustrated Fig. 5(b). The value of BV begins to decrease when the decrement in $V_{\rm I}$ exceeds the increment in $V_{\rm sub}$. Figure 5(a) also indicates that BV increases and the optimum $L_{\rm W}$ decreases with the decrease of $k_{\rm I}$ because a lager percentage of BV is shared by a buried layer with a lower k value. The value of $V_{\rm sub}$ decreases with $N_{\rm sub}$ increasing, so does BV in Fig. 5(a). In Fig. 5(b), $V_{\rm S}$ of LK PSOI is slightly lower than that of the CP-SOI due to its low field in the SOI layer (in Fig. 2(a)).

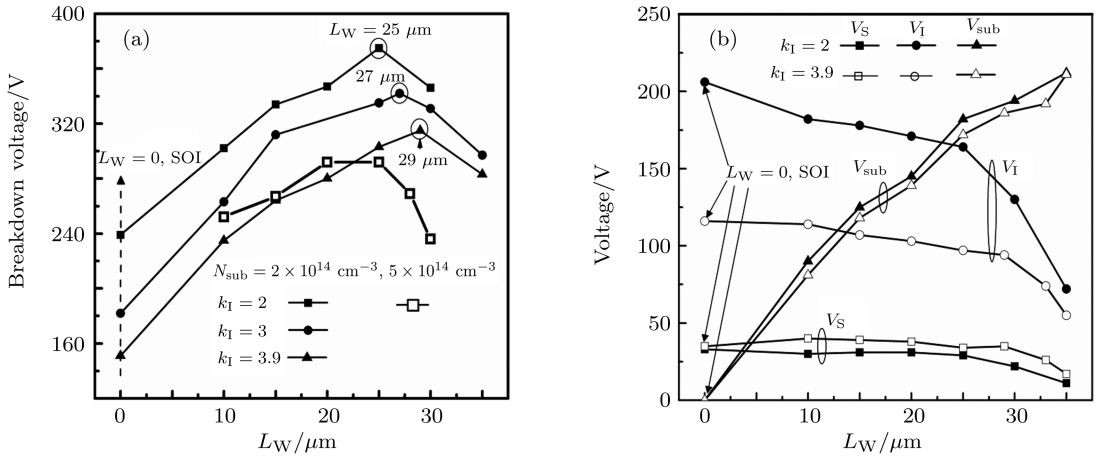


Fig. 5. Dependences of BV on $L_{\rm W}$ ($t_{\rm S}$ = 2 μm, $t_{\rm I}$ = 1 μm, $L_{\rm d}$ = 30 μm, L = 40 μm). Panel (a) shows dependence of BV on $L_{\rm W}$ as a function of $k_{\rm I}$, and panel (b) exhibits dependences of $V_{\rm S}$, $V_{\rm I}$ and $V_{\rm sub}$ under the drain on $L_{\rm W}$.

Figure 6(a) shows the influence of $N_{\rm d}$ on BV as a function of $L_{\rm W}$. The big open circles represent maximal values of BV ($\rm BV_{max}$) of LK PSOI for some given structure parameters, and the corresponding $N_{\rm d}$ is named $N_{d,o}$. The depletion region into the substrate widens with $L_{\rm W}$ increasing, which not only enhances $V_{\rm Sub}$, but also relieves the surface field peak at the drain and thus avoids the premature breakdown there, and even the SOI layer is not fully depleted for a large $L_{\rm W}$. Consequently, $\rm BV_{max}$ first increases and then decreases and $N_{\rm d,o}$ monotonically decreases with $L_{\rm W}$ increasing. Figure 6(b) gives the surface field distributions at breakdown for LK PSOI LDMOSFETs with different values of $L_{\rm W}$ at $N_{\rm d} = 6 \times 10^{15}$ cm^{-3}. Doping concentration $N_{\rm d}$ of 6×10^{15} cm^{-3} is so high that the drift region is not fully depleted for LK PSOI with $L_{\rm W}$ = 25 μm and it is too low for LK PSOI with $L_{\rm W}$ = 0 μm, but it is optimal for LK PSOI with $L_{\rm W}$ = 10 μm. This is determined by the RESURF effect as done in CPSOI and CSOI devices.[11,15]

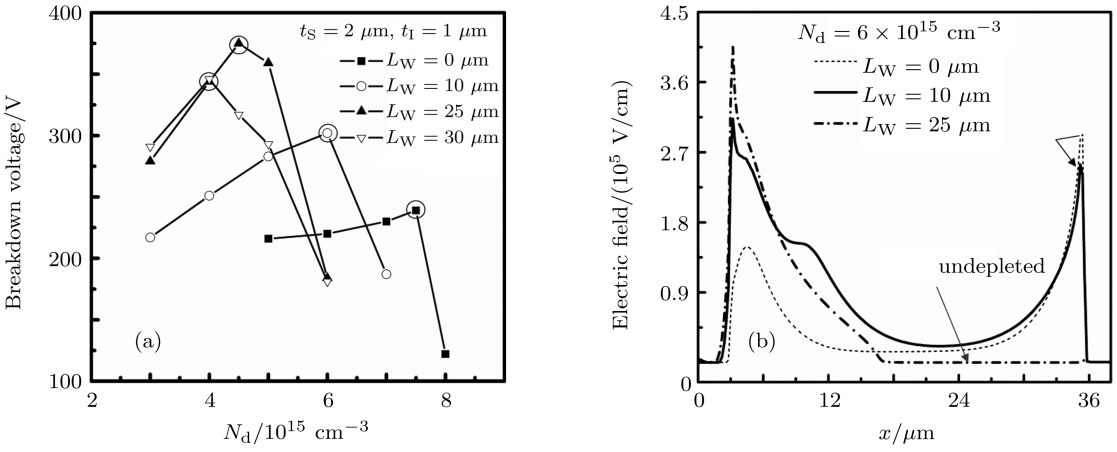


Fig. 6. Effects of $N_{\rm d}$ on BV (a) and surface field distributions at breakdown with $N_{\rm d} = 6 \times 10^{15}$ cm^{-3} (b) for different values of $L_{\rm W}$.

Figure 7 indicates the effects of $L_{\rm W}$ on $\rm BV_{max}$ and maximal temperature $T_{\rm max}$ at a power of 1 mW/μm in the on-state condition. The substrate temperature and the gate voltage ($V_{\rm G}$) are 300 K and 15 V in simulating heat dissipation, respectively. Because the values of κ for most low-k dielectrics are 13–7 times smaller than that of thermally grown SiO_2 (1.4 W/(cm·K)), the κ of 0.15 W/(cm·K) is defined in simulation.[12,16] Figure 7 shows that $T_{\rm max}$ decreases monotonically with the increase of $L_{\rm W}$ due to a widened heat conduction path. However, BV first increases and then decreases. So at an optimal $L_{\rm W}$ a tradeoff between $\rm BV_{max}$ and $T_{\rm max}$ can be obtained. The optimal value of $L_{\rm W}$ is 25 μm, i.e. $L_{\rm W} = 25$ μm for LK PSOI with $k_{\rm I} = 2$. LK SOI (LK PSOI at $L_{\rm W} = 0$) has the lowest BV and the highest $T_{\rm max}$.

The surface temperature profiles and three-dimensional (3D) temperature distributions are given in Fig. 8. The Si window results in a low temperature in PSOI LDMOSFETs compared with that in SOI devices. The low κ value of the low-k dielectric leads to two facts: i) the temperature in LK SOI is far higher than that of VLKD SOI whose buried layer is made of a low-k dielectric and SiO_2 in the x-direction; ii) the temperature in LK PSOI is slightly higher than that in the CPSOI. Moreover, the temperatures at the Si window for all PSOI devices are close to 300 K. It can be concluded that LK PSOI devices can enhance BV and alleviate self-heating effect.

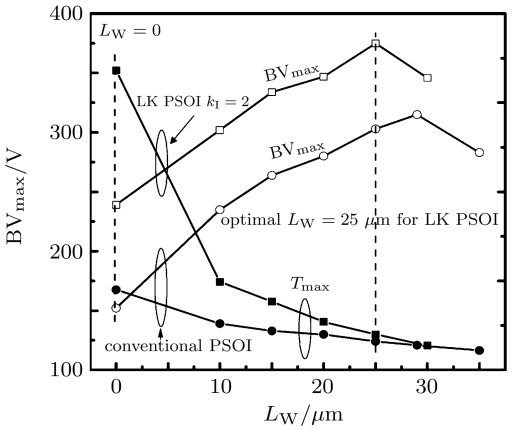


Fig. 7. Dependences of $\rm BV_{max}$ and $T_{\rm max}$ on $L_{\rm W}$ ($t_{\rm S}$ = 2 μm, $t_{\rm I} = 1$ μm, $L_{\rm d} = 30$ μm, $L = 40$ μm).

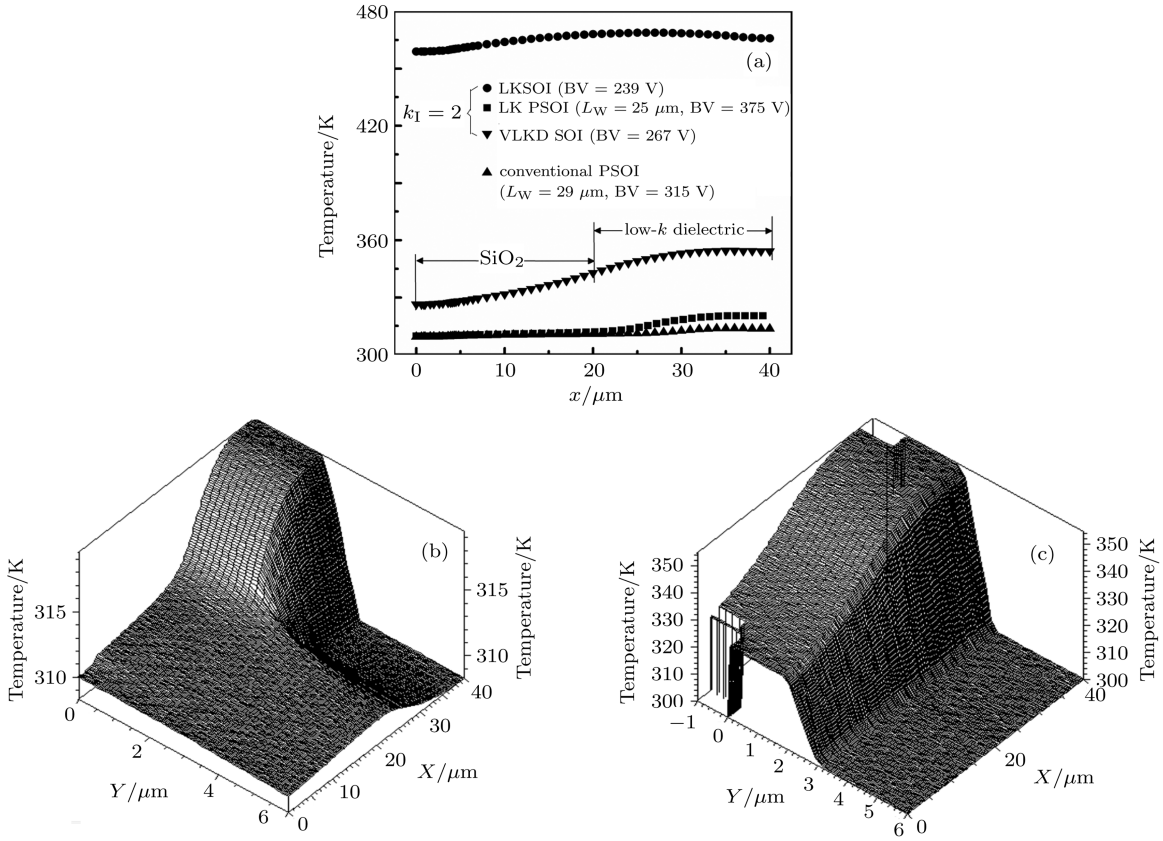


Fig. 8. Temperature distributions ($t_{\rm S} = 2$ μm, $t_{\rm I} = 1$ μm, $L_{\rm d} = 30$ μm, $L = 40$ μm) (a) Surface temperature profiles; 3D temperature distributions: (b) LK PSOI ($k_{\rm I} = 2$); (c) VLKD SOI.

One of promising low-k dielectrics as a buried layer can be Fluorinated Silicate Glasses (FSG) with a critical electric field of 9.2–10.1 MV/cm.[[17,18]] Its low k value is achieved by replacing the Si–O bonds with the less polar Si–F bonds.[17−19] Although F incorporation increases the water-absorption, resulting in the increase of the average k value, its water-resistivity is improved by doping with carbon.[20,21] This kind of film is formed through adding CH_4 gas into $SiH_4/O_2/CF_4$ gas mixtures by using a plasma-enhanced chemical vapour deposition (PECVD) technique or implanting CF_4 into the thermally grown SiO_2 film, and the k value is in a range of 2.5–2.8.[18,20,21] Figure 9 shows the key steps for LK PSOI wafer with carbon- doped FSG buried layer: i) so that dry etch to form Si trench; ii) so that local oxidation to form SiO_2 through steps i) and ii) the planarization of the thick dioxide layer can be avoided; iii) remove the shielding Si_3N_4 and SiO_2 layers, implant CF_4, remove the photoresist and surface planarization; iv) combine the Si vertical growth (VEG) and the lateral epitaxial overgrowth (LEOG) to form the Si device layer.[22] The fabrication process of the LK PSOI LDMOS is the same as that of the conventional SOI LDMOS.

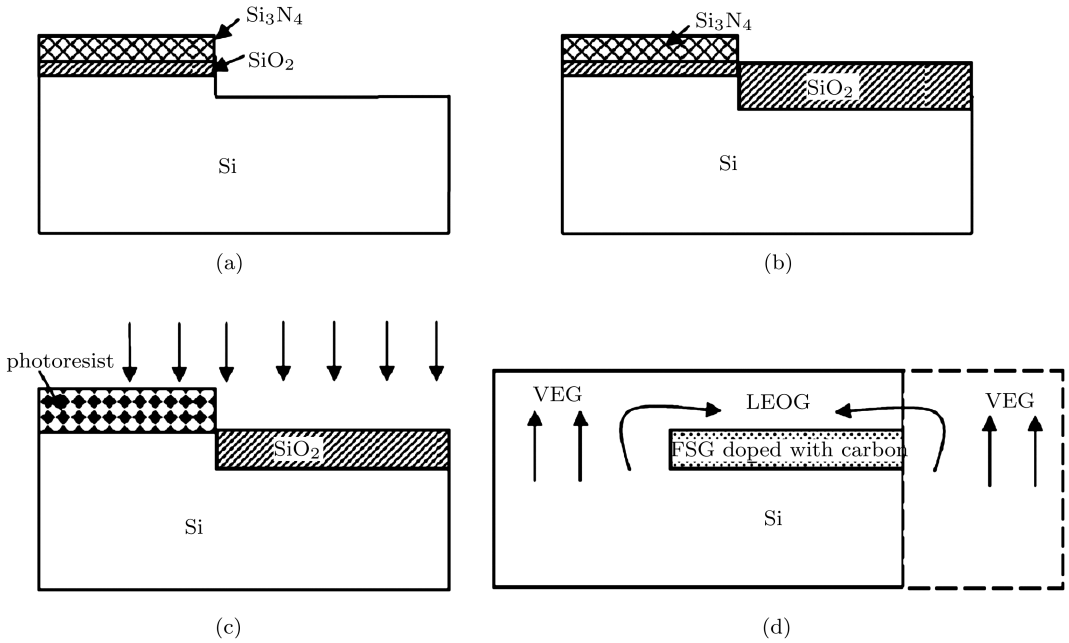


Fig. 9. Key steps of LK PSOI wafer: (a) dry etch to form Si trench; (b) local oxidation; (c) remove the shielding Si_3N_4 and SiO_2 layers, implant CF_4 and surface planarization; (d) VEG and LEOG.

4. Conclusion

A novel LK PSOI high voltage device structure and its breakdown mechanism are presented and investigated by MEDICI. Owing to the enhancement of the electric field in the low-k dielectric as well as the modulation effects of the low-k dielectric and the Si window on the electric field in the SOI layer, E_I and BV for LK PSOI with $k_I = 2$, $t_S = 2$ μm and $t_I = 1$ μm are enhanced by 74% and 19% compared with those for the conventional PSOI, respectively. The self-heating effect is reduced by the Si window. The promising low-k dielectric as a buried layer of SOI wafer and fabrication methods are discussed.

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