# Properties of $C_{60}$ thin film transistor based on polystyrene*

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This paper reports that the n-type organic thin-film transistors have been fabricated by using $C_{60}$ as the active layer and polystyrene as the dielectric. The properties of insulator and the growth characteristic of $C_{60}$ film were carefully investigated. By choosing different source/drain electrodes, a device with good performance can be obtained. The highest electron field effect mobility about 1.15 $cm^2/(V \cdot s)$ could reach when Barium was introduced as electrodes. Moreover, the $C_{60}$ transistor shows a negligible 'hysteresis effect' contributed to the hydroxyl-free of insulator. The result suggests that polymer dielectrics are promising in applications among n-type organic transistors.

**Keywords:** organic thin film transistors, n-type, $C_{60}$, polystyrene
**PACC:** 7340Q, 7360R, 7360T

## 1. Introduction

Organic thin film transistors (OTFTs) have gained a lot of interest mainly due to their potential applications in low cost and flexible electronics. The performance of OTFTs has been improved rapidly in the last decade. To date, the mobility of p-type OTFTs can already compare with that of amorphous silicon thin film transistors (1 $cm^2/(V \cdot s)$).[1−4] The p-type pentacene transistors even have attempted to use in driven active matrix organic light-emitting diode (OLEDs) displays.[5] However, in order to realise applications, such as in organic complementary logic circuits, both p-type and n-type transistors are needed and should have comparable performances. Because there are most reports focusing on the p-type OTFT, recently, developing high performance n-type OTFTs is demanded highly.[6−8]

The development history of the n-type $C_{60}$ transistor is over 10 years, since the first report about it was published by Haddon *et al.* in 1995.[9] However, the breakthrough about the performance of $C_{60}$ OTFTs was done in more recently. In 2006, Anthopoulos *et al.*[10] fabricated $C_{60}$ TFTs with high mobility of 6 $cm^2/(V \cdot s)$ based on $C_{60}$ films grown by hot wall epitaxy upon dirinyltetramethyldisiloxane-biscbenzocyclobutene (BCB) substrate under substrate temperature at 250 °C. In 2007, Zhang *et al.*[11] reported that the electric mobility of $C_{60}$ OTFTs can reach more than 2.5 $cm^2/(V \cdot s)$ by modifying the $SiO_2$ insulator. One problem of the $C_{60}$ transistors is unstable in the air. However, Horiuchi *et al.*[12] reported that the $C_{60}$ OTFTs can operate steadily in the air for more than one month using the passivation layer of alumina ($Al_2O_3$). Due to the high electric mobility and the possibility of operating in air normally, $C_{60}$ is a very promising material to utilise in commercial products now.

On the other hand, it is well known that OTFTs work in the accumulation region and most of the modulated charge lies in the semiconductor near the insulator/semiconductor interface. And the interaction between gate insulator and the semiconductor plays an important role in the formation about morphology of active semiconductor and in the carrier transport.[13] Thus, to investigate the property of OTFTs based on different dielectric seems to be very critical. For simple low-cost, low temperature fabrication process and large area flexible applications, polymer dielectric with solution process are more attractive to use in the OTFTs. But until now, there have been few reports about n-type OTFTs based on polymer dielectric with high performance (>1 $cm^2/(V \cdot s)$).[10] In this paper, we report on the fabrication and performance of n-type $C_{60}$ transistors based on polystyrene (PS) as the

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dielectric. The device shows a high electron mobility of 1.15 $cm^2/(V \cdot s)$.

## 2. Experimental

Fullerene $C_{60}$ OTFTs were fabricated with a top contact configuration, as shown in Fig. 1. The glass substrate with pre-formed indium tin oxide (ITO) layer (100 nm) was used as the gate electrode. The PS layer was prepared by spin-coating from a p-xylene solution (70 mg/ml in concentration) on the ITO substrate and baked on a hot plate at 100 °C for 60 minutes. After naturally cooling at room temperature, the thickness of insulating film was measured to be about 522 nm. A $C_{60}$ film with 100 nm thickness was thermally deposited in a vacuum under a pressure of $3\times10^{-4}$ Pa as the active layer. The deposition rate of approximately 1 Å/s and the substrate was maintained at room temperature. To complete the TFT structure, on the top of the $C_{60}$ layer, different source-drain metal (S/D) electrodes, Ba (4 nm)/Al (100 nm), Al (100 nm) or Au (100 nm) with low to high work-function (2.7 eV for Ba, 4.1 eV for Al, and 5.1 eV for Au), were thermally evaporated through a shadow mask, respectively. The length ($L$) and width ($W$) of the channel were 100 $\mu$m and 10 mm, respectively, shaped in an inter-digital structure.

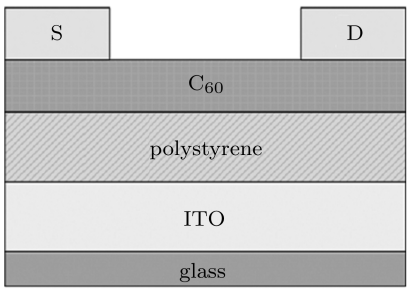



**Fig. 1.** Schematic structure of OTFTs.

The ITO/dielectric/Au (MIM) structures were fabricated to evaluate the capacitance–frequency ($C$–$F$) and current density–electric field ($J$–$E$) characteristics of dielectric layers. The contact area is estimated to be 0.024 $cm^2$. The $C$–$F$ characteristics were measured by an HP 4192A impedance analyser during the sweep frequency was changed from $10^4$ Hz to $10^6$ Hz. Both the electrical characteristics of the OTFTs and the $J$–$E$ characteristics of dielectric were measured in nitrogen atmosphere with an Agilent 4155C semiconductor parameter analyser. The surface morphology of the films was examined by atomic force microscopy (AFM, DI MultiMode Nanoscope IIIa, Veeco) operating in tapping mode.

## 3. Results and discussion

Figure 2 exhibits the $C$–$F$ and the $J$–$E$ characteristics (inset) of PS dielectric. For the 522 nm-thick PS layer, the capacitance per unit area of the insulator was 4.1 $nF/cm^2$ at 1 MHz. Thus, the relative dielectric constant ($k$) of the PS was estimated to be 2.4. This $k$ value is similar with the previously reported value.[14] Furthermore, the PS dielectric had a very small leakage current less than $1.5\times10^{-8}$ $A/cm^2$ even at the electric field of 1.85 MV/cm (the voltage is 100 V), as shown in inset of Fig. 2. Assuming an active transistor area of less than 0.04 $cm^2$, at the gate voltage of 60 V, the transistor gate leakage is less than 250 pA. Therefore, comparing the $10^{-4}$ A of the drain current in the experiment, we do not suppose the gate leakages to affect the performance of transistors.

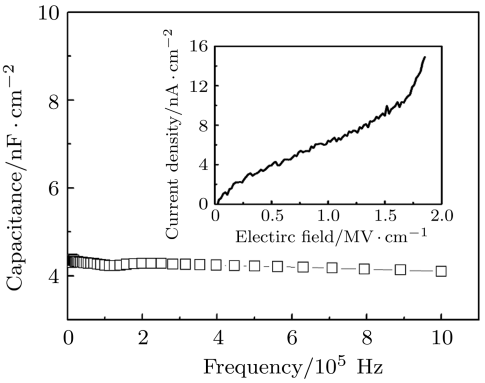



**Fig. 2.** Plots of $C$–$F$ and $J$–$E$ characteristics of PS insulator in the ITO/PS/Au structure.

Since OTFTs work in the accumulation region and most of the modulated charge lies within the first 10 nm in the semiconductor near the interface, the gate dielectric layer roughness can strongly influence the performance of OTFTs. Increased roughness leads to valleys in the channel region, which may act as carrier traps and various scattering. Consequently, the mobility decreases drastically. The case has been reported in pentacene TFTs with inorganic gate dielectrics such as $SiO_2$.[15] They showed that the mobility decreased from 0.49 $cm^2/(V \cdot s)$ to 0.11 $cm^2/(V \cdot s)$ as the rms roughness of the $SiO_2$ gate dielectric layer increased from 0.24 to 1.15 nm. Similar effect was also found in n-type $C_{60}$ transistors based on $Ba_{0.4}Sr_{0.6}Ti_{0.96}O_3$ (BST) dielectric.[16] Due to the

large roughness of the BST insulator, a very low mobility of $4.1\times10^{-5}$ cm$^2$/(V·s) was obtained. In contrast, the PS film can provide a very smooth surface. Figure 3(a) shows the AFM image of PS film surface on coarse ITO substrate. The rms roughness was only 0.283 nm. Thus, a high quality conductive channel at the interface between semiconductor and insulator was expected. Figure 3(b) shows the surface morphology of $C_{60}$ film upon PS layer. The small grains, which is characteristic to that observed previously when $C_{60}$ films was deposited at room temperature.[11] But the grain size can be increased by increasing the substrate temperature during the $C_{60}$ film growth.[17]

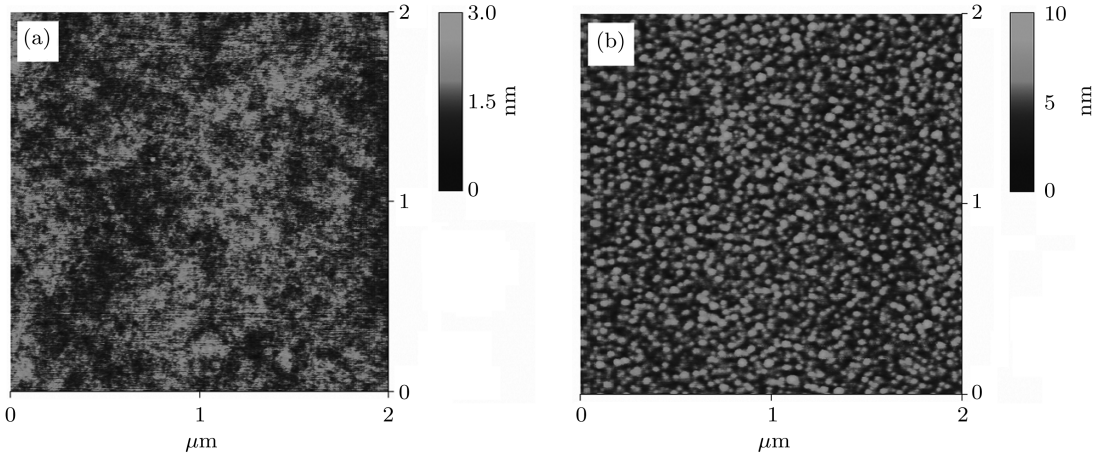



**Fig. 3.** The AFM image: (a) PS (522 nm) layer coated on ITO; (b) $C_{60}$ film deposited on the PS layer.

It has been reported that the enhancement of crystallinity can increase the mobility in $C_{60}$ transistors.[18] In order to further understand the property of the $C_{60}$ film upon PS, we then test the the semiconducting film by x-ray technique. The result is not displayed here. However, no diffraction peaks are detectable, indicating an amorphous structure obtained in our experiment. Such amorphous structure can be observed when the $C_{60}$ film is deposited by simple thermal evaporation on $SiO_2$.[19]

Figure 4(a) illustrates the output characteristic of the transistor based on PS dielectric with Ba/Al S/D electrodes. The drain and gate voltages are in range of 0 to 60 V. The transistor operates in the n-channel accumulation mode and shows a clear saturation behaviour. When $V_G = 60$ V, the on state current can reach as large as 247.9 $\mu$A. Figure 4(b) shows the corresponding transfer characteristic of the OTFT. At the saturation region, the carrier mobility ($\mu$) can be calculated from a plot of the squre root of drain current versus $V_G$ by the following equation:

$$I_{DS} = \frac{WC_i}{2L}\mu(V_G - V_T)^2, \tag{1}$$

where $W$ is the channel width and $L$ is the channel length, $C_i$ is the capacitance per unit area of the insulator and $V_T$ is the threshold voltage. The on/off current ratio was defined as the ratio of $I_{on}$ ($V_G = 60$ V)/$I_{off}$ ($V_G = 0$ V) at $V_{DS} = 60$ V. Accordingly, a high electron mobility of 1.15 cm$^2$/(V·s) can be extracted. The threshold voltage and on/off ratio were 29 V and $3.2\times10^5$, respectively. And the subthreshold slope $S$ which determines the sharp turn in the behaviour of the transitor is given by

$$S = \frac{dV_{GS}}{d(\log I_{DS})}. \tag{2}$$

The present device exhibits an $S$ of 4.3 V/decade due to the large thickness of dielectric.[20]

Actually, the $\mu$ value is closely related to injection efficiency from S/D electrodes to semiconductor film. Here, we proposed that the use of Ba electrodes can make excellent injection characteristic because the work function of Ba (2.7 eV) is much lower than the energy level of lowest unoccupied molecular orbital (LUMO) of $C_{60}$ (3.57 eV). To confirm the role of the Ba electrodes, we then fabricated the transistors with Al or Au as the S/D electrodes, respectively. Figures 5(a) and 5(b) show the output characteristics of the transistors with such two metals. Under the same $V_{GS}$ of 60 V, the saturated current decreased to

175.56 $\mu$A for Al-device and 14.55 $\mu$A for Au-device. As a result, the determined parameters about $\mu$, $V_T$ and on/off current ratio were 0.97 cm$^2$/(V·s), 30 V and $2.8\times10^5$ for Al-device, and 0.126 cm$^2$/(V·s), 36 V and $6.7\times10^4$ for Au-device. Obviously, the performance of devices got worse with increasing the contact barrier. When the electrodes were changed from Ba to Au, not only the mobility decreased, the threshold voltage also increased. The mobility increases near 10 times in the transistor with Ba/Al electrodes in comparison with that of the transistor with Au electrodes. However, since it has been found that the mobility in $C_{60}$ transistors with Pt (5.65 eV) electrodes was strangely higher than that of transistors with Au,[21] the modification of local electronic structure at the interface between special metal and $C_{60}$ should be further investigated. The parameters for all devices in our experiment are summarized in Table 1.

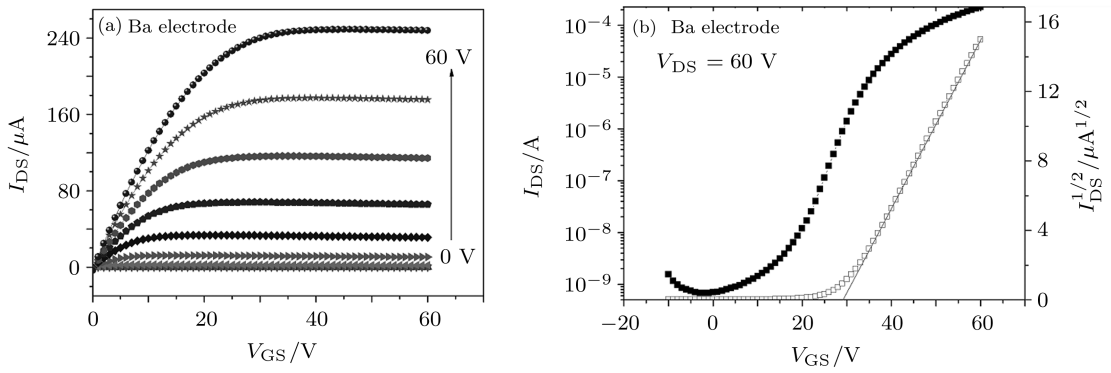



**Fig. 4.** Electrical output characteristic (a) and transfer characteristic (b) of the $C_{60}$ OTFTs based on PS insulator with Ba / Al electrodes.

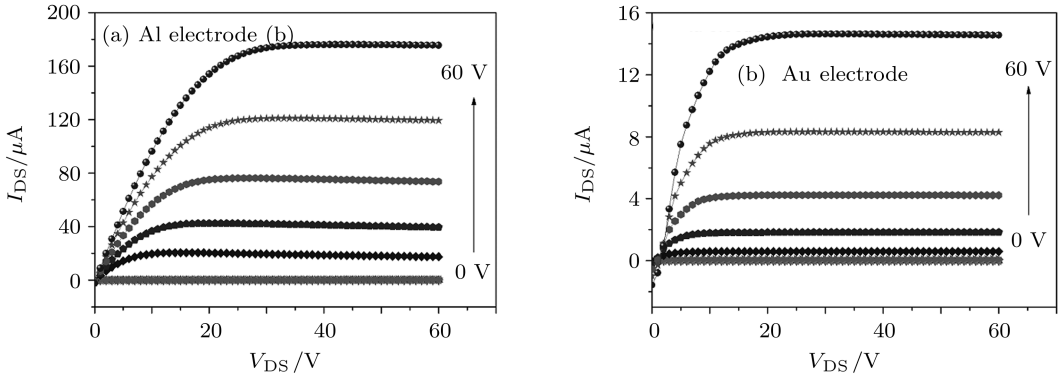



**Fig. 5.** Electrical output characteristics of $C_{60}$ OTFTs based on PS insulator with (a) Al electrodes or (b) Au electrodes.

**Table 1.** Parameters of the transistors.

| electrode | $\mu$/(cm$^2$/(V·s)) | $V_T$/V | on/off ratio | $S$/(V/decade) |
|---|---|---|---|---|
| Ba | 1.15 | 29 | $3.2\times10^5$ | 4.3 |
| Al | 0.97 | 30 | $2.8\times10^5$ | 4.2 |
| Au | 0.126 | 36 | $6.7\times10^4$ | 4.7 |

Besides forming a smooth surface with low baking temperature and the good insulating characteristics, the hydroxyl-free properties can be an original motivation to choose the PS as the dielectric. In n-type OTFTs, OH-groups (silanol groups) appeared at the dielectric surface can trap electron easily, which could lower the mobility and make a large hysteresis. Moreover, since such electrons are often trapped irreversibly, the performance of devices will weaken drastically even cease working after a certain time of continuous stress due to the shift of the threshold voltage.[22] By measuring, the water contact angle of the PS layer surface is 89°. Thus, a hydrophobic surface condition can be provided and the number of electron traps can be decreased obviously. Figure 6

shows the 'hysteresis effect' of $C_{60}$ transistors with different S/D electrodes. All device shows good electrical stability. And the small hysteresis, which could not lead the threshold voltage shift, was observed in the current–voltage characteristics during the sweep direction of gate voltage from –10 V to 60 V (off to on state) and 60 V to –10 V (on to off state). Interestingly, although all devices have the same insulator/semiconductor interface, we notice that the Au-deice have a largest hysteresis comparing with others. Recently, Li *et al.*[23] have showed the different metal gate electrode on hysteresis characteristics of OTFTs. We then suspect that the hysteresis effect of transistor also can be influenced by S/D electrodes.

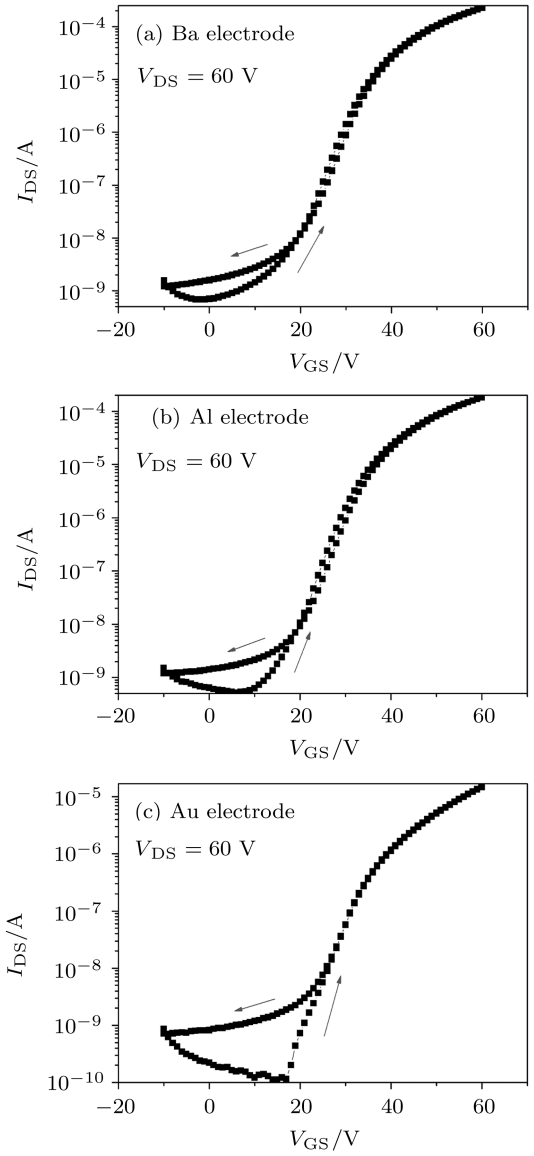



**Fig. 6.** 'Hysteresis effect' of $C_{60}$ transistors with different S/D electrodes.

## 4. Conclusion

In conclusion, we have successfully fabricated high performance n-type $C_{60}$ transistors based on polymer dielectric by depositing the semiconductor layer with a simple vacuum vapour deposition process at room temperature. Although the deposited $C_{60}$ film upon PS is of amorphous structure, the PS can provide a hydroxyl-free condition and a smooth surface, which are very helpful for forming a high quality conductive channel for the electron transport. Furthermore, the Barium electrodes were utilized for the excellent injection characteristic in $C_{60}$ OTFTs. Thus, a transistor with electron mobility as high as 1.15 $cm^2/(V \cdot s)$ and negligible 'hysteresis effect' was obtained. Such results might suggest some attractive interests in the investigation of n-type $C_{60}$ transistors based on polymer dielectrics.

## Ackonwlegement

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